Synchronous All-Optical Code-Division Multiple-Access Local-Area Networks with Symmetric Codes

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Abstract: A non-coherent synchronous all-optical code-division multiple-access (CDMA) network is proposed. In this network, symmetric codes derived from prime sequence codes are used. We present the construction of symmetric codes and show that the pseudo-orthogonality of the new codes is the same as that of the original prime-sequence codes while the cardinality of the new codes is larger than that of the prime sequence codes and the modified prime codes in the same field GF(p). Therefore, an optical CDMA LAN using symmetric codes can have a larger number of potential subscribers. The new codes allow designing fully programmable serial all-optical transmitter and receiver suitable for low-loss, high-capacity, optical CDMA LANs. It is also shown that compared to systems using modified prime codes the proposed system can achieve better BER performance for low received chip optical power.

1. Introduction

Code-division multiple-access (CDMA) techniques have been widely used in satellite and mobile radio communication systems. In recent years, many authors have proposed to apply CDMA techniques in future very high-speed optical fiber networks. Depending on the requirement of time synchronization, there are asynchronous or synchronous optical fiber CDMA systems. Comparing with asynchronous CDMA (A/CDMA) network, synchronous CDMA (S/CDMA) that requires network access among all users be synchronized can provide higher throughput (i.e. more successful transmission) and accommodate more subscribers.

In recent years, some non-coherent optical S/CDMA schemes have been proposed. Among the families of codes proposed so far for optical S/CDMA are modified prime codes, quadratic congruence codes, which can be generated/correlated by all-optical transmitter/receiver based on parallel optical delay lines [1]. The main disadvantage of the parallel delay-line transmitter/receiver is the very high optical loss due to the use of optical splitter and combiner. In order to overcome this drawback, serial transmitter and receiver based on optical fiber lattices have been proposed for non-coherent optical S/CDMA networks using modified prime codes [2]. However, the system described in [2] is not an all-optical system but an electro-optical one, where the processing speed is limited by the speed of the controlling electronics used for changing the state of electro-optical switches. Therefore, the huge bandwidth of optical fiber is not efficiently exploited.

In this paper we propose a non-coherent all-optical S/CDMA LAN based on a new class of symmetric codes. The construction of the new codes is presented. Those codes are derived from the symmetric codes for non-coherent all-optical A/CDMA networks [3], which in turn are generated based on prime sequence codes [4]. In order to differentiate the new codes from the original symmetric codes we called them *synchronous symmetric codes (SSC)*. We shown that the pseudo-orthogonality of synchronous symmetric codes is not different from that of prime sequence codes while the cardinality (that is, the number of code sequences) of the new codes is larger than that of prime sequence codes and modified prime codes. The architecture of all-optical fully programmable transmitter and receiver, which cause significantly lower optical loss as compared to the transmitter and receiver based on parallel optical delay lines is also proposed. Finally, the BER of the proposed system is compared to that of systems using modified prime codes described in [5].

2. Symmetric Codes for S/CDMA

A prime sequence [4] $S_i = \{s_{i,0}, s_{i,1}, \ldots, s_{i,j}, \ldots, s_{i,p-1}\}$ is constructed by $s_{i,j} = i.j \pmod p$ where $i,j \in GF(p)$, the Galois field with prime number p. A binary prime sequence (BPS) is generated by mapping a prime sequence S_i into a binary sequence $C_i = \{c_{i,0}, c_{i,1}, \ldots, c_{i,k}, \ldots, c_{i,N-1}\}$ of length p^2 according to

$$c_{i,k} = \begin{cases} 1 & \text{for } k = s_{ij} + jp \\ 0 & \text{otherwise} \end{cases}$$

A prime sequence code (PSC) consists of p BPS C_i, which is made up of p subsequences of length p. Each subsequence has only one "1" chip and the value of each $s_{i,j}$ in the prime sequence S_i represents the position of the "1" chip in the jth subsequence. For $i \in GF(p)$, the adjacent delay between two "1" chips of C_i generated by S_i is defined as [3]

$t_j = s_{i,j+1} \pmod p - s_{i,j} \pmod p + p$ for $j \in [0,p-2]$.

It has been shown in [3] that the adjacent delays t_1^i, $t_2^i, \ldots, t_{p-2}^i$ of the ith binary prime sequence $(0 \le i \le p-1)$ in $GF(p)$ are related by $t_j^i = t^i_{p-1-j}$ for $0 < j < (p-1)/2$. Based on this characteristic, synchronous symmetric code sequences of weight equal $2^n < p$ (that is, the number of "1" chips in each code sequence is 2^n, for $n = 2,3,\ldots$) can be constructed from binary prime sequences of weight p [3]. However, in this paper only the construction of symmetric code sequences of weight 4 is presented. The construction of symmetric codes of higher weight will be reported in other literature.

Starting from a binary prime sequence C_i of weight p and length p^2 symmetric code sequences of weight 4 and length $p(p-1)$ for S/CDMA can be constructed by the following algorithm.

Step 1: From the ith binary prime sequence C_i of weight p $(0 \le i \le p-1)$, for each integer m such that $1 \le m \le (p-3)/2$, the adjacent delays $\Delta_1^{i,m}$, $\Delta_2^{i,m}$ and $\Delta_3^{i,m}$ of a new symmetric code sequence are determined by

$$\Delta_1^{i,m} = t^i_1 + t^i_2 + \ldots + t^i_m$$
$$\Delta_2^{i,m} = t^i_{m+1} + t^i_{m+2} + \ldots + t^i_{p-m-2}$$
$$\Delta_3^{i,m} = t^i_{p-m-1} + t^i_{p-m-2} + \ldots + t^i_{p-2}$$

where t^i_r $(1 \le r \le p-2)$ are the adjacent delays of the ith binary prime sequence.

Step 2: Keep the "1" chips of the binary prime sequence C_i corresponding to $\Delta_1^{i,m}$, $\Delta_2^{i,m}$ and $\Delta_3^{i,m}$ unchanged. All other "1" chips of the binary prime sequence are replaced by "0".

Step 3: Truncate the first p "0" chips of the obtained sequence. The resulting sequence A_{im} is of length $N=p(p-1)$, weight 4 and can be represented by a quadruple $SA_{im} = (t^i_0 - p, \Delta_1^{i,m}, \Delta_2^{i,m}, \Delta_3^{i,m})$, where $t^i_0 - p$ is the number of "0" chips preceded the first "1" chip, $\Delta_1^{i,m}$, $\Delta_2^{i,m}$, $\Delta_3^{i,m}$ are the adjacent delays. From a binary prime sequence C_i $(p-3)/2$ symmetric code sequences A_{im} can be constructed [3].

Step 4: Each of $p(p-3)/2$ symmetric code sequence A_{im} is taken as a seed from which a group of new sequences can be generated. Left-rotate W chips "1" of sequence A_{im} $p-1$ times to create $(p-1)$ new sequences A_{imt} where t $(0<t<p)$ represents the number of times A_{im} has been left-rotated.

Step 5: Exclude any of the sequences A_{imt}., which are not symmetric, we obtain a new set of synchronous symmetric code sequences for S/CDMA networks.

Table 1 shows all the sequences A_{imt} of weight 4 and length 20 generated in GF(5). Note that each synchronous symmetric code sequence $A_{i,m0}$ is the same as the original symmetric code sequence A_{im} whereas the other synchronous symmetric code sequences $A_{i,mt}$ (with $t \neq 0$) are time-shift versions of A_{im}. It can be seen that there are 8 non-symmetric sequences: A_{112}, A_{114}, A_{212}, A_{214}, A_{312}, A_{314}, A_{412}, A_{414}, which must be excluded. The remaining 17 sequences are symmetric.

We find that the number V of synchronous symmetric code sequences generated in GF(p) can be calculated by the following formula

If $p=4k+1$ (k is positive integer)

$$V = (2k-1)(8k^2+8k+1) - 8\sum_{i=0}^{k-1} i(i-2k+1)$$

If $p=4k+3$

$$V = 2k(8k^2+18k+7-8\sum_{i=0}^{k-1} i(i-2k)$$

Table 2 shows the sequence length N, the cardinality V of synchronous symmetric codes (SSC), prime sequence codes (PSC) [4] and modified prime codes (MPC) [5]. It can be seen that compared to the other two codes the number of the synchronous symmetric code sequences is larger while the sequence is shorter (for the same $p>5$).

Table 1. Synchronous Symmetric Sequences in GF(5) for S/CDMA

i	$A_{i,mt}$	Synchronous symmetric code sequences for S/CDMA
0	A_{010}	10000,10000,10000,10000
	A_{011}	00001,00001,00001,00001
	A_{012}	00010,00010,00010,00010
	A_{013}	00100,00100,00100,00100
	A_{014}	01000,01000,01000,01000
1	A_{110}	01000,00100,00010,00001
	A_{111}	10000,01000,00100,00010
	A_{112}	**00001,10000,01000,00100**
	A_{113}	00010,00001,10000,01000
	A_{114}	**00100,00010,00001,10000**
2	A_{210}	00100,00001,01000,00010
	A_{211}	01000,00010,10000,00100
	A_{212}	**10000,00100,00001,01000**
	A_{213}	00001,01000,00010,10000
	A_{214}	**00010,10000,00100,00001**
3	A_{310}	00010,01000,00001,00100
	A_{311}	00100,10000,00010,01000
	A_{312}	**01000,00001,00100,10000**
	A_{313}	10000,00010,01000,00001
	A_{314}	**00001,00100,10000,00010**
4	A_{410}	00001,00010,00100,01000
	A_{411}	00010,00100,01000,10000
	A_{412}	**00100,01000,10000,00001**
	A_{413}	01000,10000,00001,00010
	A_{414}	**10000,00001,00010,00100**

Table 2. N and V of SSC, PSC and MPC

p	**SSC**		**PSC**		**MPC**	
	N	**V**	**N**	**V**	**N**	**V**
5	20	17	25	5	25	25
7	42	66	49	7	49	49
11	110	324	121	11	121	121
13	156	565	169	13	169	169
17	272	1351	289	17	289	289
19	342	1928	361	19	361	361
23	506	3530	529	23	529	529

The generation of synchronous symmetric sequences is based on removing the $p-4$ unwanted "1" chips from binary prime sequences of weight p. Hence, the cross-correlation constraint of the new codes is not different from that of prime sequence codes. That is, the maximum cross-correlation of two synchronous symmetric code sequences is equal 2.

3. Optical Transmitter and Receiver

The optical transmitter and receiver for synchronous all-optical CDMA LANs using synchronous symmetric codes of weight 4 are designed based on programmable optical lattices [6]. A programmable optical lattice of L stages consists of a cascade of $L+1$ 2x2 electro-optic switches and L $(L \geq 1)$ optical delay lines. The lth delay line $(0 \leq l \leq L)$ causes a delay equal $2^{l-1}T_c$, where T_c is the duration of the sequence chip time. Each 2x2 electro-optic switch can be configured into two possible states (i.e. cross-state or bar-state) according to its DC bias voltage controlled by the electronic control circuit. The total amount of delay that an optical pulse experiences when passing through the lattice can be varied from $0T_c$ to $(2^{L-1}-1)T_c$ and the delay depends on the states of all the 2x2 electro-optic switches.

The schematic diagram of a fully programmable optical transmitter is shown in Figure 1. In this transmitter three programmable optical lattices are used. When transmitting an "1" bit the optical source generates an optical pulse of maximum pulse width T_c where $T_c = T/(p^2-p)$ is the sequence chip time and T is the bit time and no pulse is emitted for a "0" bit. The pulse is passed through the optical lattice 1 of $L_1 = \lfloor log_2 p \rfloor + 1$ stages, where $\lfloor x \rfloor$ is the integer part of x. This lattice provides the delay preceded the first "1" chip of the sequence and the delay can be any integer value between $0T_c$ and $(p-1)T_c$. The delayed optical pulse is then split into two pulses by a passive splitter S_1 and one of the pulse is delayed by a time of τ_1. For a set of V new sequences of weight 4, the delay τ_1 for the jth sequence $(1 \leq j \leq V)$ is equal Δ_1^j. This delay is provided by the programmable optical lattice 2 of $L_2 = \lfloor log_2 \Delta\tau_1 \rfloor + 1$ stages connected in series with an optical delay of Δ_{1min}, where $\Delta\tau_1 = \Delta_{1max} - \Delta_{1min}$, $\Delta_{1max} = \max(D_1^j)$, $\Delta_{1min} = \min(D_1^j)$, where D_1^j is the first adjacent delay of the jth sequence. The delayed pulse combines with the non-delayed one at the 2x2 coupler S_2. These two pulses then split into four pulses and two of them are delayed by a delay of τ_2. The delay τ_2 for the jth sequence is equal $\Delta_1^{\,j} + \Delta_2^{\,j}$. This delay is provided by the programmable optical lattice 3 of $L_3 = \lfloor log_2 \Delta\tau_2 \rfloor + 1$ stages connected in series with an optical delay of Δ_{2min}, where $\Delta\tau_2 = \Delta_{2max} - \Delta_{2min}$, $\Delta_{2max} = \max(D_1^j + D_2^j)$, $\Delta_{2min} = \min(D_1^j + D_2^j)$, where D_2^j is the second adjacent delay of the jth sequence. All the four pulses are then combined at the passive combiner S_3. Optical symmetric code sequences of weight 4 are obtained at the output of this combiner with the adjacent delays being $(\tau_1, \tau_2, \tau_1 + \tau_2)$. By controlling the control circuit of the lattices 1, 2 and 3 for setting 2x2 switches at the bar or cross-state all V sequences can be generated. If the laser and the optical gate are removed the transmitter can be used as decoder in the receiver. Note that the delays will be set so that they are inversely matched to the pulse spacings in the receiver address sequence.

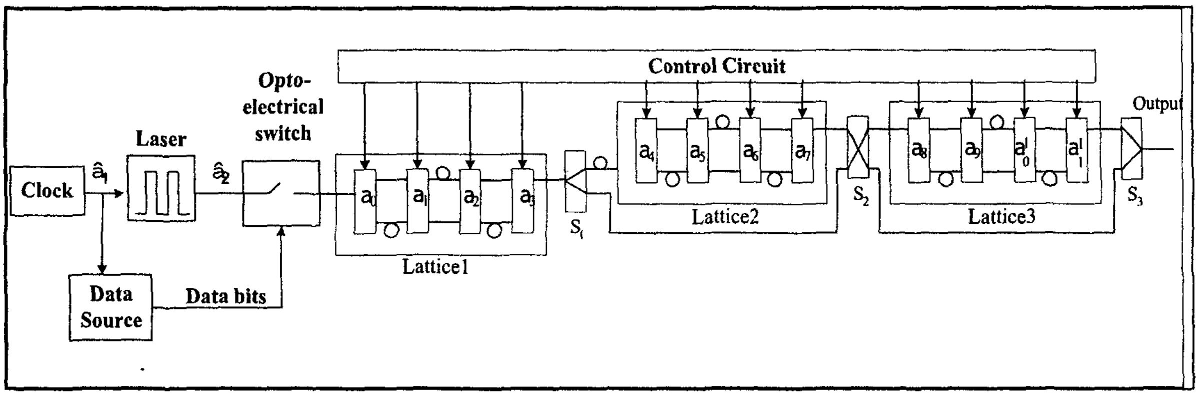

Figure 1 Optical Transmitter

4. BER Performance

We compare the performance of the proposed system with that of the non-coherent synchronous optical CDMA system using modified prime codes [5]. The BER performance for both systems is calculated as a function of the received chip optical power P_s with the number of simultaneous users K as parameter. The effects of interference, shot noise and thermal noise on the BER are considered and the Gaussian approximation presented in [7] is used for calculating the BER performance of two systems. The following parameters are used: Data bit rate D =10 Mb/s, PIN diode of responsivity R=0.8 A/W, dark current noise I_d=10 nA, the power spectral density of the thermal noise $N_{Th} = 10^{-24}$ A^2/Hz, the received chip optical power P_s is varied from -30 dB to 30 dB.

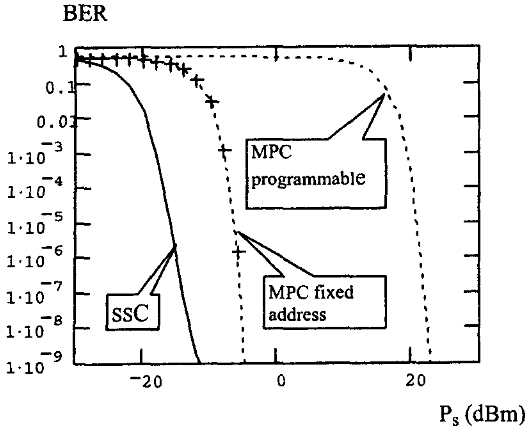

Figure 2. BER for K=3

Figure 2 shows the BER for the proposed system with synchronous symmetric sequences of length N = 506 and that for systems using modified prime sequences of N = 529 (Both fixed address and programmable receivers). The number of simultaneous is K =3. It can be seen that for BER = 10^{-9} the system using synchronous symmetric code requires the lowest received chip optical power (only P_s =-12 dBm) while the system using modified prime codes needs P_s = -5 dBm for (fixed address receiver) and P_s = 23 dBm (for programmable receiver).

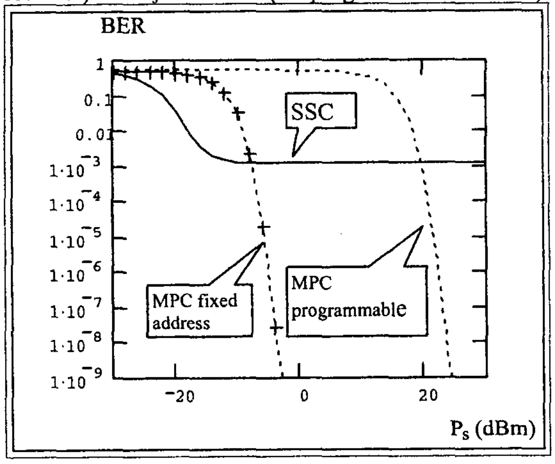

Figure 3. BER for K=10

However, due to the lower weight (W=4) when the number of simultaneous users increases, the BER of the system using synchronous symmetric codes degrades rapidly. This is illustrated in Figure 3, where the BER of the two systems for K=10 is presented. It should be noted that the system using modified prime codes can only achieve BER = 10^{-9} for very high received power (P_s = -3 dBm for fixed address receiver and P_s = 24 dBm for programmable receiver, respectively). For low received power, the BER of systems using modified prime codes is worse than that of the system using synchronous symmetric codes. In order to improve the performance of the proposed system, SSC of higher weight (e.g. W=8 or W=16) are needed. The performance of such systems will be reported in other literature.

5. Conclusions

In this paper we propose a non-coherent synchronous all-optical CDMA LAN using new symmetric codes. The construction of the new codes based on the well-known prime sequence codes is presented. It is shown that the size of a new code is larger than that of the original prime sequence code [4] and the modified prime-code [5] in the same field GF(p). This implies that optical CDMA networks using the new codes can have a larger number of potential subscribers. We also show that the pseudo-orthogonality of the new codes is the same as that of prime sequence codes. The design of fully programmable transmitter and receiver for all-optical CDMA LANs using the new codes is presented. This configuration is particularly attractive for the future ultra-fast optical CDMA networks because of its low-loss and programmable features. Finally, the BER of the proposed system is compared to that of systems using modified prime codes. It is shown that the proposed system can achieve better performance for low received chip optical power.

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