A Cell-Network Type SC DC-DC Converter with Large Current Output

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Abstract: In this paper, an IC realization of a cell-network type SC DC-DC converter is reported. To achieve small and low-cost realization, the converter is designed by using a 1.2 μm CMOS technology. The CMOS implemented converter will be useful as a building block of various mobile equipments since step-up and step-down voltages can be provided at one time. Concerning the proposed DC-DC converter, SPICE simulations are performed to investigate the characteristics of the circuit. The SPICE simulations show that the efficiency of the simulated circuit is more than 95 %. From the layout design using a CAD tool, MAGIC, the VLSI chip is fabricated in the chip fabrication program of VLSI Design and Education Center(VDEC), the University of Tokyo with the collaboration by On-Semiconductor. The proposed circuit is integrable by a standard 1.2 μm CMOS technology.

1. Introduction

A power conversion circuit is one of the most important building blocks for electronic equipments. For the realization of the power conversion circuits, two major approaches have been studied : a power conversion circuit using inductors and an inductorless power transformer using switched-capacitor (SC) techniques. However, magnetic elements such as inductor cause the possibility of faulty operation for neighboring circuits. For this reason, the power conversion circuits using SC techniques attract many researchers' attention. Among others, SC DC-DC converters which can provide a step-up/step-down voltage by controlling the timing of clock pulse received much attention since the mobile equipments such as digital camera require step-up and step-down voltages at one time. For this reason, several attempts have already been made for an IC realization of the SC transformers [1]-[4]. Among others, a ring-type DC-DC converter [1],[2] proposed by Hara et al. is known as an efficient DC-DC converter. In the design of these SC transformers, small number of power-switches is desirable.

In this paper, a cell-network type SC DC-DC converter with bootstrapped gate transfer switches is proposed. The cell structure and the bootstrapped gate transfer switches enables us to realize the DC-DC converter with small number of power-switches. In this study, to achieve low-cost realization, the converter is designed by using a 1.2 μm CMOS technology. Concerning the cell block of the proposed circuit, the VLSI chip is fabricated in the chip fabrication program of VLSI Design and Education Center(VDEC), the University of Tokyo with the collaboration by On-Semiconductor.

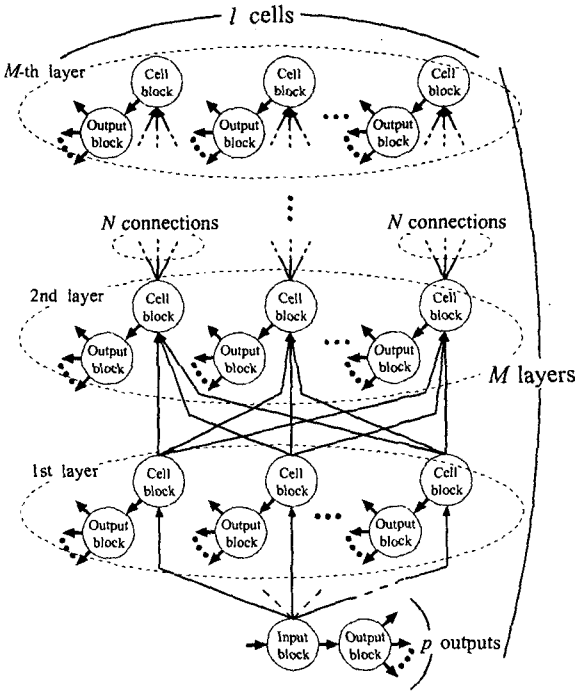

Fig.1 Architecture of the proposed circuit.

2. Circuit Structure

2.1 Block Diagram

Figure 1 shows the architecture of the proposed DC-DC converter with cell structure. The circuit shown in Fig.1 consists of an input block, $(M-1) \times l$ cell blocks, and $(M-1) \times l + 1$ output blocks. The cell block in $j-1$-th layer is connected to the cell blocks in j-th layer $(j = 1, \ldots, M)$. Figure 2 shows the block diagram of the respective building blocks. In the input block of Fig.2 (a), the power-switches connected to the input and GND terminal are expressed by ${}^k S_{ii}^j$ and ${}^k S_{gi}^j$ $((i = 1, \ldots, N)$ and $(k = 1$ and $j = 1))$, respectively. The switch used to realize ring-connection is expressed by ${}^k S_{ri}^j$ $(k = 1$ and $j = 1)$. As an example of the cell

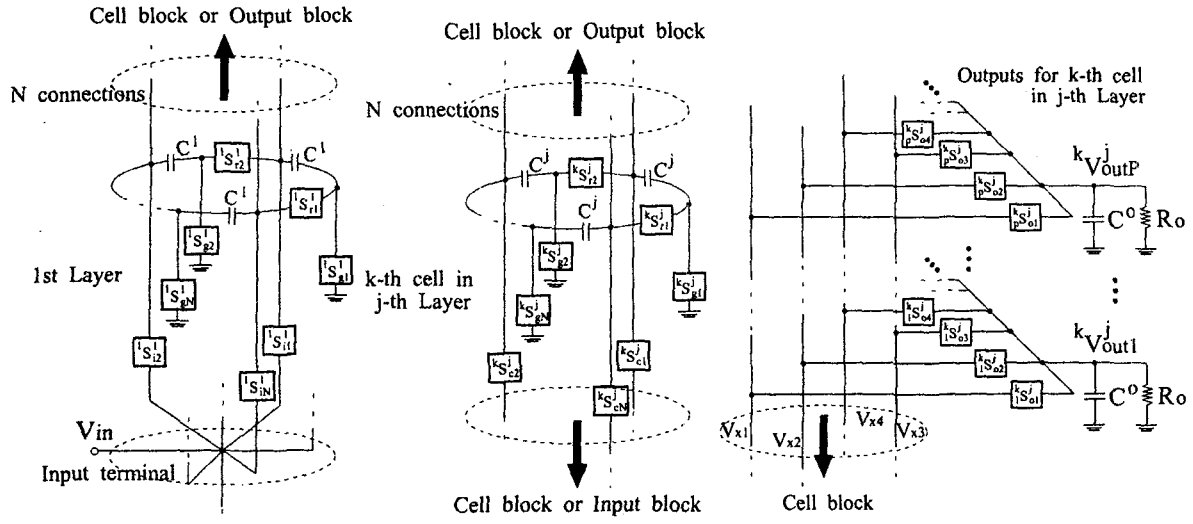

Fig.2 Building block of the proposed circuit. (a) Input block. (b) Cell Block. (c) Output block.

blocks, Fig.2 (b) shows the k-th cell ($k = 1, \ldots, l$) in the j-th layer ($j = 1, \ldots, M$). The cell block is connected to the other blocks via switches ${}^{k}S^{j}_{ci}$'s. Figure 2 (c) shows the block diagram of the output block for k-th cell in j-th layer. The switches connected to the output terminal is expressed by ${}^{k}_{q}S^{j}_{oi}$ ($q = 1, \ldots, p$), where p denotes the number of the outputs of k-th cell in j-th layer. By controlling the switches, the proposed circuit converts a voltage to other by means of changing the connections of capacitors. The clock pulses for ${}^{k}S^{j}_{gi}$'s ($i = 1, \ldots, N$) are non-overlapped N-phase pulses ${}^{k}\Phi^{j}_{gi}$'s and the clock pulses for ${}^{k}S^{j}_{ri}$'s ($i = 1, \ldots, N$) are set to the inverted pulses of ${}^{k}\Phi^{j}_{gi}$'s, respectively. The switches ${}^{k}S^{j}_{ci}$'s and ${}^{k}_{q}S^{j}_{oi}$'s are driven by the clock pulses obtained by shifting the clock-pulses ${}^{k}\Phi^{j}_{gi}$'s cyclically. When the output current is 0 and the voltage-drop caused by power-switches is free, the output voltage is given by

$$ {}^{k}\mathrm{V}^{j}_{\mathrm{outq}} = \frac{\Pi^{j}_{s=1}\ {}^{k}Y^{s-1}\ {}^{k}_{q}O^{j}}{\Pi^{j}_{s=1}\ {}^{k}X^{s}}\mathrm{V_{in}}, \qquad (1) $$

where

$$ {}^{k}Y^{0} = 1. $$

In Eq.(1), ${}^{k}X^{s}$ and ${}^{k}Y^{s-1}$ are the number of capacitors, C^{j}'s, connected to the input terminal and the output terminal of the building block in series, respectively. And ${}^{k}_{q}O^{j}$ is the number of capacitors, C^{j}'s, connected to the j-th output block in series.

On the other hand, the output voltage of a ring-type DC-DC converter [1],[2] proposed by Hara et. al. is given by

$$ \mathrm{V_{out}} = \frac{Q}{P}\mathrm{V_{in}}, \qquad (2) $$

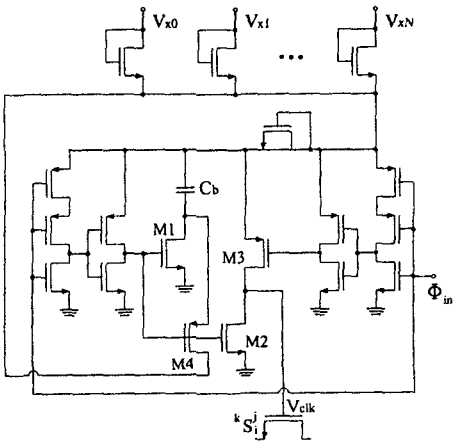

Fig.3 Proposed bootstrapped gate transfer switch.

where P and Q denote the number of the capacitors connected to the input terminal and the output terminal, respectively. As Eqs.(1) and (2) show, the proposed circuit can realize superior DC-DC conversion to the conventional circuit.

2.2 Circuit Design

SC power conversion circuits consist of only capacitors and power-switches. For this reason, the key for the efficient design of the SC converter is a design of power-switches.

Figure 3 shows a bootstrapped gate transfer switch used in the proposed circuit. In Fig.3, the inputs $\mathrm{V_{x0}}$ and $\mathrm{V_{xi}}$'s ($i = 1, \ldots, N$) are connected to the voltage source $\mathrm{V_{in}}$ and the nodes $\mathrm{V_{xi}}$'s in the output block ,respectively.

During the input pulse Φ_{in} is *high*, the MOS-switches M1 and M2 are *on*, and the MOS-switches M3 and M4 are *off*. In this timing, the capacitor $\mathrm{C_b}$ is charged by

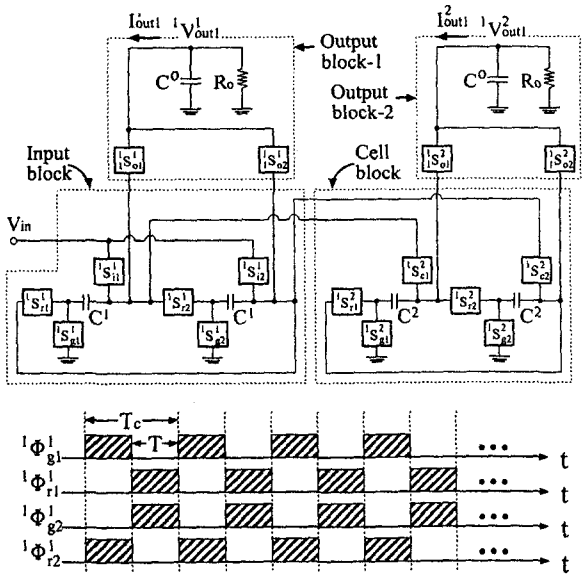

Fig.4 An example of the proposed DC-DC converters. ($\max({}^{k}V^{j}_{outq}) = 4V_{in}$ and $\min({}^{k}V^{j}_{outq}) = V_{in}/4$.)

the maximum voltage V_{max} of V_{xq}'s ($q = 0, 1, \ldots, N$). When voltage-drop caused by MOS-switches is 0, the capacitor C_b is charged to $V_{max} - 2V_{th}$, where V_{th} denotes the threshold voltage of diodes.

On the other hand, during Φ_{in} is *low*, the states of MOS-switches M1, M2, M3, and M4 are reversed. Via M3, C_b, and M4, the gate terminal of the power-switch $S_{i,j}$ is driven by the output voltage V_{clk}. When voltage-drop caused by MOS-switches is 0, the output voltage V_{clk} is given by

$$V_{clk} = \begin{cases} 2V_{max} - 3V_{th} & \text{if } \Phi_{in} = low, \\ 0 & \text{if } \Phi_{in} = high, \end{cases} \quad (3)$$

where

$$V_{max} = \max\{V_{x0}, V_{x1}, \ldots, V_{xN}\}.$$

In Eq.(3), V_{th} denotes the threshold voltage of diode connected MOSFET's.

3. Simulation

To confirm the validity of circuit design, the DC-DC converter which has 6 capacitors, 16 power-switches, and a clock pulse generator was designed by assuming a 1.2 μm process produced by On-Semiconductor. Concerning the circuit shown in Fig.4, SPICE simulations were performed under the conditions that $V_{in} = 3.6V$ [1] , $C = 200nF$, $R_o = 100\Omega$, and $T_c = 0.5\mu s$.

Figure 5 shows the simulated characteristics of bootstrap circuits. Figure 5 (a) shows the simulated characteristics of the proposed circuit shown in Fig.3. Figure

[1]The voltage of the lithium battery used in the mobile equipments is 2.8 ~ 3.8 V.

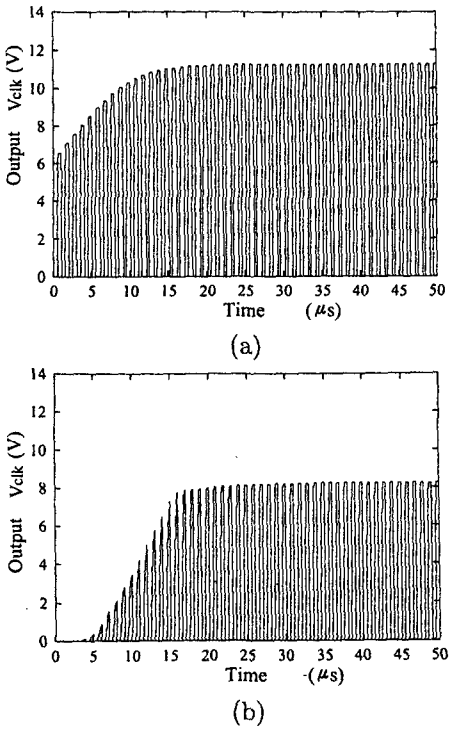

Fig.5 Simulated characteristics of bootstrap circuits. (a) Proposed. (b) Conventional.

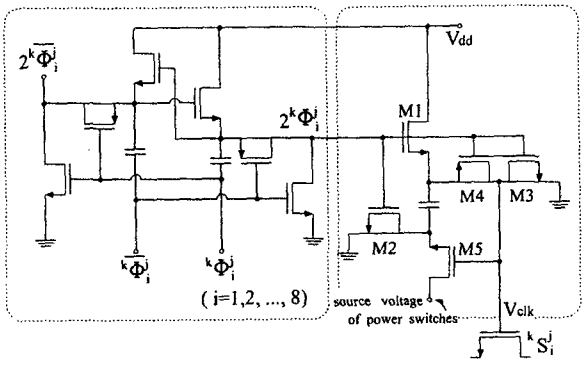

Fig.6 Conventional Bootstrapped gate transfer switch.

5 (b) shows the simulated characteristics of the conventional circuit shown in Fig.6 [5] [2] . The output voltage of the conventional bootstrap circuit is given by

$$V_{clk} = \begin{cases} V_y + V_{in} & \text{if } \Phi_{i,j} = low, \\ 0 & \text{if } \Phi_{i,j} = high, \end{cases} \quad (4)$$

where V_y denotes a source voltage of a power-switch. In Fig.5, the amplitude of input pulse and the supply voltage V_{dd} were set to 3V. The source voltage of power-switches and the nodes V_{xi}'s were set to 6V. As Fig.5

[2]Of course, several types of power converters have been proposed. Among others, Myono et al. proposed efficient circuits by employing level shift circuits [6]. However, these circuits cannot be adopted to step-up and step-down power converters such as ring-type power converters, cell-network type power converters, etc..

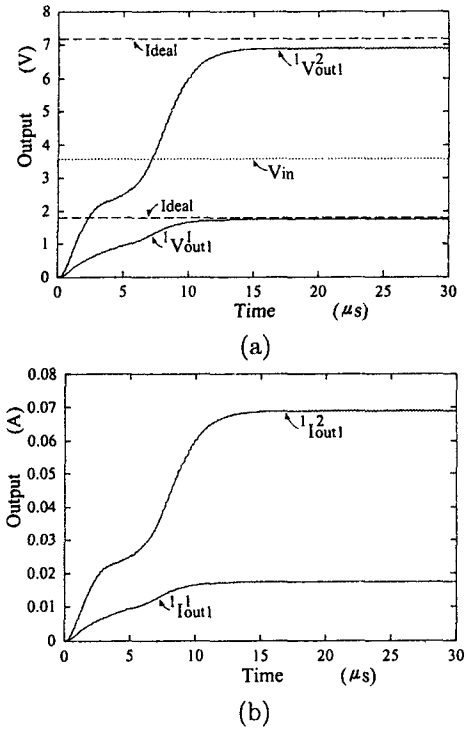

Fig.7 Simulated outputs of the DC-DC converters. (a) Output voltages. (b) Output currents.

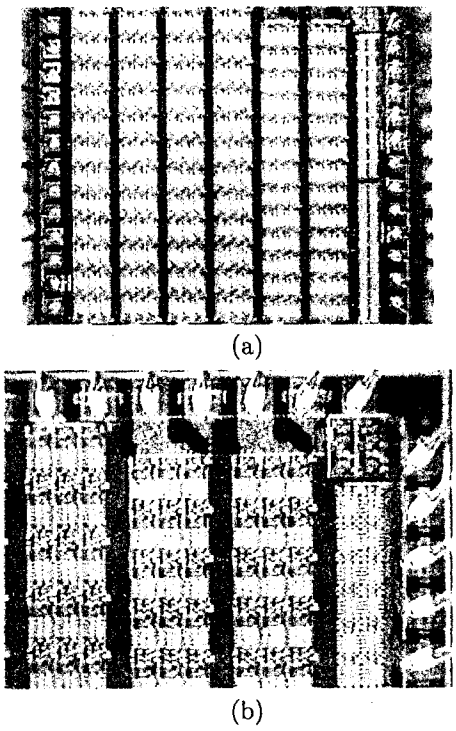

Fig.8 Photograph of the fabricated IC. (a) Total view. (b) Enlarged photograph.

shows, the amplitude of output pulse V_{clk} for the proposed circuit is larger than that of the conventional circuit proposed in [5]. In other word, the proposed switch can achieve small on-resistance.

Figure 7 shows the simulated output voltages. The *ideal* values for the outputs, $2V_{in}$ and $V_{in}/2$, are 7.2 V and 1.8 V, respectively. As Fig.7 shows the proposed circuit can realize a step-up and step-down DC-DC conversion. The efficiency of DC-DC conversion is more than 95 %.

4. IC Implementation

To confirm the circuit design, a cell block with 8 power-switches was implemented onto an IC chip. The layout of this circuit was performed by using an analog CAD tool, MAGIC.

Figure 8 shows the photograph of the fabricated IC. The size of the fabricated IC designed by a 1.2 μm CMOS process is $2.3mm \times 2.3mm$. [3] .

5. Conclusion

An IC realization of a cell-network type SC DC-DC converter has been reported in this paper. The SPICE simulation showed the following results: 1. The proposed SC converter can perform a step-up and step-down DC-DC conversion. 2. The efficiency was more than 95 %. 3. The proposed circuit is implementable by a standard CMOS technology.

[3]The capacitors of the proposed circuit are not included in this IC.

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