CMOS Synaptic Model Considering Spatio-Temporal Summation of Inputs

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Abstract: A number of studies have recently been published concerning neuron models and asynchronous neural networks. In the case of large-scale neural networks having neuron models, the neural network should be constructed using analog hardware, rather than by computer simulation via software, because of the limitation of the computational power. In this paper, we discuss the circuit structure of a synaptic section model having the spatio-temporal summation of inputs and utilizing CMOS processing.

1. Introduction

Brain sub-systems have a high degree of information processing ability, namely recognition and learning. But the information processing functions have not been clarified, as yet. So, neuron models and artificial neural networks (ANNs) have recently been studied, in order to clarify the information processing functions of biological neural networks [1][2].

In traditional ANNs, digital type and analog type neuron models have been used for simplicity. As for these models, the user must decide how the neurons can communicate information. For example, it is necessary to change an input signal into digital and make a pulse density corresponding to the analog quantity. On the other hand, in physiology a biological neuron transmits nerve impulses to other neurons.

We have been trying to produce hardware from the viewpoint that the development of a new hardware neuron model is one of the most important problems in the study of neural networks. If we regard a biological neuron as an element that processes many pulses received asynchronously, a single neuron model should be comprised of a pulse-type hardware neuron model [1]. That is, in the case of considering large-scale neural networks with pulse-type neuron models, it is important to construct the neural network, using hardware rather than computer simulation because of the limitation of the computer speed and memory capacity. In addition, it is necessary to construct a single neuron model, which is suitable for CMOS processing. Also, a biological neuron exhibits chaotic phenomena easily, because of its nonlinear dynamics. For this reason, nonlinear characteristics, including chaos, have been investigated in several neuron models and neural networks [2]-[4].

On the basis of the above considerations, we have been studying the possibility of asynchronous neural networks, including chaotic phenomena with pulse-type hardware neuron models for CMOS-IC [5].

In previous discussions, we have elaborated on the circuit structure of a Pulse-type Hardware Chaotic Neuron Model, (hereafter "P-HCNM"), on the basis of equations from the mathematical model of a chaotic neuron. This P-HCNM incorporates a synaptic section and a cell-body section, and demonstrates the three properties of the chaotic neuron model, i.e. spatio-temporal summation of inputs, relative refractoriness, and graded responses of output pulse amplitude. However, the synaptic section of a P-HCNM needs to be constructed using an analog circuit, which is suitable for CMOS processing in order to constitute a large-scale chaotic neural network implemented by P-HCNM.

In this paper, we discuss the circuit structure of a synaptic section model having a spatio-temporal summation of inputs and utilizing CMOS processing.

2. The CMOS Synaptic Model

In this section, we discuss the structure of the circuit of the CMOS synaptic model having a spatio-temporal summation of inputs. We are convinced that the circuit can be composed of an addition circuit and an integration circuit. The spatial summation circuit is constructed from the addition circuit and the temporal summation circuit is constructed from the integration circuit.

2.1 The Spatial Summation Circuit

Figure 1 shows a diagram of the spatial summation circuit. This circuit can be constructed from the capacitive coupled multi-input MOSFET. Here, in the case of j-th input terminal, the connection weight w_{ij} to which input voltage v_{ij} is applied is as follows:

$$w_{ij} = C_{ij} \Big/ \sum_{j=1}^{m} C_{ij} \,. \tag{1}$$

Therefore, the equation of gate voltage v_g is as follows:

$$v_g = \sum_{k=1}^{m} C_{ik} v_{ik} \Big/ \sum_{j=1}^{m} C_{ij} . \quad (2)$$

Accordingly, the v_g can be expressed with the spatial summation of inputs.

We examine the circuit of the capacitive coupled multi-input MOSFET with 2 input terminals in order to clarify the spatial summation of inputs.

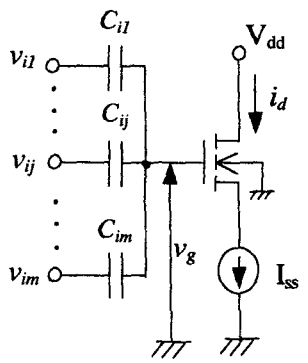


Figure 1: The circuit diagram of the capacitive coupled multi-input MOSFET

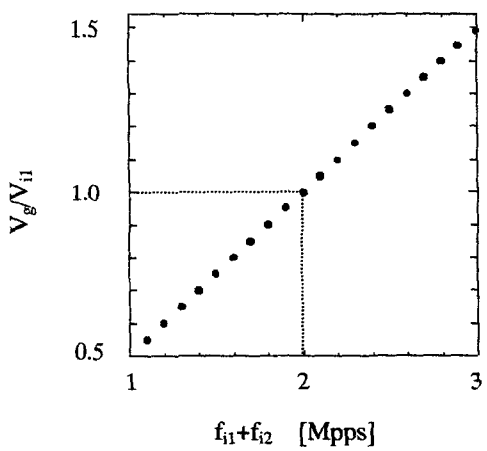


Figure 2: The characteristic of spatial summation of inputs

Figure 2 shows an example of the characteristics of spatial summation of inputs for one input frequency that is fixed and another input frequency that is changed. V_g and V_{i1} are the average values of gate voltage v_g and input voltage v_{i1} respectively and f_{i1} and f_{i2} are pulse densities of input voltages v_{i1} and v_{i2} respectively. We analyze the characteristics of spatial summation of inputs by PSpice, using circuit parameters in Fig.1, the ratio (W/L) of enhancement-mode MOSFET is 1, where W is the gate width and L is the gate length, C_{i1}=1.0[pF], C_{i2}=1.0[pF], I_{ss}=15[μA], V_{dd}=5[V], pulse width is 0.1[μs], pulse amplitude is 2[V] and one fixed frequency is 1[MHz]. This figure shows that if we assume that C_{i1}=C_{i2}, the value of V_g/V_{i1}=1 in the case of f_{i1}=f_{i2}. If the value of f_{i2} is greater than f_{i1}, the value of V_g/V_{i1} is greater than 1.0, and if the value of f_{i2} is less than f_{i1}, the V_g/V_{i1} is less than 1.0. Therefore, this circuit has a property of the spatial summation of inputs.

2.2 The Temporal Summation Circuit

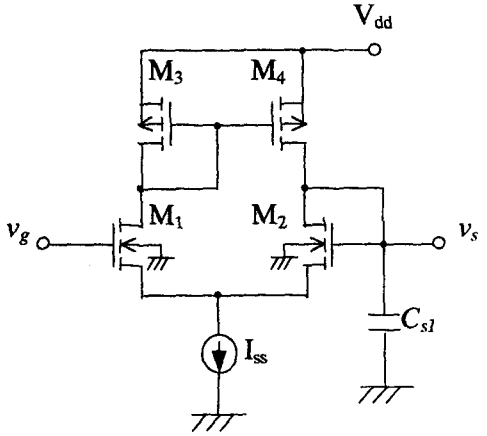


Figure 3: The diagram of the integration circuit

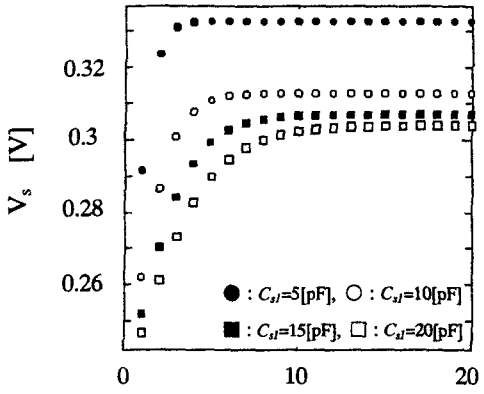
Figure 3 shows a diagram of the integration circuit. This circuit can be constructed from a differential pair of M_1 to M_4 and capacitor C_{s1}. The circuit in Fig.3 must have the property of the temporal summation of inputs, so it must function as the integrator consisting of a resistor and a capacitor.

We examine the characteristics of temporal summation of inputs for the circuit in Fig. 3, where v_g of periodic pulse train is applied to the gate terminal of M_1.

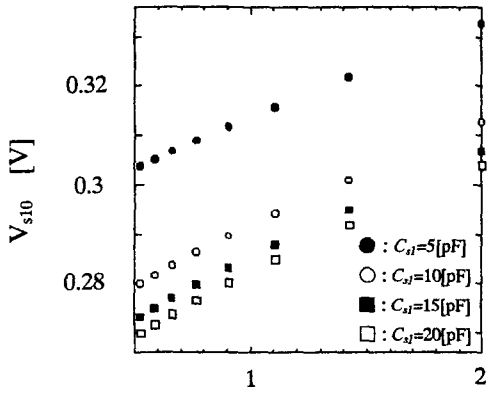
Figure 4 shows an example of the characteristics of temporal summation of inputs. In Fig. 4-(a), V_s indicates the output voltage given by each input pulse, and N_p indicates the number of the input pulse. In Fig. 4-(b), V_{s10} indicates the output voltage given by 10-th input pulse, f_i indicates the input pulse density. The characteristics of temporal summation of inputs were analyzed by PSpice, using circuit parameters in Fig.3, the ratios $(W/L)_1$-$(W/L)_4$ of each enhancement-mode MOSFETs, M_1-M_4, are 1, 5, 5, and 1, V_{dd}=5[V], I_{ss}=15[μA], and pulse amplitude is 2[V]. These figures show that if capacitor C_{s1} is changed from 5[pF] to 20[pF], V_s increases as the number of input pulses although inclinations are differ, and if pulse density f_i is changed, V_{s10} increases although inclinations are differ, too.

Next, we discuss the structure of the circuit that improves the characteristics, which enlarge the dynamic range and use a capacitor of low capacity.

Figure 5 shows a diagram of the temporal summation circuit,



(a)



(b)

Figure 4: The characteristics of circuit in Fig. 3

which has improved characteristics. This circuit is considered as the composition, which added capacitor C_{s2} and enhancement-mode MOSFET of M_5 to the circuit in Fig. 3.

We examine the characteristics of the circuit in Fig. 5, where v_g of periodic pulse train is applied to the gate terminal of M_1. Figure 6 shows an example of the characteristics of the circuit in Fig. 5. The characteristics were analyzed by PSpice, using circuit parameters in Fig.5, the ratios $(W/L)_1$-$(W/L)_5$ of each enhancement-mode MOSFETs, M_1-M_5, are 1, 5, 5, 1, and 5, V_{dd}=5[V], I_{ss}=15[μA], R_L=5[MΩ], C_{s2}=0.5[pF], and pulse amplitude is 2[V]. These figures show that if capacitor C_{s1} is changed from 1.0[pF] to 2.5[pF], V_s and V_{s10} both increase although the inclinations are differ, and the value of C_{s1} is smaller than it is in Fig. 3, and the dynamic range is greater than it is in Fig. 3.

In the above figures, it is shown that it is possible to construct a circuit using CMOS and some capacitors of low

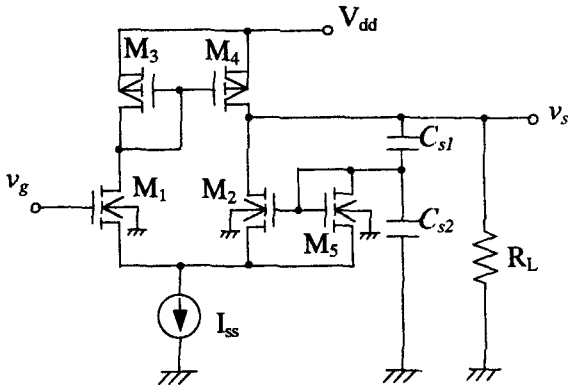
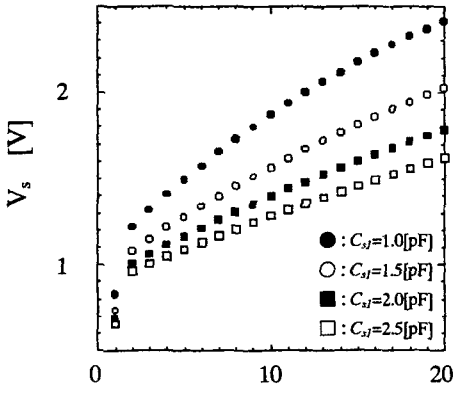
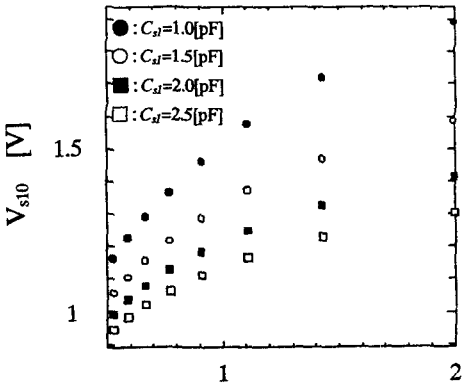


Figure 5: The circuit considering temporal summation of inputs



(a)



(b)

Figure 6: The characteristics of temporal summation of inputs

capacity. So, a synaptic model is composed of the circuit in Fig. 1 and Fig. 5.

3. The Synaptic Model

Figure 7 shows a diagram of the synaptic circuit. Here, MOSFETs of M_6-M_8 are added to connect the synaptic circuit to a cell-body. The current $\gamma\xi_i$ changed as well as v_s, is applied to a cell-body section.

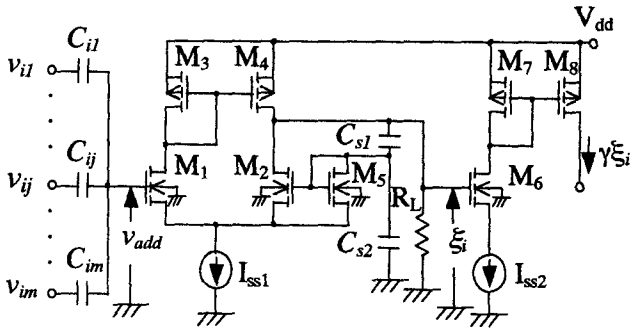


Figure 7: The diagram of the synaptic model

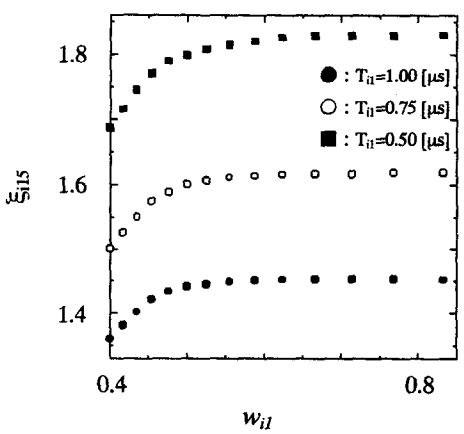


Figure 8: The characteristics of spatial-temporal summation of inputs

We examine the characteristics of the synaptic circuit in Fig. 7, where v_{il} and v_{i2} of periodic pulse train are applied to the input terminal. The characteristics were analyzed by PSpice, using circuit parameters in Fig.7, the ratios $(W/L)_1$-$(W/L)_8$ of each enhancement-mode MOSFETs, M_1-M_8, are 1, 5, 5, 1, 5, 1, 1, and 1, V_{dd}=5[V], I_{ss1}=15[μA], I_{ss2}=15[μA], R_L=5[MΩ], C_{s1}=1.5, C_{s2}=0.5[pF], and pulse amplitude is 2[V]. Figure 8 shows an example of the characteristics of the circuit in Fig.7. In Fig. 8, ξ_{i15} indicates the output voltage given by 10-th input pulse. This figure shows that if weight w_{il} is changed from 0.4 to 0.8, ξ_{i15} increases although the inclinations are differ by pulse densities f_{i1} and f_{i2}. Therefore, this result proves that this circuit has spatio-temporal summation of inputs, which is suitable for CMOS processing.

4. Conclusion

We have discussed the circuit structure of a synaptic section model having the spatio-temporal summation of inputs and utilizing CMOS processing. As a result, we have shown that the synaptic circuit can be constructed using CMOS and several capacitors. In addition, we clarify the characteristics of spatio-temporal summation of inputs of our proposed model. In the future, we shall examine the synaptic circuit of multi-inputs, and the chaotic neural network implemented by P-HCNM.

References

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