Low-Power Receiver Circuit for Wireless Communication System

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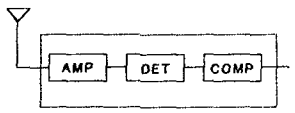
Abstract: In this paper, we propose Low-Power Receiver circuits for a wireless communication system using ASK signal. Their structures are suitable for low supply current. The proposed circuits are designed and simulated by Spectre using 0.8m CMOS process parameters, and operate with supply current below 1.5μA.

1. Introduction

This paper describes Low-Power receiver circuits for a wireless communication system using ASK signal whose constraction is shown in Figure 1.

An opamp is the most important block in analog integrated circuits, which is used in many applications. The architectures of an opamp must be changed by each application, which is presented in [1], [2]. The structure of amplifiers which are suitable for low dc power dissipation and the opamp design that is used in these amplifiers are discussed in Section 3. In Section 4, we propose an AM-detector circuit and a comparator which are able to apply to this system. Finally, simulation results are shown in Section 5.



AMP:Amplifier

DET:Detector

COMP:Comparator

Figure 1. Block of this system

2. Design Specifications

The design specification of this system is shown in Table.1. It is supposed that the power source of this system is a battery just like a micro cell. When the system operates, since the power source is not stabilized, the level of the voltage source is reduced from 3.0[V] to 1.8[V]. The total DC current dissipation of the amplifier and the AM detector are less than 1.5μA, and the current passes of the current sources are not included.

The input signal is shown in Figure 2. That is multiplied the signal wave which is pulse wave at 4kHz with 2mVpp and the carrier wave which is sinusoidal wave at 100kHz. Since the devices which applied this system are used in our life, the temperature range is decided at -40 to 80[℃].

Table 1. The design specifications of system

Supply Voltage	V_{DD}	1.8~3.0[V]
DC suply current	Ic	<1.5[μA]
Signal Frecuency	fs	100[kHz]
Temperature	Ta	-40~80[℃]

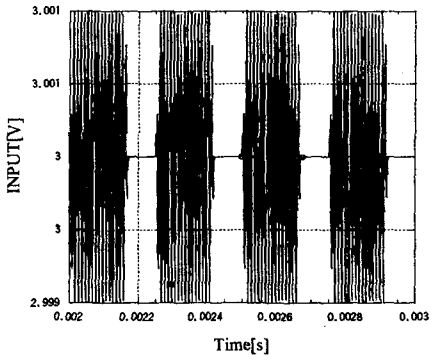


Figure 2. Input ASK signal

3. Amplifier

3.1. Construction of Amplifier

It is demanded that the number of current passes are minimized to operate the amplifier in low power supply. The proposed architecture of the amplifier is shown in Figure 3. This is based on a fundamental positive gain amplifier using two feedback resistors. Although basically construction of the positive gain amplifier consumes much larger DC current, the proposed design does not lose it on account of connecting a capacitor between the feedback resistor R1 and the ground(gnd).

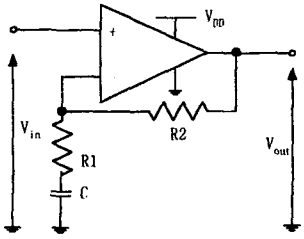


Figure 3. Proposed construction of amplifier

3.2 Opamp Design

As it is already mentioned, reducing DC power dissipation needs to construct the amplifier in minimum current passes. The two-stage opamp is good approach to satisfy the demand.

Two-stage opamps are shown in Figure 4.1. and Figure 4.2. The difference between type N and type P amplifier is the type of transistor of the first and second gain stages. The output stage of the amplifier dose not have ability to drive any road because of the small bias current. In other words, the small bias current causes the reduction of the lower part or upper part of the output signal. So the construction of the output stage must not change.

As for setting up the bias point of type N amplifier, it is difficult to establish the bias point.

For the feedback effect, the output bias point of the type N gives

$$V_O = V_A = V_{DD} - V_{GS_{N3}} \qquad (1)$$

where V_A is the input DC voltage of the input transistor N1. The range of the output bias point to operate all of the transistors in saturation region gives

$$V_O \le V_{DD} - V_{DS(sat)} - V_{GS_{N4}} \qquad (2)$$

$$V_O \ge V_{DS(sat)} + V_{GS_{N2}} \qquad (3)$$

From (2),(3), when the supply voltage changes to minimum supply voltage 1.8[V], we find that the setting of the bias point in saturation region is impossible.

The other amplifier that changes the type of transistor is show in Figure 4.2. Using this circuit, the range of the output bias point gives

$$V_{DS(sat)} \le V_O \le V_{DD} - V_{DS(sat)} - V_{GS_{N5}} \qquad (4)$$

from (4), we have

$$V_{DS(sat)} \le V_{DD} - V_{GS_{N3}} \le V_{DD} - V_{DS(sat)} - V_{GS_{N5}}$$

$$\therefore \quad V_{DS(sat)} + V_{GS_{N5}} \le V_{GS_{N3}} \le V_{DD} - V_{DS(sat)} \qquad (5)$$

Therefore, whenever the output bias point is set up following (5), the amplifier operates in saturation region. In other words, if the gate-source voltage of the transistor N3 that is working for the level shift becomes more large such as in that ranges, it is impossible to set up the bias point to the saturation region.

The way of increasing the voltage is to take advantage of the body effects. The threshold voltage is given by

$$V_{th} = V_{th0} + \gamma\left(\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}\right) \qquad (6)$$

From (6), connecting the bulk to gnd, the source-bulk voltage is generated and the gate-source voltage of N3 becomes large. Therefore, the bias point of the amplifier is set in the range, and the amplifier the operates.

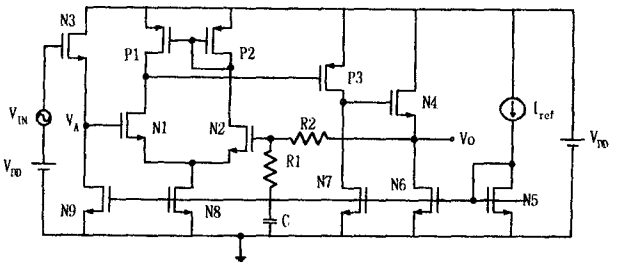


Figure 4.1 Two-stage opamp with buffer (Type N)

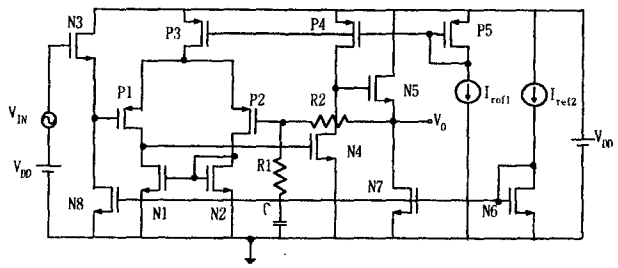


Figure 4.2 Two-stage opamp with buffer (Type P)

3.3 Opamp Compensation

Compensation of an opamp is considered to be one of the most difficult and important parts of the opamp design. Usually, the two-stage opamp should be compensated to have stable operation.

The open-loop gain and phase of the opamp which is not included feedback element is shown in Figure 5. At the unity-gain frequency, this opamp dose not have the phase margin. So the opamp compensation is needed in it.

However ,the amplifier is added feedback element, R1, R2 and capacitor. The loop-gain and phase of the amplifier which are shown in Figure 6. At the unity-gain frequency, the phase margin of this amplifier is over 60° ,which gives stable operation and argue that this amplifier dose not need opamp compensation.

4. AM Detector Circuit and Comparator

We propose the AM detector circuit which is suitable for the low-power system is shown in Figure 7. The envelope detection circuit is constructed with transistor N1, bias current I_{REF1}, and capacitor C_{det}. Resistor $R_{LPF1,2}$ and capacitor $C_{LPF1,2}$ consist of the low-pass filter(LPF). Although N1 and I_{REF1} operate as a level shift circuit, connected capacitor C_{det} the source follower N1 and current source I_{REF1} , it operates as an envelope detection circuit.

An AM detector circuit is typically consisted of a half-wave rectification circuit using a diode and a low-pass filter. An opamp can be used in the half-wave rectification circuit in order to approximate to an ideal diode. They are not suitable for the low-power system because it increases the DC power dissipation much more, and the DC supply voltage change

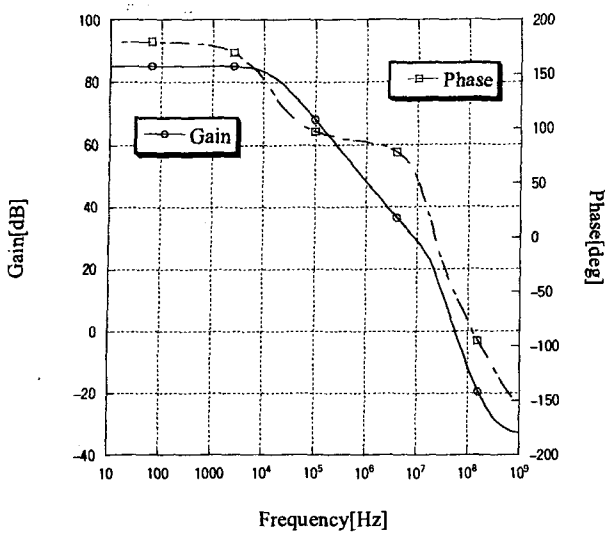


Figure 5. open-loop gain of Opamp

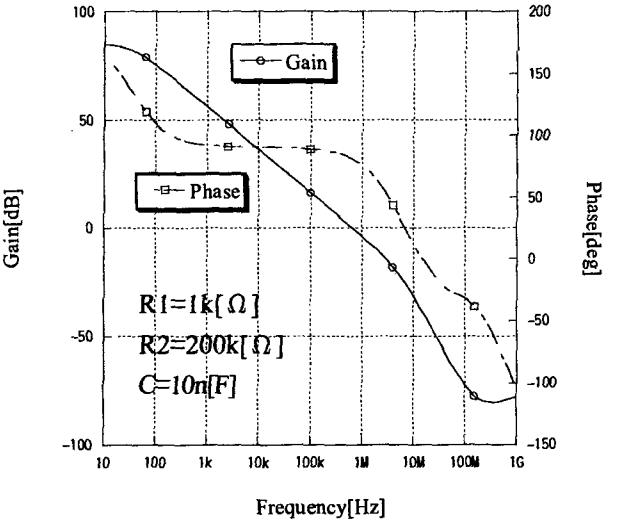


Figure 6. open-loop gain of Amplifier

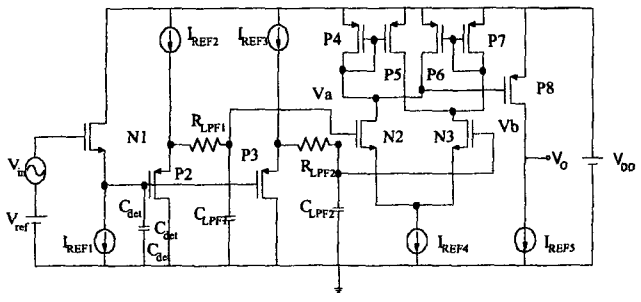


Figure 7. Proposed AM detector circuit and Comparator

influences to the operation.

The advantage of this circuit is that DC supply current is reduced, and the size of capacitor becomes small by the supply current. The problem of influencing by the DC supply voltage change is solved because DC supply current is decided by current sources I_{REF1} and I_{REF2}.

In the design of a comparator which uses in this system, the most important problem is the fluctuation the supply voltage. When the supply voltage is changed, the comparator which is needed reference voltage can not operate correctly. Because the bias points of this circuit are changed by the supply voltage.

The transistor P4, P5, P6,P7,P8,N2, N3, and N4 consist of the hysteresis comparator[3]. As this comparator make use of the difference of the time constant , it is not need reference voltage. The time constant of the input signals decided by the LPF of the detector circuit, resistor and capacitor.Using the hysteresis comparator, the influence of signal noise is removed near the crossing point of input signal.The width of hysteresis, V_{hys}, is defined as

$$V_{hys} = \left| \frac{1-\alpha}{1+\alpha} \sqrt{\frac{I_{REF4}}{K}} \right| = \left| \frac{1-\alpha}{1+\alpha} \sqrt{\frac{I_{REF4}}{K_o}} \left(\frac{W_{N2}}{L_{N2}} \right)^{-\frac{1}{2}} \right| \quad (7)$$

$$\alpha = \frac{W_{P4}/L_{P4}}{W_{P6}/L_{P6}} \quad (8)$$

5. Simulation Results

The proposed Low-Power Receiver circuit shown in Figure 8 are simulated by Spectre using 0.8μ CMOS process parameters. Then the total DC current dissipation of this circuit is 1.3[μA].

The frequency responses of this amplifier when the supply voltage change from 1.8[V] to 3.0[V] are shown in Figure 9. From this result, the proposed circuit can operate when the supply voltage changes.

The transient responses shown in Figure 10 and in Figure 11, when the signal which is shown in Figure 2. is inputted this circuit. Figure 10 shows the signal at Va, Vb, and the output signal of the comparator when the supply voltage is 1.8[V].At the same, Figure 11. shows the signal when the supply voltage is 3.0[V].

6. Conclusions

This paper has proposed a Low-Power Receiver circuit which is suitable for low power system. The proposed amplifie is robustwhen the supply voltage and the temperature change.

Besides, since the DC current dissipation of this system below 1.5μA, it is possible to apply to wireless communication system using micro cell.

7. REFERENCES

[1]Paul R.Gray, Robert G.Meyer, *Analysis and Design of ANALOG INTEGRATED CIRCUITS*, John Willey & Sons, Inc.

[2]Satoshi Sakurai, Mohammed Ismail, *LOW-VOLTAGE CMOS OPERATIONAL AMPLIFIERS Theory, Design and Implementation*, Kluwer Academic Publishers.

[3]Hidetoshi Miyazaki, Masao Yanagisawa, Tatsuo Ohtsuki, Eitake Ibaragi, Satoru Shingai, "Design Consideraition of Level Shift Comparator for Logic Interface", The Papers of Technical Meeting on Electronic Circuits, IEE Japan, ECT-02-16, pp-13-16, Feb.2002.

Table.2 Simulation Condition

Transistor	W/L(mm/mm)
M1,M4,M5,M6,M7,M8 M9,M14,M17,M26,M28	2.4/2.4
M2,M27,M29	2.4/6.0
M3,M21	3.6/2.4
M10	4.8.4.8
M11	2.4/7.2
M12	40/1.0
M13	2.4/40.0
M15,M18	2.4/1.2
M19,M20	2.4/4.8
M22,M25	2.4/12.0
M23,M24	2.4/9.6

I_{ref1},I_{ref2}	150[nA]
R1	1k[Ω]
R2	100k[Ω]
C_{det}	6p[F]
C_{LPF1}	10p[F]
C_{LPF2}	50p[F]
R_{LPF1},R_{LPF2}	500k[Ω]

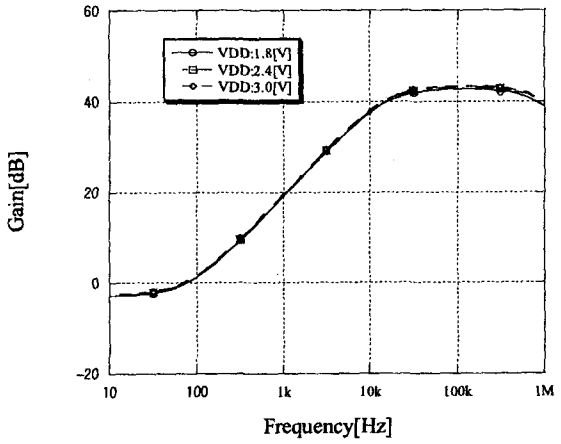


Figure 9. Frequency response of Amplifier

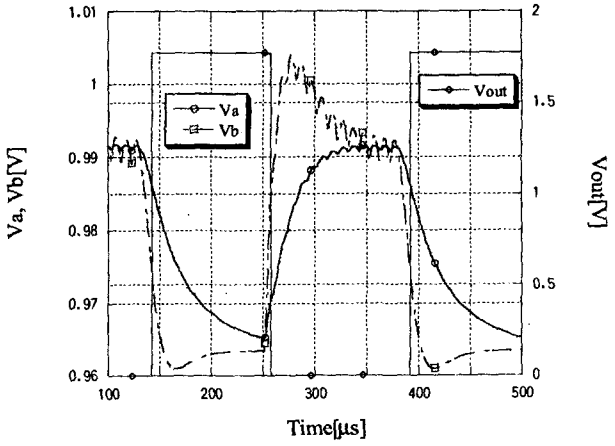


Figure 10. Transient response

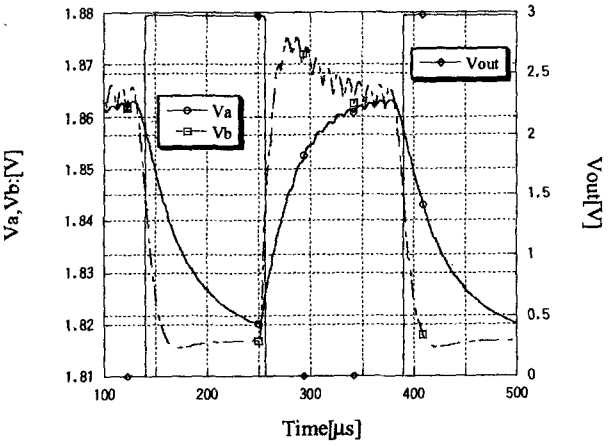


Figure 11. Transient response

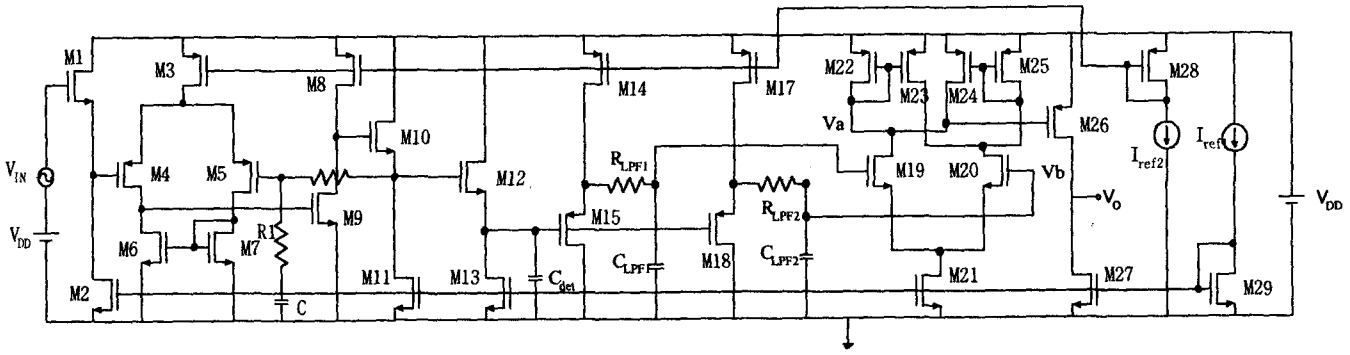


Figure 8. Low-Power receiver circuit