A Design of a Circular Pattern Recognition Circuit for a Binary Image with Variable Resolutions and Its FPGA Implementation

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Abstract: A fast algorithm for a circular pattern recognition from a binary edge image is proposed in this paper. The implementation of this algorithm onto an FPGA is designed using Verilog-HDL where a target device is Altera EPF10K100ARC240-3. For a 256 x 256-pixel binary edge image assuming a real watermelon in a greenhouse, improved circuit performance of the proposed design was confirmed.

1. Introduction

Automation of agriculture can provide farmers with modern tools to enhance productivity and to save manpower. Especially, an intelligent vision robot for harvesting crops automatically is a promising tool to assist farmers' work. An on-chip vision system for such a kind of agro-robot is required to be compact and to be capable of doing real-time processing.

Our group has already developed an on-chip vision system for a watermelon harvesting robot to be used in a watermelon greenhouse. This vision system consists of two major blocks. One is a recognition block which recognizes a watermelon in a binary image. The other is an image preprocessing block which finishes an input image such that it can meet the requirement of the post-stage circular pattern recognition block. The image preprocessing block performs the following operations: 1) conversion of a color image to a binary image 2) stationary edge detection and 3) noise reduction.

Watermelons are usually camouflaged by same-colored leaves and stalks. Therefore, detection of a watermelon in a greenhouse is a difficult problem for a robot. For pattern recognition, various methods have already been proposed in the past, such as neural networks[1], fuzzy clustering[2], and pattern classifier algorithms. However, most of these methods are not compatible with system-on-chip implementation and real-time requirements since they involve a heavy computational load and a considerably large amount of hardware.

In an agricultural environment, a robot vision system has to be customized to different environment. In this meaning, FPGA(Field Programmable Gate Array) implementation is an economical solution which satisfies both flexibility requirements, customization requirements, and real-time requirements.

In harvesting a watermelon, a robot has to do soft-handling. This requires precise information, namely high-resolution images. However, high resolution image processing generally takes long computational time.

In this paper, a real-time circular pattern recognition circuit and its interface block in a 256 x 256-pixel binary image is proposed. The proposed algorithm has the advantage in speed as compared to the histogram method [3] reported in the past. This algorithm performs image coarsening to create a 1/4-resolution image. The recognition principle of this algorithm is based on the method in [3] combined with a global search of the COC(center of a circle) performed with coarse resolution followed by a local precise search of the COC performed with fine resolution. The proposed algorithm consists of three-step image coarsening, one global search and three local searches of the COC. The global search with coarse resolution can effectively reduce the regions for a search with fine resolution so that the computation time can be reduced by a large amount while increase of the hardware cost is small.

2. Proposed algorithm

At first, the principle of the proposed circular pattern recognition algorithm is explained in section **2.1** and **2.2**.

2.1 Generation of Histograms

We regard any pixel in $2^{m+5} \times 2^{m+5}$-pixel ($0 \leq m \leq 3$) binary image as the center of a circle (call this point as the CCOC(candidate of the center of a circle). Then, by counting the number of black pixels n_r at the discrete Euclid distance r from the CCOC, a histogram with respect to r and n_r is obtained. By displacing the position of the CCOC in the image, similar histograms are also obtained.

The r is defined as follows. We segment the input image to 32 x 32-pixel regions. We express the coordinates of the region in the image as (X, Y) and black pixel's global coordinates in the image as $(\hat{x}, \hat{y})$ while the pixel's local coordinate in a 32 x 32-pixel region as (x, y). Then, the following equations are obtained.

$$r = [\sqrt{(p-\hat{x})^2 + (q-\hat{y})^2} + 0.5] \quad (1)$$

$[\cdot]$: Gauss' symbol.

where

$$(\hat{x}, \hat{y}) = (32X + x, 32Y + y) \quad (2)$$

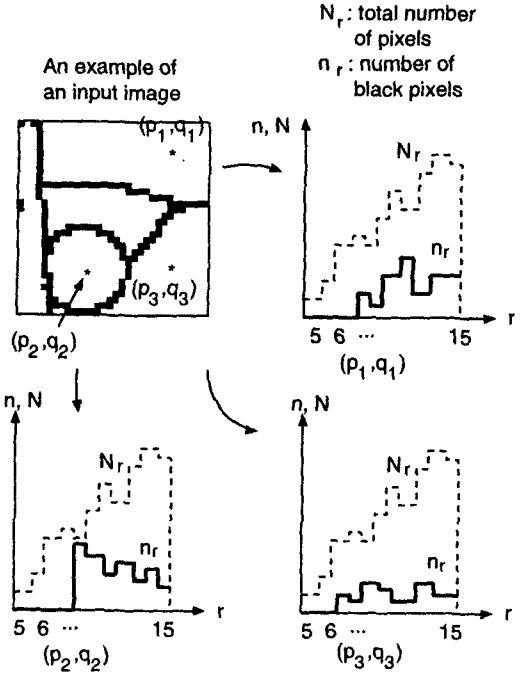

Fig.1 Generation of histograms from an image.

2.2 Calculation of Matching Degree

Matching degree to a circle $MDC_r|_{(p,q)}$ of the set of black pixels at the radius r from the CCOC (p, q) is defined as follows.

$$MDC_r|_{(p,q)} \triangleq \frac{n_r|_{(p,q)}}{N_r} \quad (3)$$

where

$n_r|_{(p,q)}$: total number of pixels
N_r : number of black pixels

Then, the maximum matching degree to a circle, MDC, by the set of black pixels in the image is determined as follows.

$$MDC \triangleq \max_{p,q}\{\max_{r}\{MDC_r|_{(p,q)}\}\} \quad (4)$$

$\max\{\cdot\}$: maximum operation

Circular pattern is recognized from the center (p, q) and the radius r in equation (4).

2.3 Image Coarsening

To realize fast processing, the following coarsening process is adopted.

Step1

We cover a $2^{m+5} \times 2^{m+5}$-pixel binary image by 2×2-pixel regions such that the regions will not overlap.

Step2

If there are at least one black pixel in each 4 pixels, then we output one black pixel. Else, output one white pixel.

Following this process, we obtain a new $2^{m+4} \times 2^{m+4}$-pixel image with 1/4 resolution to the original image.

2.4 Fast Circular Pattern Recognition Algorithm

In this section, the whole algorithm using the method in **2.3** is shown. Here, the input image is a 256×256-pixel(say $m = 3$ in **2.3**) binary image.

Step1

If $m = 0$, go step4, else go step2.

Step2

Create a coarsened image by using the method proposed in 2.1.

Step3

Substitute $m \leftarrow m - 1$. If $m \geq 1$, go step1, else go step4.

Step4

Regard every pixel in the image as the CCOC and generate respective histograms.

Step5

Calculate MDC in each histogram. If $MDC \geq 0.5$, we regard the (p, q) and r as the COC and the radius of the recognizad circle, respectively, under this resolution. And if $m = 3$, output the current (p, q)- and r-values and finish the recognition process, else go step 6.

Step6

Substitute $m \leftarrow m + 1$. Generate histograms over the region consisting of $(2p, 2q)$ and its 8 neighbors where (p, q) is the coordinate (p, q) given by step 5. And go step 5.

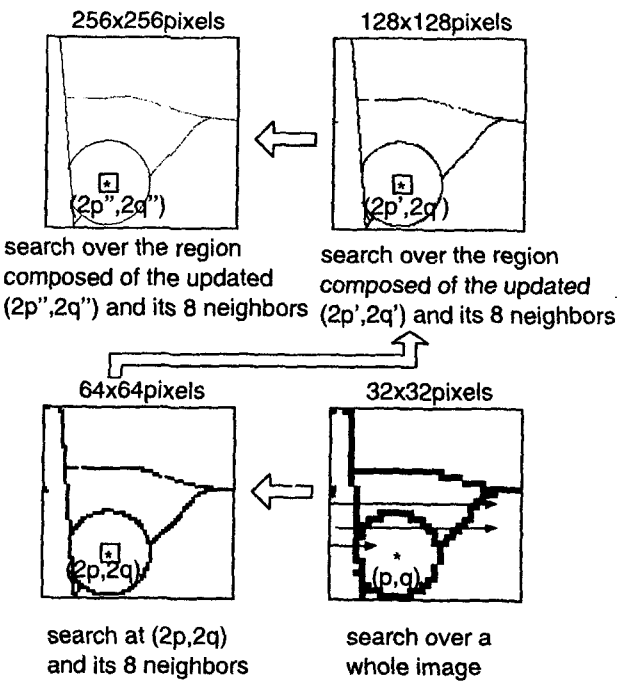

Fig.2 Search region of CCOC.

3. Multipurpose FPGA Board

The multipurpose FPGA board contains Altera's FPGA EPF10K100ARC240-3 and can be connected to a PC via PCI bus controller PCI9052. The board can also implement in its socket two SRAMs as external memory of FPGA. In this paper, two SRAMs whose access time is 7.5ns is implemented. The clock frequency of the PCI bus is 33MHz and the maximum clock frequency of this board is 40MHz.

4. Circuit Architecture

The whole architecture of the proposed circuit is shown in Fig.3. The proposed circuit is configured assuming as follows.

1 Default value of the SRAMs is wrote from the PC via PCI bus.

2 The output of the circular pattern recognition circuit is observed via PCI bus, which does not interfere the access between an FPGA and SRAMs.

The clock frequency of proposed circuit is 16.5MHz which is determined considering maximum path delay and PCI bus clock 33MHz. Looking at FPGA from PCI9052, FPGA looks like a memory shown in Fig.4. If PCI9052 access to the address 13843 or 13844, the FPGA returns the value 1111'h(in hexadecimal expression) or 2222'h, respectively, which means executing of both reset and enable of the circuit.

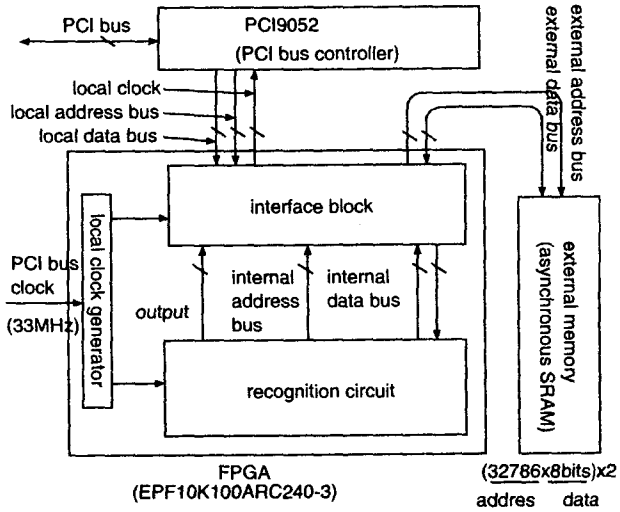

Fig.3 Whole architecture of the proposed circuit.

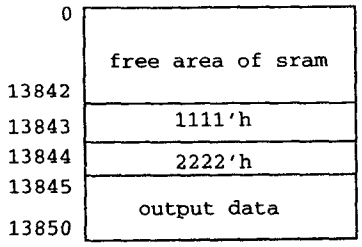

Fig.4 FPGA seen from PCI9052.

Circuit architecture of the recognition circuit is shown in fig.5. This block consists of three sub modules and its controller block.

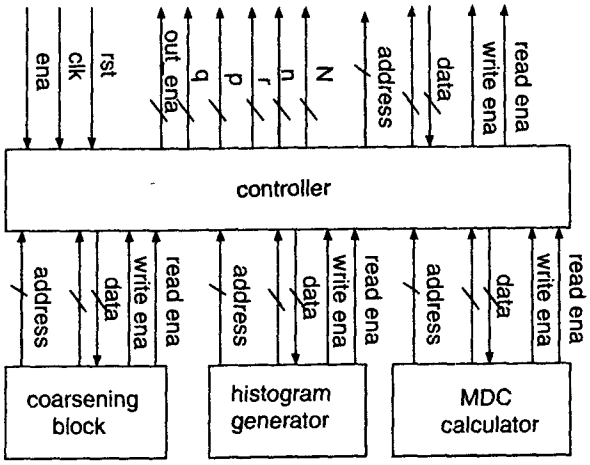

Fig.5 Architecture of recognition circuit.

Circuit architecture of the interface block is shown in Fig.6. This block is connected to three blocks; recognition block, two SRAMs and slave PCI bus controller PCI9052. SRAMs are used as external memories of the FPGA and has 15-bit address bus and 8-bit data bus. This block mainly consists of two selectors and behaves as follows.

4.1 Reset and Enable of Recognition Circuit

1 PCI9052 makes an access to the address which is assigned to reset(rst) and enable(ena)(expressed as rst/ena), respectively.

2 The rst/ena signal is output to the recognition circuit using the address decoder.

3 If the output rst/ena signal is completed, output the value 1111'h or 2222'h to PCI9052 via selector 1.

4.2 Access to SRAMs

If access is required from PCI9052 or recognition circuit, the interface block connects SRAMs and PCI9052 or the recognition block using selector 2.

4.3 Monitoring of Recognition Circuit

If PCI9052 makes an access to the output address in Fig.4, the output of the recognition circuit is observed by the PC via selector 1.

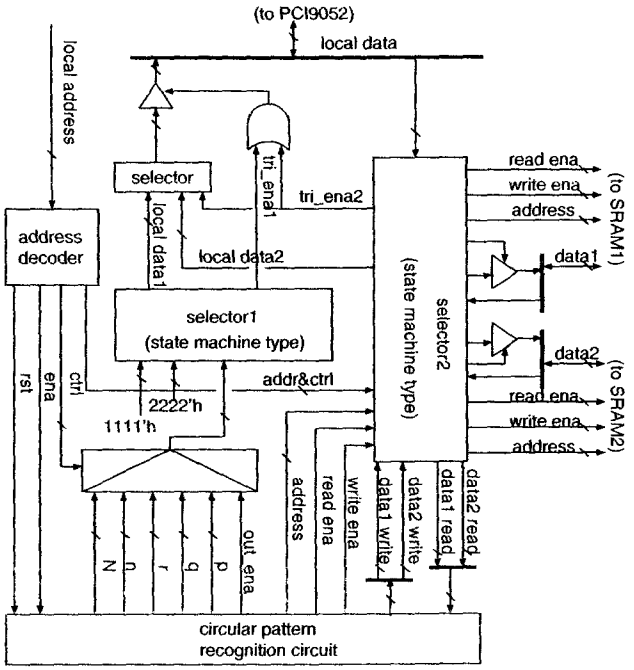

Fig.6 Architecture of interface block.

5. Verification and Implementation to FPGA

The proposed circuit is designed using hardware description language Verilog-HDL for a target FPGA, Altera EPF10K100ARC240-3, and its performance is evaluated by using an input image given in Fig.7(a). Under the same condition as the previous circuit[3], Verilog simulations confirmed that the proposed circuit without the interface block, has achieved about 1000 times faster speed in this design than in the previous design. Table.1 shows the performance comparison between the proposed circuit with/without the interface block and the previous design[3], where processing speed is calculated under 16.5MHz clock frequency. As Table 1 shows, both proposed circuits show the same recognition result as the previous design regarding the input image in Fig.7(a).

The circuit performance is evaluated with a logic synthesis tool Leonardo Spectrum and with integrated hardware description CAD tool MAX+plusII(see Table 2). The proposed circuit is implemented to EPF10K100ARC240-3.

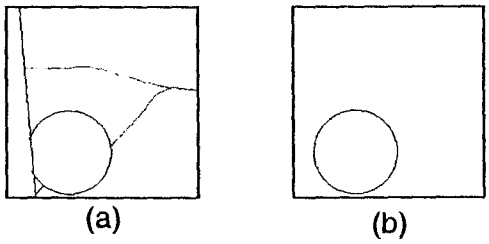

Fig.7 Input image and recognized circular pattern (256 x 256-pixel).

Table 1 Recognition result of the proposed circuit.

	Proposed design with interface block	Proposed design without interface block	Previous design
(p,q)	(195,172)	(195,172)	(195,172)
r	56	56	56
processing steps	21,672,490	9,326,045	* 13,270,109,688
processing speed	1.35s	384ms	359.6s

* means estimated value

Table 2 Evaluation of the performance of the proposed circuit.

	Proposed design with interface block	Previous design
maximum path delay	35.35ns	35.50ns
maximum clock frequency	28.3MHz	28.2MHz
number of logic cells (LCs)	2326(46%)	1316(26%)
number of EAB*	0(0%)	0(0%)

*EAB(Embedded Array Block): 8bit x 256 RAM can construct with this block

6. Conclusions

In this paper, a fast circular pattern recognition algorithm is proposed and designed with Verilog-HDL together with its interface block. For a 256 x 256-pixel binary image which is modeled after a watermelon in a greenhouse, the processing speed of the proposed design without interface block was 1.35ns at a 16.5MHz clock, which is about 1000 times faster than that of the previous design using one kind of resolution.

References

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