A Design of Multiple-Valued Logic Circuits Using Neuron Mos Transister

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Abstract ; The performance of the LSI improved drastically due to the progress of the semiconductor manufacturing technology in recent years. However, a new problem such as wiring delay and complication inside the LSI occurs. The study to solve these problems with much reserch organization is been doing.
We tried to solve of these problems by using the neuron MOS transistor with 4-valued signal in addition to the binary signal.
In this paper, We present method which realizes 4-valued logic function. And, a designed circuit is verified by using HSPICE.

1. Introduction

Since when an integrated circuit was developed, improvement of integration level has generating a high performance circuit.

However, the number of transistors has increased drastically according to the progress of the semiconductor manufacturing technology in recent years. And, the complication of the entailed design and wiring delay are causing a very severe problem.

It is considering that multiple value logic is effective for the solution of these problems.
The density of the information rises by using multiple value logic, and the decrease of the number of elements and the number of wiring can be expected.

We design 4-valued add-subtracter by using a neuron MOS transistor, and the design method for 4-valued logic function is examined

2. Neuron Mos Transister

The neuron MOS transistor consists of electrical floating gates of which each input is capacitively coupled to floating gate. The ON and OFF operation of the neuron MOS transistor is controlled by whether the floating gate potential is high or not than the threshold value of the transistor. The electrical potential Φ_F of the floating gate is described by

$$\phi_F = \frac{C_1V_1 + C_2V_2 + \cdots\cdots C_nV_n}{C_0 + C_1 + C_2 + \cdots C_n}.$$

C_0 is the capacitive coupling coefficient between the floating gate and the substrate.

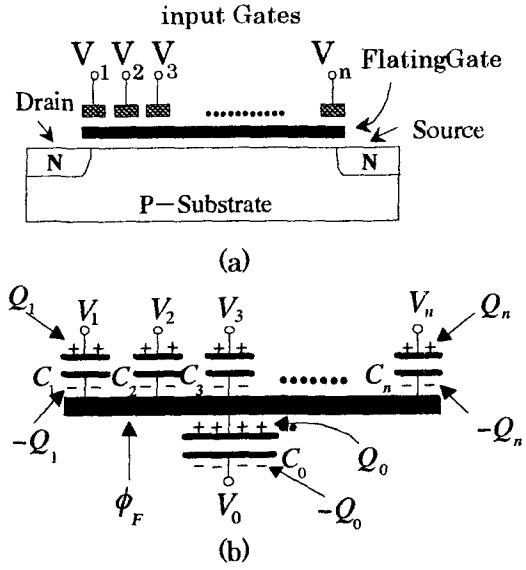

Fig.1. Neuron MOS transistor: (a) basic construction; (b) relationship among terminal voltages and capacitance coupling coefficients.

3. Multiple-Valued Logic

Multiple-valued logic uses multiple-valued signals, such as 4-valued signal, in addition to digital signal.

The input of the neuron MOS transistor cares about neither the digital signal nor the analog signal. But, an output signal is the digital signal of 0 and 1. Because of this, it can't be used as a basic element of the multiple value logic.

However, it can get floating gate potential by composing source follower circuit of the neuron MOS transistor as an output. It can be said more than these that it is the device multiple value signals are easy to handle about the neuron MOS transistor. Because the density of the signal increases by using multiple value signals, the decrease of the number of wiring inside the LSI can be expected.

4. 4-Valued Combinational Circuit

Table.1 is contained the pattern numbers of the logic function of 1 output of 1 input, 1 output of 2 inputs.

	Two binary numbers	Four binary numbers
1 input, 1 output	4	16
2 input, 1 output	256	4^{16}

Table.1 the logic function

It can be understood from this table that the patterns of the logic function are increasing sensationally by the expansion from 2 value to 4 value. As like this, the degree of freedom how to select basic elements becomes large in a many value logic circuit. The design method has not been established for multi-valued logic, although various algebra systems have been proposed. Also, the elements of the analogue circuit are included to the realization of the algebra system that was proposed in the past and act with the current mode. There is not enough practicality from the reason that present CMOS transistor by binary system is developed. Thereupon, we think that information density can be increased without damaging the advantage, by expanding a conventional binary system to 4-value. Then, we grope the realization method.

First of all, we disassemble the 4-value truth table to the 3 layers. Next, for each layer, sub-truth table is taken the algebraic sum of each signal by using a ν MOS source follower circuit, and sub-truth table is composed. The circuit is generated on the final step. By doing so, we develop the method that the signals of 4 values is generated. The method is explained below.

4.1 Generation of the Sub-truth Table

We express the method that the 4-value truth table of the Fig.2 is disassembled in the sub-truth table of Fig.3(a),(b),(c). It is a very important part in the design because the possibility of the circuit scale depends on the disassemble method of the 4-value truth table.

X2 \ X1	0	1	2	3
0	3	0	2	3
1	1	1	3	0
2	0	3	1	2
3	2	3	2	1

The 4-value truth table

Fig.2 The 4-value truth table for a 4-value logic function.

The place where "3" is included in the 4-value truth table (Fig.2) in the case of (a) is indispensable and can also transfer to the same place of (b), (c). Furthermore disassembling (a), (a-1) (a-2) (a-3) are made. (X1, X2) = (0, 1), (X1, X2) = (1, 1) that is not selected here is moved in other the sub-truth tables. They are moved to the same place of the sub-truth table (b), although the movement place is optional. At this time, it is transferred to the same place of the sub-truth table (c), in the case of that "1" is included in the same place of the sub-truth table (b). However, the sub-truth table becomes the condition1 of the Fig.4 because both of them can insert to (b) in this time. For (b), the place where

"3" is contained in the sub-truth table become indispensable clause and also is included in the 4-value truth table and it must be selected without fail with (b) because it becomes an indispensable clause, if there is the 1's place that is not selected with (a). However, it does not exist in this example.

As like (a), by disassembling (b) to select the it's pattern, (b-1),(b-2),(b-3) are made. The place where it is not selected here is moved in the sub-truth table (c). At this time, the sub-truth table (b),(c) becomes the condition 2 of Fig.4. All the clause in (c) become an indispensable clause. By disassembling (c), (c-1),(c-2),(c-3) are obtained.

Doing the aforementioned operation, sub-truth tables of (a-1),(a-2),(a-3),(b-1), (b-2),(b-3),(c-1),(c-2),(c-3) are generated finally.

	0	1	2	3
0	1	0	1	1
1	1	1	1	0
2	0	1	1	1
3	1	1	1	1

(a)

	0	1	2	3
0	1	0	1	1
1	0	0	1	0
2	0	1	0	1
3	1	1	1	0

(b)

	0	1	2	3
0	1	0	0	1
1	0	0	1	0
2	0	1	0	0
3	0	1	0	0

(c)

Fig.3 The sub-truth table for a 4-value logic function.

4.2 Realization of the sub truth table

Furthermore, AND of those output are taken by using the converter that input 0123 is converted to output 0010 and the converter that input 0123 is converted to output 0001. As the reason of this deed, the operations of AND, OR, XOR, can not be selected in the sub-truth table which is not disassembled yet. Regarding Fig.4 (a-2), (a-3), (a-4) similarly, AND of each output is taken. In this way, doing the same procedure regarding sub-truth table Fig.3 (b), (c), the output OUTb and OUTc are obtained.

	0	1	2	3
0	0	0	1	0
1	0	0	1	0
2	0	0	1	0
3	1	1	1	1

(a-1)

	0	1	2	3
0	1	0	0	1
1	0	0	0	0
2	0	0	0	0
3	0	0	0	0

(a-2)

	0	1	2	3
0	0	0	0	0
1	0	0	0	0
2	0	1	0	1
3	0	0	0	0

(a-3)

	0	1	2	3
0	1	0	1	1
1	1	1	1	0
2	0	1	0	1
3	1	1	1	0

(b)

	0	1	2	3
0	1	0	0	1
1	0	0	1	0
2	0	1	0	0
3	0	1	0	0

(c)

Condition 1

	0	1	2	3
0	1	0	1	0
1	1	0	1	0
2	0	0	0	0
3	1	0	1	0

(b-1)

	0	1	2	3
0	0	0	0	0
1	0	1	0	0
2	0	1	0	0
3	0	1	0	0

(b-2)

	0	1	2	3
0	0	0	0	1
1	0	0	0	0
2	0	0	0	1
3	0	0	0	0

(b-3)

	0	1	2	3
0	1	0	0	1
1	0	0	1	0
2	0	1	0	0
3	0	1	0	0

(c)

Condition 2

	0	1	2	3
0	0	0	0	0
1	0	0	0	0
2	0	1	0	0
3	0	1	0	0

(c-1)

	0	1	2	3
0	1	0	0	1
1	0	0	0	0
2	0	0	0	0
3	0	0	0	0

(c-2)

	0	1	2	3
0	0	0	0	0
1	0	0	1	0
2	0	0	0	0
3	0	0	0	0

(c-3)

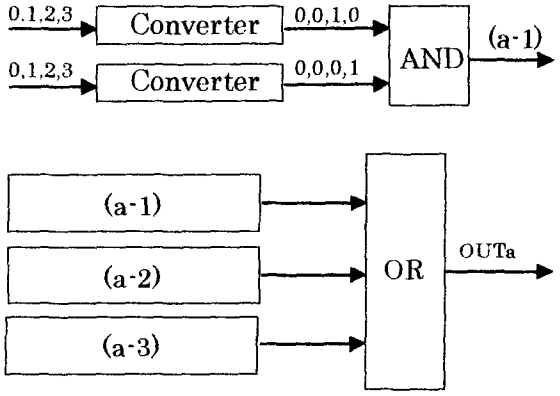

Fig.4 Realization of the sub-truth table

4.3 Generation of 4 value signals

At the last, the output OUTa, OUTb, OUTc of each the sub-truth table are added in the source follower circuit. In this way, the signal of 4-value can be obtained.

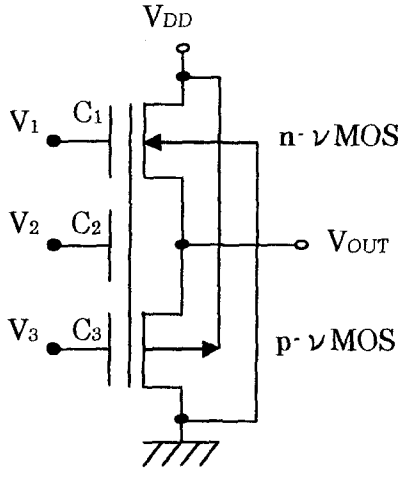

Fig. 5 Source follower circuit by the neuron MOS transistor.

We compare the binary circuit which has the functions equivalent to 4-value circuits that is designed by the above way. Then, the element numbers and element area can be composed of 37.5% and 21.9% of the binary circuit.

5. Conclusions

We have used a neuron MOS transistor for the purpose of the decrease of the number of elements inside the LSI and the number of wiring, and examined the method to realize the design of 4-valued add-subtracter and 4-value combinational circuit.

References

1) T.Shibata and T.Ohmi. "An functional MOS transistor featuring gate-level weighted sum and threshold operations," *IEEE Trans. Electron Devices*, vol.39,no.6, pp. 1444-1455,1992.

2) T.Shibata and T.Ohmi. "Neuron MOS binary-logic integrated circuits:Part I,Design fundamentals and soft-hardware-logic circuit implementation," *IEEE Trans. Electron Devices*, vol.40, no.3,pp.570-576,1993.

3) T.Shibata and T.Ohmi. "Neuron MOS binary-logic integrated circuits:Part II,simplifying techniques of circuit configuration and their practical applications". *IEEE Trans. Electron Devices*, vol.40,no.5,1993.

4) T.Shibata and T.Ohmi. "Neuron MOS voltage-mode circuit technology for multiple-valued logic," *IECE Trans. Electron Devices*, vol.E76-C,no.3 March 1993.