Design and Implementation of a Fully Synthesizable Bluetooth Baseband Module Considering IP Reuse

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Abstract: In this paper, we describe the structure and the test results of a Bluetooth baseband module we have developed. The module has a distributed buffer, i.e. FIFO, for data stream. Bus interface of the module is designed on the basis of interface of microprocessor widely used and the external interface is designed to consider chips connected directly. Since the module performs as many hardware efficient tasks as possible, processing load of microprocessor is very small. It can also be controlled either by software or by hardware for flexibility. The fully synthesizable baseband module was fabricated in a 0.25μm CMOS technology occupying 2.79×2.8mm^2 area. And an FPGA implementation of this module is tested for file and bit-stream transfers between PCs.

1. Introduction

Due to progress in related technologies in the past decades, wireless telecommunication technology has been applied to telephony service, medical instruments, home electronics, and more applications. The existing wire-applications have accepted wireless technology for more convenience of consumers. Especially since ISM (Industrial, Scientific, and Medical) band is the unlicensed band, wireless communication using this band will be increased explosively.

Bluetooth is a specification for short-range wireless communication. The Bluetooth specification [1] was developed to substitute cables connecting portable or desktop devices and build low-cost wireless networks for mobile and portable devices in 1999 by the Bluetooth Special Interest Group (SIG); an industry consortium founded by Ericsson, IBM, Intel, Nokia, and Toshiba. This group was further expanded in Dec. 1999 with 3COM, Lucent, Microsoft, and Motorola. In addition to these nine promoter companies, more than 1800 companies have joined as adaptors [1]. Bluetooth operates in the 2.4 GHz ISM band. It emphasizes low complexity, power consumption, and cost target. Moreover it should have flexibility and very fast integration time for applying to various applications, complying with the above points.

This paper describes a flexible and reusable digital baseband module that is suitable for use as an IP (Intellectual Property) core. The module is the part for performing protocol of physical layer in Bluetooth Device. Bus interface of the module is designed on the basis of 8bit data width and interfaces of related chips are considered for the external interface. These interfaces provide users with easy integration to various Bluetooth systems. We also designed the baseband module to control low-level timing either by hardware or by software (microprocessor) for flexibility and handle bit-stream without distributed buffers between coding blocks by considering the data stream-flow for low power. We performed verification and test to this module for the bit stream process. The module is made up of a logic part of only 85k gates on ASIC. It conforms to the latest version of the Bluetooth.

2. Overall Architecture

In this paper, we have designed a baseband module that consists of link controller, UART (Univeral Asynchronous Receiver Transmitter), USB (Universal Serial Bus), and audio CODEC. The link controller performs the baseband protocol and low-level connection processing. UART and USB are host controller interfaces (HCI) and operate alternatively. Audio CODEC processes voice data. The four units have a distributed buffer, i.e. FIFO, respectively and are connected via a bus interface commonly used to Bluetooth systems as shown in Figure 1. The general-purpose interface supports easy integration of the module to various Bluetooth systems. The baseband module is directly connected to an RF module via RF interface, which is designed on the basis of Ericsson's RF module interface. We also considered the other RF modules. The RF interface signals are controlled by registers, which are set by firmware, of link controller. The control of RF module is performed through serial control interface based on IEEE standard 1149.1 boundary scan architecture. Audio CODEC passes 8-16bit linear PCM signal. Chips connected externally considered like this, our module can be easily applied as an IP to various Bluetooth systems. Moreover each block such as UART, USB, audio CODEC can be use as IP core for ASICs (Application-Specific Integrated Circuits).

In the Bluetooth baseband, link manager and link controller are very important function blocks. Link manager translates command and data into behaviour of baseband level and establishes and controls link among Bluetooth devices. These parts are generally performed by software running on microprocessor. Link controller, which is implemented in dedicated hardware, controls physical link and recombines packets [3], [4]. Thus, trade-off of software and hardware between link manager and link controller is a great important part for flexibility. So we designed the baseband module to perform the complex part of the link controller requiring flexibility, such as decision-making on received baseband packets and context switching between

links, either by software or by hardware. Microprocessor easily can control each peripheral such as baseband unit, UART, USB, and audio CODEC constituting the baseband module by internal register and memory mapped I/O. And the link controller includes baseband unit that is the part to perform bit-level processing by encoding or decoding the bit-stream and control low-level timing. Figure 1 shows overall architecture of the Bluetooth baseband module.

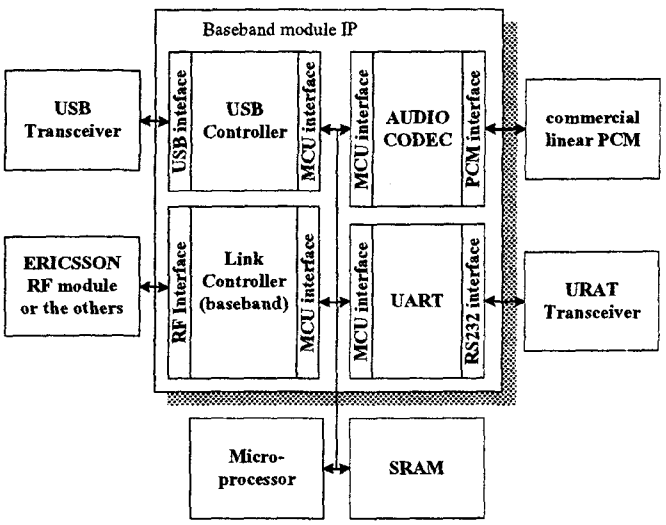

Figure 1. Overall architecture of the Bluetooth baseband module.

2.1 Link Controller

The link controller is designed to perform many hardware efficient tasks, such as low-level timing control, frequency hop calculation, encryption, decryption, access code generation and detection, correlation, Bluetooth clock control, etc., because the baseband functions of Bluetooth are bit-intensive and time-critical. Therefore, it is faster than software in performing access code generation detection and encryption/decryption. Microcontroller can manage all of the baseband unit functions in the link controller, for instance bit-stream processing, interrupt, and encryption, by setting the internal registers of baseband unit since the registers control all those functions. When a critical event occurs in relation to transmission or reception of packets, the link controller calls the microcontroller interrupt, and all the related information can be transferred to the microcontroller via an interrupt register. The link controller has a 128byte buffer block; TX and RX buffer have 64byte respectively. These buffers are used to reduce load of microprocessor and process bit-stream smoothly. The system clock frequency is 12MHz, but the interface with radio module operates at 1MHz clock. As sub-clocks, 3.2KHz and 4MHz clock are used in relation to RF interface. The 3.2KHz is very important for Bluetooth timing control. Transmission is synchronized to the 1MHz provided by RF module, and reception is synchronized to the clock extracted from PLL block of RF interface module. For detection of an expected data packet, the baseband module has to perform periodically synchronization with synchword. So we designed correlator using 64bit synchword. Figure 2 shows the block diagram of the baseband unit.

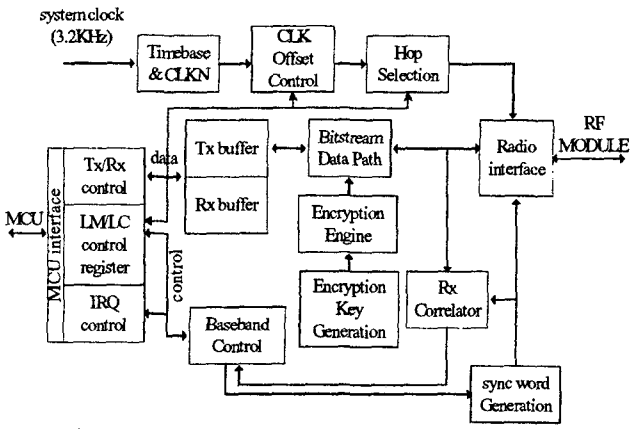

Figure 2. Block diagram of Baseband unit.

2.2 Host Controller Interface

For the data transmission or reception between the Bluetooth baseband module and a host such as PC and mobile or portable device, two serial interfaces, UART and USB, are provided. The UART and USB units constitute the physical layer of Bluetooth HCI. Each of the interface units has an internal FIFO and its size is 64bytes.

The Bluetooth HCI UART transport layer is the most general serial interface between the host and the Bluetooth device. The UART unit is designed on the basis of industry-standard 16C450. It supports baud rates from 300bit/s to 1.5Mbit/s by NCO (Numerical Controlled Oscillator) and the analysis function in relation to HCI command. For this, the UART unit includes a packet decoder that finds the HCI packet type and length of the received packets to help HCI processing of the microcontroller.

The USB unit complies with USB Specification 1.1 [6] and HCI USB transport layer specification of Bluetooth v1.1 [2], and supports full-speed 12Mbit/s interface. USB device controller consists of transceiver interface, serial interface engine, protocol layer handler, registers/endpoint manager, and parallel interface. The transceiver interface block generates output enable signal for the transceiver to drive signal line when sending data, and it contains an RX clock recovery circuit. The serial interface engine encodes, decodes, and samples signals at the recovered clock. Protocol layer handler works as a transaction sequencer, which performs the control to send or receive expected packets. If it receives an unexpected packet, it ignores the packet. When it receives an expected error-free packet, it stores the packet in the corresponding endpoint FIFO and writes related information to registers. Parallel interface and interrupt are provided for data ex-change with memory.

2.3 Audio CODEC

A major application for Bluetooth is as a carrier of audio information. So we designed audio CODEC for processing voice data. Audio data is carried via Synchronous Connection-Oriented (SCO) channels and through the use of several coding schemes. We designed the audio CODEC for user to select and control easily the coding method by

register. Bluetooth specifies three audio coding methods: Log PCM coding using either A-law or μ-law and CVSD (continuous variable slope delta modulation). We implemented all the three coding methods in a hardware audio CODEC and designed the external interface based on a general commercial PCM chip. This CODEC unit has a 64byte buffer block to store voice data. In simple applications, the audio CODEC can access a voice data without control by processor.

2.4 Bluetooth Clock Control

Clock control is one of the most important parts in design of a Bluetooth unit. When two Bluetooth units are to establish a communication channel, the Slave clock and its phase must be synchronized to the Master clock. For this, Baseband unit uses 3.2KHz clock to determine the transmission start time and a 28-bit counter is designed for this. Bluetooth defines and uses three clocks: CLKN, CLKE, and CLK [2], [3], [4]. CLKN, the native clock, is used as the basis of the other clocks. CLKE and CLK, which represent estimated clock and master clock respectively, are obtained by adding offset to CLKN. Channel timing and frequency hopping are dependent of the Master clock. Figure 3 shows block diagram for Bluetooth clock generation.

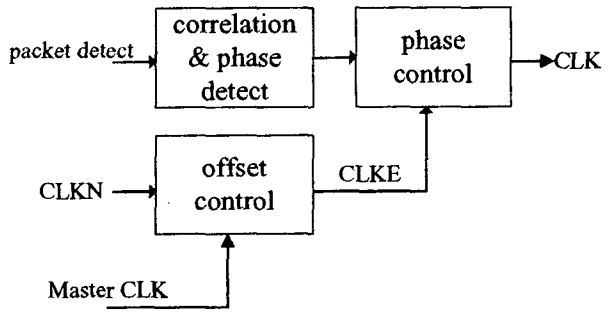

Figure 3. Bluetooth clock generation block.

2.5 Bit-stream Processing

Channel coding of data before transmission through RF channel is essential to protect the data against an imperfect channel. Figure 4 and 5 show the TX and RX bit-stream processing blocks of the proposed link controller (baseband unit), respectively. The blocks are connected so that data can stream through the blocks continuously without any buffers between them. For this, we designed a sequencer that controls timing of each function block, such as HEC, CRC, Whiten, Encryption, FEC, etc., depending on the type of the packet. In addition, the sequencer sends various information produced during processing to the control registers of baseband unit. In terms of error detection, a packet is partitioned into three parts: access code, header for HEC, and payload for CRC [3]. Whitening block randomizes data and minimizes DC bias. It reduces a long sequence of zero or one by mixing data bit-stream and pseudo-random bits [2].

The TX/RX bit-stream processing varies depending on the received packet. At this time, RX processing is different from TX processing. Because we do not know the packet type and length in advance, we must recognize that information during the reception. RX block therefore requires a block that analyzes the form of received data. To perform the task, we designed the payload header analysis block and the header analysis block. They first identify whether a received packet belongs to the Bluetooth device, and then analyze the packet type and the length information of received data.

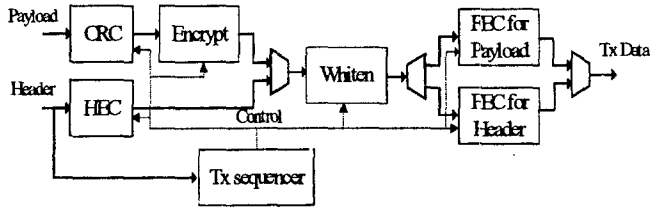

Figure 4. Packet transmission block.

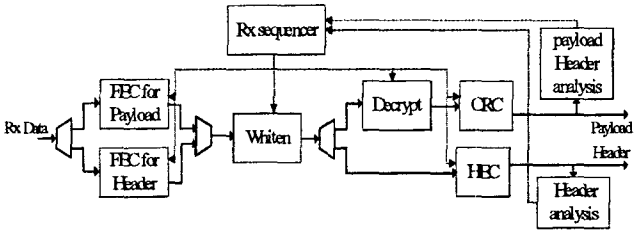

Figure 5. Packet reception block.

3. Implementation and Test of the Baseband Module

We have implemented and tested ASICs and FPGA for this module.

At the FPGA test, we mapped our design into Xilinx 1000K gate virtex chip and implemented a test board. The FPGA has microprocessor, link controller, UART, USB, and audio CODEC in the chip. Test board has the FPGA, flash memory, external RAM, Ericsson RF chip, PBA313 01/2, and antenna. We confirmed and verified the point-to-point connection capability of baseband module with two test boards. Two boards successfully established a connection and transferred bit-streams and files via UART HCI interface.

In parallel with the above FPGA test, we have implemented a prototype chip of the baseband module in a 0.25μm 5metal CMOS technology. The prototype chip has four blocks: the microcontroller, baseband unit, USB, and UART. The audio unit is not included in this version. Figure 6 shows a die microphotograph. All the block of the chip is described in Verilog HDL and fully synthesizable. For implementation, we used a semi-custom method. The chip size is $2.79 \times 2.8 mm^2$ area. The module is made up of a logic part of only 85k gates. The chip is fully tested using IMS ATS2 test station to verify its functionality and timing.

4. Conclusion

The Bluetooth can easily establish a wireless network by only adding the Bluetooth device to a wire device. It supports various applications and protocols. And so it can be widely used in industrial or home fields. In addition, since ISM band is the unlicensed band, we can make the transceiver module for global market. However the

development of small area, high speed, and easy implementation has to be preceded.

In this paper, we developed the fully synthesizable, flexible, and high speed Bluetooth baseband module based on Bluetooth specification 1.1. Since the module has been designed to perform as many hardware efficient tasks as possible, it provides high speed bit-stream processing and low-level timing control. And since the module is a small, fully synthesizable soft core, it can be easily integrated as an IP core on SoC (System-on-a-Chip) ASICs for the applications related to Bluetooth communications. The module is implemented and tested by ASIC and FPGA. For the test of this module, we have made two test boards and tested for file and bit-stream transfers between PCs.

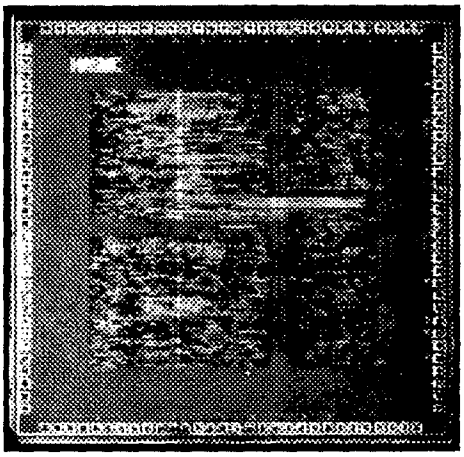

Figure 7. Die Microphotograph of the prototype chip.

Acknowledgement

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