Design of A 1.8-V CMOS Frequency Synthesizer for WCDMA

Young-Mi Lee, Ju-Sang Lee, Ri-A Ju, Bu-Cheol Jang and Sang-Dae Yu
School of Electrical Engineering and Computer Science,
Kyungpook National University,
1370 Sankyuk-dong, Buk-gu, Daegu, Korea
Tel: +82-53-940-8837, Fax: +82-53-950-5505
E-mail : ymlee0210@korea.com, sdyu@bh.knu.ac.kr

Abstract: This research describes the design of a fully integrated fractional-N frequency synthesizer intended for the local oscillator in IMT-2000 system using 0.18-μm CMOS technology and 1.8-V single power supply. The designed fractional-N synthesizer contains following components. Modified charge pump uses active cascode transistors to achieve the high output impedance. A multi-modulus prescaler has modified ECL-like D flip-flop with additional diode-connected transistors for short transient time and high frequency operation. And phase-frequency detector, integrated passive loop filter, LC-tuned VCO having a tuning range from 1.584 to 2.4 GHz at 1.8-V power supply, and higher-order sigma-delta modulator are contained.
Finally, designed frequency synthesizer provides 5 MHz channel spacing with −122.6 dBc/Hz at 1 MHz in the WCDMA band and total output power is 28 mW.

1. Introduction

The recent rapid growth of the wireless communication market inspires many people to research the concerned region with strong passion. Of such a many developments, enhanced operating frequency of CMOS technology encourages the designer to implement single-chip RF-to-baseband systems with it instead of bipolar or GaAs. One of the important design goals of portable wireless systems is low power consumption for long battery life. CMOS technology satisfies the requirements of low power consumption, low cost, reduced size, and also a few GHz operating frequency in wireless systems. Because the dynamic power dissipation of digital CMOS circuits is proportional to the square of supply voltage, the goals can be efficiently achieved by lowering the supply voltage.

IMT-2000 service is a hot issue of such a many wireless systems. The spectrum allocation of IMT-2000 system known as WCDMA or UMTS in Europe is 1920-1980 MHz (up-link) and 2110-2170 MHz (down-link). Frequency synthesizer is one of the basic building blocks in that system. So this research challenges low-power, fully integrated CMOS frequency synthesizer applicable to the WCDMA and also suggests 1.8-V power supply, high speed prescaler with low power consumption while having low switching noise and short transient time.

2. System Architecture

The easiest way to understand the IMT-2000 system is to compare it with present 2nd generation technology. Some of the comparisons about several important parts are listed in Table 1 [8].

Table 1. Specification of 2nd and 3rd generation technology

Classification	2nd generation	3rd generation
Frequency range	800 MHz/ 1.7-1.8 GHz	2 GHz band
Channel BW	1.23 MHz	5-20 MHz
Data rate	Max 64 kbps	14 kbps-2 Mbps
Vocoder	Max 13 kbps	8-32 kbps
Providing service	Voice, slow data	Multimedia
Roaming range	Domestic	Global

We assume WCDMA system based-on the normal heterodyne architecture and consider various specifications, the effects of any other systems, and reasonable Q of channel selecting filter. There are several possible IF Rx/Tx frequencies. One example of them is to select IF Rx/Tx frequency of 350/160 MHz and thus needed local oscillator frequency is 1760-1820 MHz.

The designed frequency synthesizer for WCDMA handset uses fractional-N method. Figure 1 shows the block diagram of the designed frequency synthesizer. It is made up of multi-modulus prescaler with modified ECL-like D flip-flop and a higher-order sigma-delta modulator, which is one of the noise shaping techniques to suppress the fractional spurs occurring at all multiples of the frational frequency resolution offset.

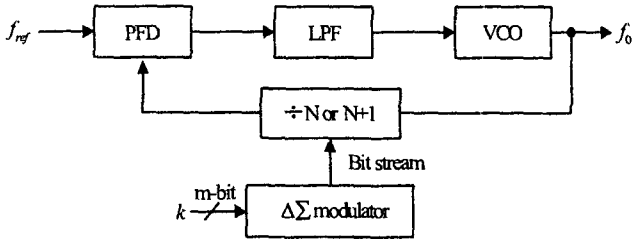


Figure 1. Block diagram of the designed synthesizer

When the PLL is locked, the RF output frequency is

$$f_0 = (N + \frac{k}{2^m}) f_{ref} \quad (1)$$

This architecture allows higher reference frequencies than the channel spacing and considerably reduces the divide ratio N, while using the highest possible reference frequency. The chance of using a highest possible reference frequency also allows wider loop bandwidth and faster switching time. Using a reference frequency higher than the channel spacing can reduce the reference spurs at the output. A noise shaping technique using a high-order sigma-delta

modulator is used to suppress the fractional spurs. This idea is to eliminate the low frequency phase error by rapidly switching the divide ratio between different ratios and to eliminate the gradual phase error at the PFD [1][6].

Let's assume the 20 MHz reference oscillator is used. For 1760-1820 MHz of frequency range and 5 MHz channel spacing above mentioned, the divide ratio N is 88-91, m is 2-bit control signal of the sigma-delta modulator.

3. Synthesizer Building Blocks

3.1 Charge Pump and Loop Filter

In a conventional CP of Figure 2(a), several spikes occur on the output when the currents are switched on and off as switches M1 and M2 are directly connected to the output. These spikes reflect into the output if no proper actions are taken. As these spikes occur at the reference frequency, they will cause spurs in the PLL output spectrum at an offset from the carrier equal to reference frequency.

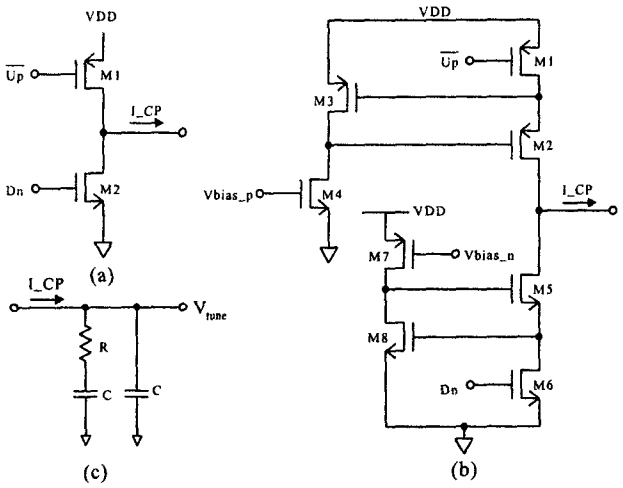


Figure 2. (a) Conventional charge pump (b) Modified charge pump (c) Second-order loop filter

In this design, to reduce the reference frequency spurs problem, we use indirectly connected switches M1 and M6 with output and thus the drain node of M2 and M5 is directly connected to the output which shown in Figure 2(b). The current glitches that now occur at the sources of M2 and M5 when switching M1 and M6 would not be directly conveyed to the output node because M2 and M5 are still off when the glitches occur [4]. Additional transistors are placed to form active cascode, and thus provide high output impedance each time sourcing or sinking. That is, M3 and M4 are the active cascode for M2, similarly M7 and M8 are the active cascode for M5. M4 and M7 relatively acts as current source load for common source amplifier M3 and M8. Figure 3(a) shows each output waveform I_CP when up or dn signal switches M1 or M6 and Figure 3(b) displays voltage compliance of I_CP by up or dn signal. They don't have any kind of spikes and show current matching between I_CPs by up and dn signal.

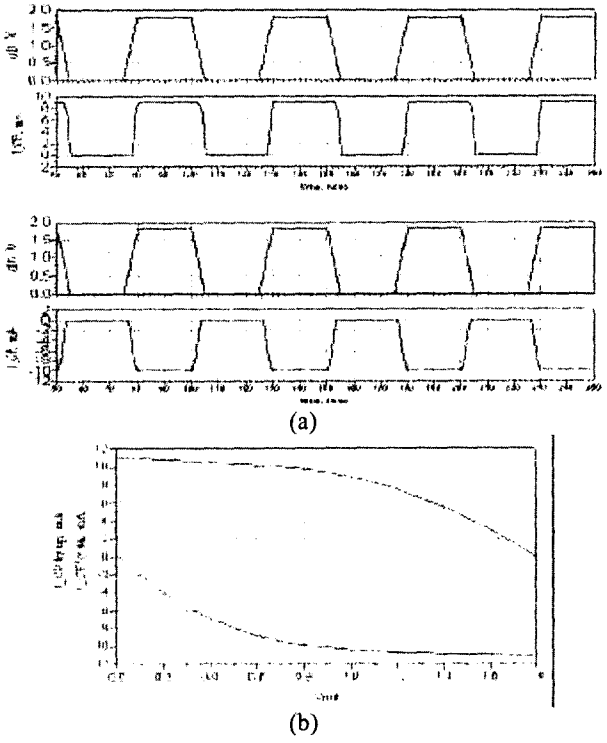


Figure 3. Simulated results of the modified CP

Most of the specifications of PLL will be determined by the loop filter. In this design, a second order low-pass filter shown in Figure 2(c) is employed. In the loop filter, extra poles and zeros can be introduced in the open loop transfer function, which are used to set the noise and transient performance of the PLL [6].

3.2 Prescaler

For prescaler architecture, we employ phase-switching topology. Multi-modulus prescaler is induced from the basic phase-switching prescaler topology. And a suitable block diagram is shown in Figure 4 [6].

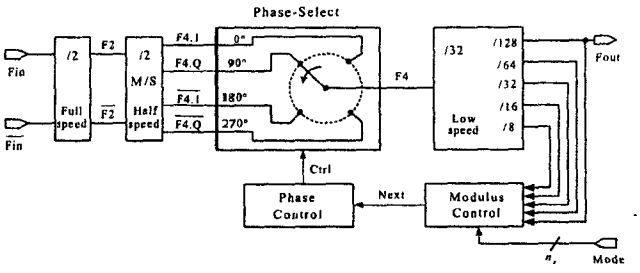


Figure 4. Phase-switching multi-modulus prescaler

Prescaler is one of the critical parts because they operate at the highest frequency. From Figure 5(a) [6], we can see that the D flip-flop of divide-by-two stages is key point for high speed operation and low power consumption.

Schematic of conventional ECL-like D flip-flops is shown in Figure 5(b) [6]. This circuit has low power, low

noise and fast but long transient time about 3 ns at 2 GHz shown as Figure 5(c).

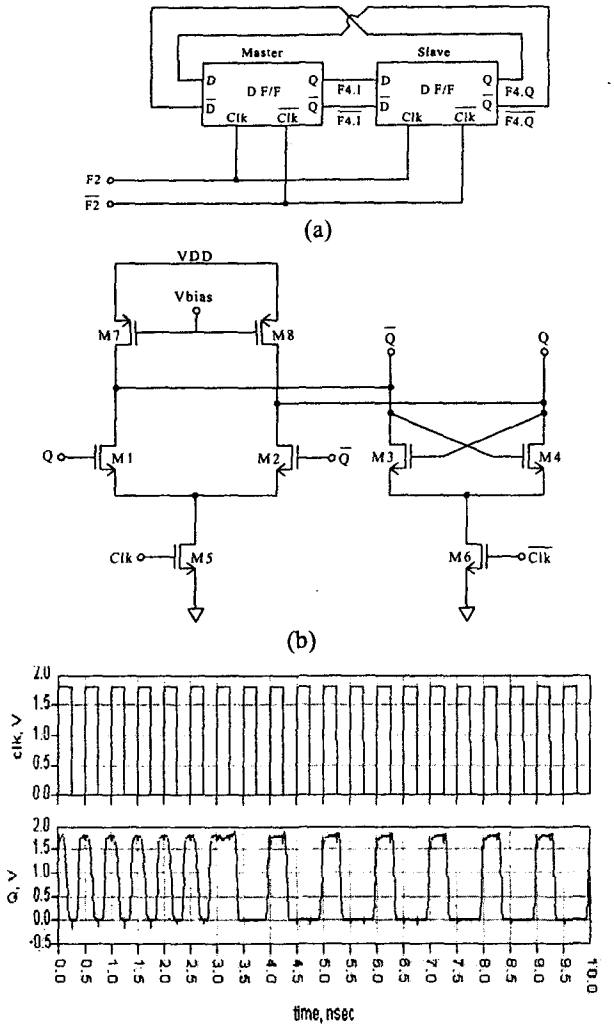


Figure 5. (a) Master/slave divide-by-2 prescaler (b) Conventional ECL-like flip-flop (c) Output waveform of the divide-by-2 prescaler with conventional ECL-like flip-flop

So we add diode-connected transistors, M9 and M10 that is shown Figure 6(a) for short transient time and more high speed operation. These two transistors are turned off during normal operation and have no effect on the D flip-flop and also serve two purposes. One is to increase the slew-rate performance of the D flip flop. However, more importantly, during times of slew-rate limiting, these transistors prevent the drain voltages of M1 and M2 from having large transients where they change from their small-signal voltages to voltages very close to the power supply voltage [5]. Thus the inclusion of M1 and M2 allows the D flip-flop to recover more quickly following a slew-rate condition. Output waveform of divide-by-two prescaler having modified ECL-like D flip-flop is shown Figure 6(b). We know there are reduced transient time of 1 ns at 2 GHz. And divide-by-two presealer with it operates up to 3.6 GHz and consumes 5 mW at 1.8-V power supply.

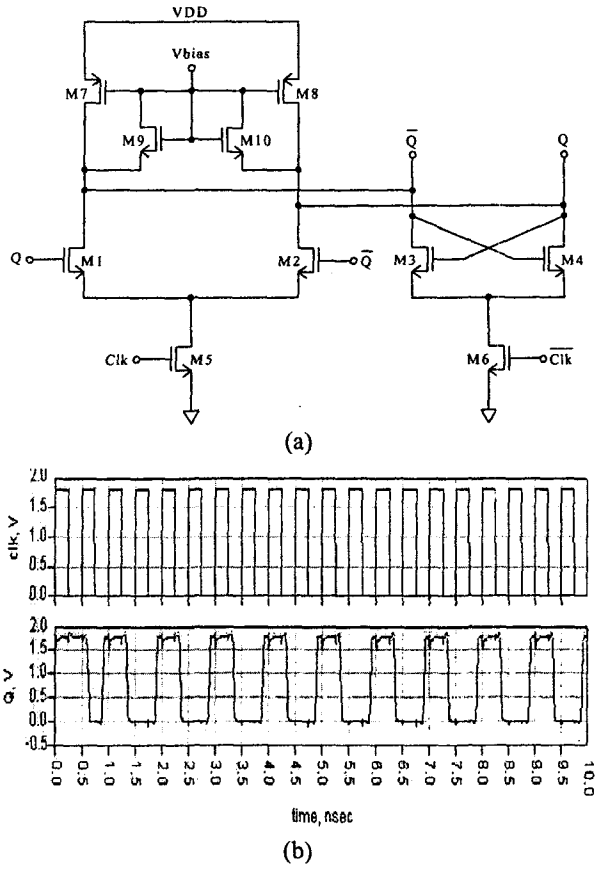


Figure 6. (a) Modified ECL-like D flip-flop for short transient tme (b) Output waveform of divide-by-two prescaler with modified ECL-like D flip-flop

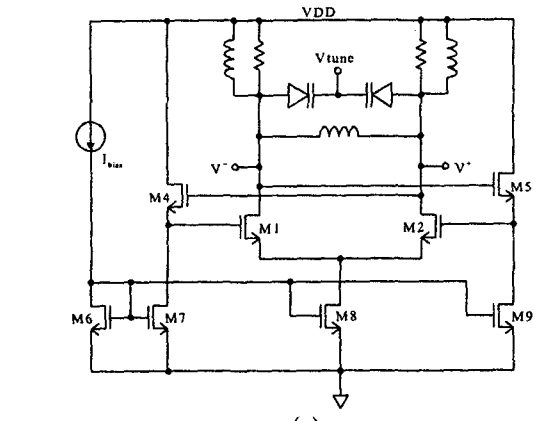
3.3 Phase Frequency Detector

The most important problem of the PFD is the crossover distortion, which changes in gain that occurs near zero phase error. This phenomenon is remedied by giving a fixed minimum width to both the pump pulses. So the proper dead zone free PFD circuit is used [6]. The combinational result of PFD and modified CP has gain of 3.125 mA/rad and no glitch.

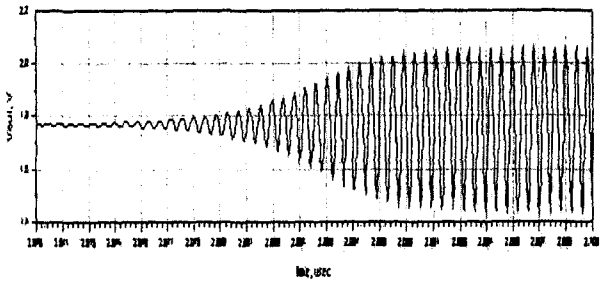
3.4 LC-Tuned VCO

The oscillator circuit schematic, which is ordinarily used cross-coupled NMOS pair, is shown in Figure 8 [7]. Transistors M1 and M2 form a positive feedback loop to provide negative resistances to compensate the loss in the LC tanks.

The LC tanks of the VCO are formed using a ~5.6-nH circular shape of spiral inductor having center hole 100 μm, metal width 12 μm, metal space 1.4 μm, turn 5, and 2-pF pn varactor. The resultant VCO has a tuning range of 1.584-2.4 GHz, phase noise of −122.6 dBc/Hz at 1 MHz offset, average tuning sensitivity of 480 MHz/V, and power consumption of 7 mW.



(a)

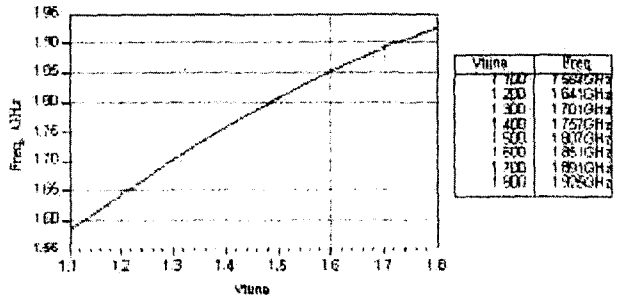


(b)

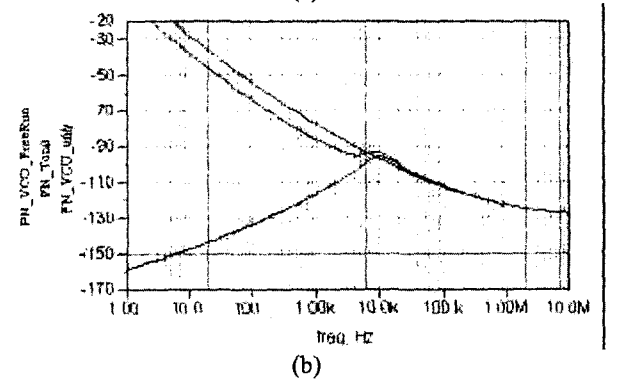
Figure 8. (a) VCO of ordinarily used cross-coupled NMOS pair (b) Simulated results for Vtune of 1.5-V

3.5 Frequency Synthesizer

Each designed component is combined with proper control logic and additional circuitry. And its simulation results are plotted in Figure 9.



(a)



(b)

Figure 9. Simulation results of the frequency synthesizer

Figure 9(a) displays a tuning range from 1.584 to 1.925 GHz as control voltage Vtune varies from 1.1-V to 1.8-V. We saw designed VCO has a tuning form 1.584 to 2.4 GHz. In here, however, tuning range is decreased due to reduced 1.8-V power supply. Although frequency synthesizer has reduced tuning range than VCO has, it has no problem because frequency range needed in this research is from 1.76 to 1.82 GHz. If wide tuning range is required, it can be feasible by inserting additional circuitry something like level shifter. Figure 9(b) shows free-running VCO phase noise, total phase noise at VCO output, within PLL and VCO contribution to total phase noise at VCO output, within PLL. Total phase noise is –122.6 dBc/Hz at 1 MHz.

4. Conclusion

The RF frequency synthesizer must satisfy the demands of low noise, low power, low cost, reduced size and weight at high frequency. This research is an effort of that kind of realization. Charge pump is modified to give high output impedance and current matching with active cascode transistors. D flip-flop of divide-by-2 prescaler also has a variation to provide short transient time and high frequency operation.

The constructed frequency-synthesizer has a tuning range of 1.584-1.925 GHz, phase noise of –122.6 dBc/Hz at 1 MHz, and total power consumption of 28 mW with 1.8-V power supply. Therefore it is possible to use as LO of WCDMA systems.

References

[1] B. Park and P. E. Allen, "A 1-GHz, low-phase-noise CMOS frequency synthesizer with integrated LC VCO for wireless communications," *Custom Integrated Circuits Conference,* pp. 567-570, 1998.

[2] Y.Tang, A. Aktas, M.Ismail, and S.Bibyk, "A fully integrated dual-mode frequency synthesizer for GSM and wideband CDMA in 0.5μm CMOS," *Proceedings of the 44th IEEE 2001 Midwest Symposium on,* vol. 2, pp. 866 –869, 2001.

[3] Behzad Razavi, *RF Microelectornics,* Prentice-Hall, 1998.

[4] C. Hung and Kenneth K.O, "A fully integrated 1.5-V 5.5-GHz CMOS phase-locked loop," *IEEE Journal of Solid-State Circuits,* vol. 37, no 4, April 2002.

[5] D.A. Johns and K. Martin, *Analog Integrated Circuit Design,* John Wiley, 1997.

[6] J. Craninckx and M. Steyaert, *Wireless CMOS Frequency Synthesizer Design,* Kluwer Academic Publishers, 2001.

[7] M. Tiebout, "Design and optimization of RF CMOS-circuits for integrated PLL' s and synthesizers," *Analog Circuit Design,* pp.325-337, Kluwer Academic Publishers, 2001.

[8] 3rd Generation Partnership Project (3GPP); Technical Specification Group Radio Access Networks; UE Radio Transmission and Reception(FDD), 25.101 V3.4.1.