A Novel Digital Automatic Gain Control for a WCDMA Receiver

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Abstract: In this paper, we propose a new architecture of digital automatic gain control (AGC) for a wideband code division multiple access (WCDMA) receiver. The feature of the proposed architecture is simplicity, in that it does not utilize complicated mathematical functions such as log and its inverse. When the proposed algorithm is implemented using a field programmable gate array (FPGA) device, the number of slices used to implement is 130 over the total of 5120 slices (less than 3%) with 61.44 MHz clock. This algorithm has been successfully applied to commercial WCDMA base stations.

1. Introduction

The availability of increasingly fast digital signal processing (DSP) and field programmable gate array (FPGA) devices has contributed to the emergence of software defined radio (SDR) architectures. The attraction of such an approach is that standard DSP or FPGA functional blocks may be defined to implement the back-end processing, such as the data modulator and first upconversion stage in transmit, or the final downconvert and demodulator functions in receive. A significant benefit of this approach is that the resulting architecture is reprogrammable, thereby offering generic processing suitable for a number of mobile communication signal formats.

Related to this, as the bandwidth of the digital back-end increases, the analog-digital interface can be migrated further up the transceiver chain towards the antenna. This places stringent requirements upon the performance of the system data conversion devices, namely the analog-to digital converters (ADC's) and digital-to-analog converters (DAC's). It also necessitates high-speed signal processing algorithms operating on wideband signals.

Focusing on the challenge of implementing the physical layer chip-rate signal processing of 3G standards [1], specifically, we consider the specification and performance of a digital automatic gain control suitable for a WCDMA signal and propose a new architecture for digital AGC.

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2. A WCDMA Receiver

Figure 1 shows a generic representation of the chip-rate signal processing chain for a WCDMA receiver employing the conventional AGC. The received signal, centered on a low IF (typically less than 200 MHz), is sampled by an ADC with n-bit precision. ADC's currently available operate at clock speeds of 60-125 M samples per second with 12- to 14-bit precision. These include operation in bandpass sampling modes and frequency translating whole multi-channel bandwidths. Exploiting the ADC aliasing function in this manner replaces a number of traditional analog components, including the final mixer, local oscillator and the back-end of the IF chain. Following sampling, digital downconversion (DDC) is applied to the waveform to downconvert the signal into quadrature baseband components. Quadrature digital channel filters typically perform a matched filter function whilst extracting the desired WCDMA channel for demodulation. These filters provide additional rejection of the adjacent received channel over and above that achieved in the analog receive chain, and also act to reduce inter-symbol interference.

AGC is required to normalize the signal level prior to rake reception and demodulation. Typically, the digital channel filter has a narrower bandwidth than the analog IF filter strip, resulting in the residual power present in the adjacent channels at the front-end of the digital receiver being removed. Therefore, the AGC must be capable of compensating for any variation in mean signal level introduced. The normalized output from the AGC is quantized to a low number of bits, m, before input to the rake receiver. For WCDMA signals this quantization is ordinarily between 4 and 6 bits.

For a WCDMA receiver, the dynamic range requirement in the digital AGC is dominated by the adjacent channel selectivity (ACS) specification. This is a measure of the receiver's ability to receive a wanted signal in the presence of a high-level signal falling within the adjacent channel (specified at a given frequency offset from the assigned channel). For the UMTS uplink, a bit error rate of better than 10^{-3} must be maintained at the base station for an adjacent channel offset by ± 5 MHz and received at a level 63 dB above the desired channel [1]. This requirement is illustrated in Figure 2. The composite signal is captured by the ADC with a mean power headroom of x dB below the full scale value that can be represented by the the ADC, which corresponds to 0 dB Full-Scale(dBFs). This headroom accommodates the peak excursions of WCDMA signal

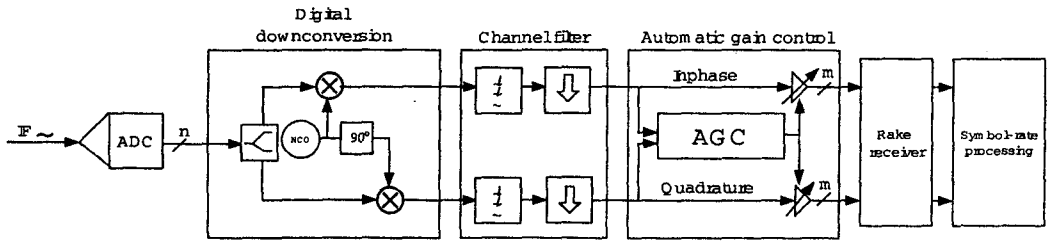

Figure 1. Signal processing chain for a WCDMA receiver.

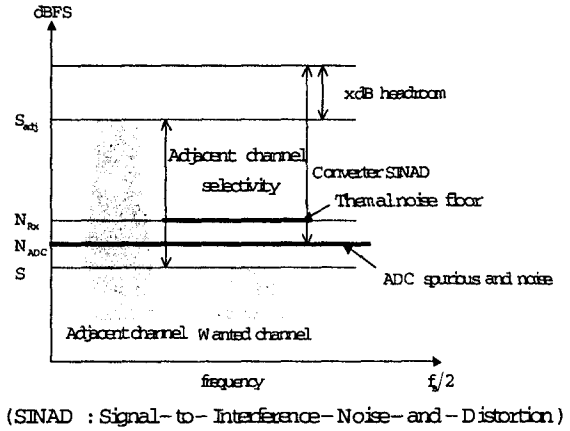

Figure 2. UMTS adjacent channel selectivity.

and provides a level of device and manufacturing tolerance. Depending upon the nature of composite CDMA waveforms being sampled, this headroom is typically set in the range 10-20 dB.

A unique feature of CDMA waveforms is that prior to despreading, the receiver operates at a negative Signal-to-Noise Ratio (SNR). It is only after the rake receiver, when the system processing gain is realized through despreading, that the signal achieves a positive E_b/N_o. Thus the wanted channel, shown in Figure 2, is at a signal power level less than the receiver thermal noise floor N_{Rx}, i.e. negative SNR.

The level of signal degradation introduced by the ADC is dependent on the location of the wideband quantization and spurious noise floor, N_{ADC}, in relation to the receiver thermal noise floor. A theoretical treatment of the reduction in SNR due to the ADC may be undertaken by calculating the total in-band noise arising from the summation of the ADC and thermal noise floors,

$$N_{TOT} = 10\log\left(10^{\frac{N_{Rx}}{10}} + 10^{\frac{N_{ADC}}{10}}\right) \quad (1)$$

where N_{TOT} is the total in-band noise power, N_{Rx} is the thermal noise power in the analog receive bandwidth and N_{ADC} is the converter quantization and spurious noise power, all measured in dBFS. The SNR degradation is then given by

$$SNR_{OUT} = S - N_{TOT} \quad (2)$$

where S (dBFS) is the input signal power and SNR_{OUT} the output SNR (dB). By way of an example, if a converter was configured such that the thermal noise floor was 13 dB above the ADC noise floor, the output SNR would be degraded by 0.21 dB relative to the input SNR.

One method to improve the SNR of the captured waveform involves oversampling the signal (i.e. sampling at greater than twice the signal bandwidth). This spreads the converter spurious and quantization noise over a bandwidth equal to $f_s/2$ and out-of-band converter noise can then be rejected by the digital channel filter.

The limited Signal-to-Interference-Noise-and Distortion (SINAD) available from state-of-the-art high-speed converters invariably means that it is the ADC that dominates implementation error in chip-rate signal processing. Therefore, the numeric precision and oversampling rates of all chip-rate algorithms should be chosen to contribute a level of numeric noise less than that introduced by the ADC.

When the adjacent channel is received at higher power levels than the desired channel, the analog channel filter passes significant power. In general, analog AGC circuits normalize the signal level according to the mean power within the composite signal of the wanted and adjacent channels. At high adjacent channel power levels, this can result in significant variation in the level of the desired channel after the digital channel filter has been applied, placing further emphasis on the the necessity of a digital AGC function.

3. Structure of the Digital AGC Algorithm

Figure 3 shows a traditional digital AGC algorithm [2] based on floating-point operation. As shown in Figure 3, this algorithm requires computing log and antilog functions and square root, which increases complexity when it is implemented in FPGA devices. Look-up table

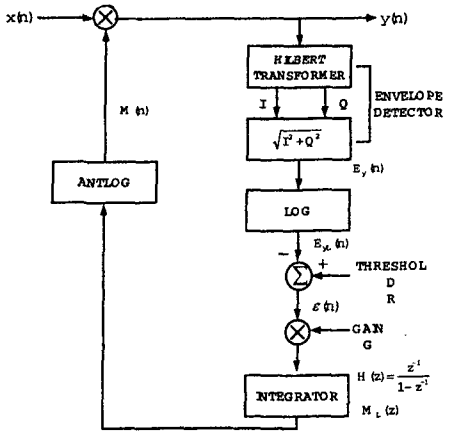

Figure 3. Block diagram of a traditional AGC algorithm [2].

(LUT)-based implementation for reducing the complexity utilizes many memories, which takes a large number of logic blocks in a FPGA device.

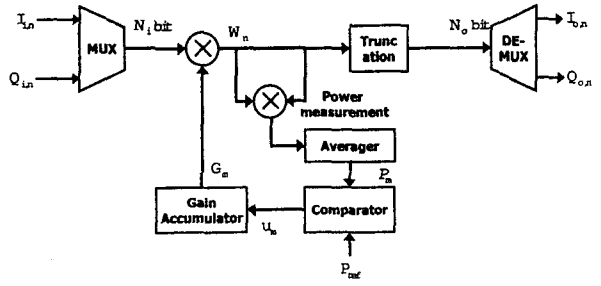

Figure 4. Block diagram of the proposed digital AGC.

Figure 4 shows the schematic block diagram of the proposed digital AGC. The input baseband signals $\{I_{i,n}, Q_{i,n}\}$ are in N_i-bit signed integer format and are multiplexed and multiplied by the unsigned P-bit integer output of the Gain Accumulator G_m to produce $(N_i + P)$ bit integer product W_n. The signal W_n from which the output signal $\{I_{o,n}, Q_{o,n}\}$ is obtained by truncating to N_o-bit ($N_o < N_i$), is fed into the square multiplier and averager to establish the closed-loop AGC.

The power average P_m is compared with the reference value P_{ref} and the feed back control signal u_m is obtained as

$$u_m = \mathrm{sgn}(P_{ref} - P_m). \tag{3}$$

The gain accumulator, of which the detailed structure is given in Figure 5, updates the exponentially increasing/decreasing gain value in every M sample period in response to the control signal, which builds up our AGC algorithm as

$$G_{m+1} = G_m \left(1 + \frac{1}{2^K}\mathrm{sgn}\left(P_{ref} - \left(\overline{I_{i,n}^2 + Q_{i,n}^2}\right) G_m\right)\right), \tag{4}$$

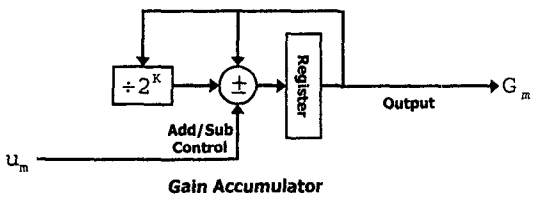

Figure 5. Architecture of the gain accumulator.

when the AGC is locked to the reference value P_{ref}.

In case where the output power average is far from the reference value, the gain accumulator exponentially increases/decreases the gain value with

$$G_{m+1}/G_m = \left(1 \pm 1/2^K\right) \tag{5}$$

to approach the locking point. The exponential behavior of the gain accumulator provides the linear slew rate in dB scale such that

$$\text{Slew Rate[sec/dB]} = \frac{2^K M}{8.68R}, \tag{6}$$

where R is the input data rate (sample/sec). The dynamic range of the AGC is closely related to the gain accumulator. The gain accumulator should be designed to have the minimum gain of 2^K to avoid to gain value of zero which causes the AGC in fail. Also the accumulator should be saturated to the maximum value $2^P - 1$ where the accumulator bit-size is P. From the design parameters P and K, The gain dynamic range (GDR) of the AGC is

$$\text{GDR[dB]} \approx 6(P - K + 1). \tag{7}$$

4. Simulations, Implementations and Experiments

The convergence characteristics of the AGC algorithm obtained from the computer simulation is shown in Figure 6. The 14-bit input value to the AGC is set to the constant values of $\{I, Q\} = \{496, 929\}$ where the gain is in minimum value. The gain curve (c) shows the exponential behavior until the AGC gets in lock. The power reference has been set to the 8 dB below the peak value of the 5-bit truncated output.

We have verified the performance of our proposed AGC using the WCDMA digital IF modules. Figure 7 is the experimental setup to investigate the performance of our AGC. The signal source generates a single WCDMA carrier (1 SCH+ 1 CPICH + 1 DPCH) at 190 MHz. This analog WCDMA IF signal is converted to the 14-bit digital base band I/Q signal with the data rate of 2x (1x = 3.84MHz) by the down-converter, and is fed into our AGC implemented in the FPGA (Xilinx Virtex-II). The up-converter converts the output of the

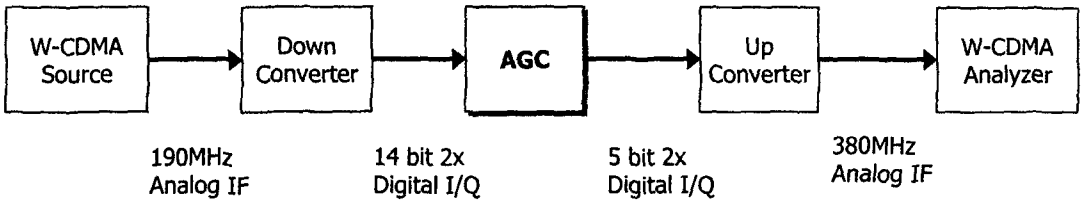

Figure 7. Experimental set up for the AGC measurement.

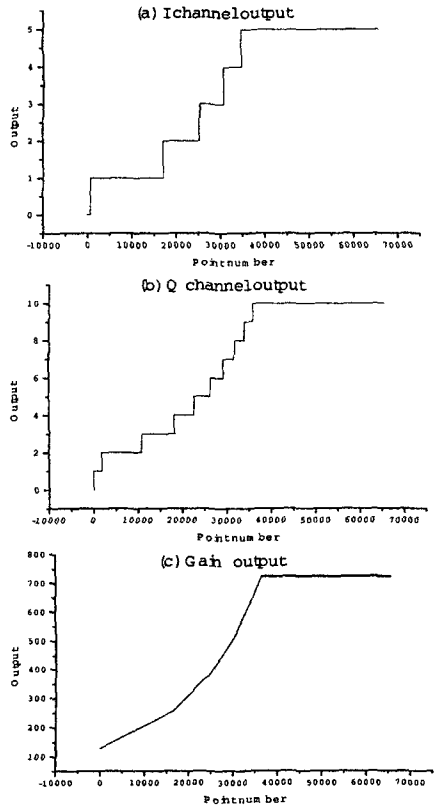

Figure 6. The convergence characteristics of the AGC.

AGC to the analog IF signal at 380 MHz to be analyzed by a WCDMA analyzer and the average channel power was measured in the code domain. Various experimental results are compared in the Figure 8. The curve with square symbols shows the detected channel power with no AGC and no truncation between the down- and up- converters. The plot with circle symbols is the results with AGC and 5-bit truncation. The plot with triangle symbol is the data with no AGC and 5-bit truncation from MSB (D[13:9]). The valid data decode was available when the average active channel power is greater than -6 dBc. The results show that our AGC can cover the full dynamic range of the 14-bit input signal with only 5-bit output.The implementation of our AGC took only 3% of the total gates available in the FPGA (XC2V1000) with 2 built-in multipliers running on 61.44 MHz (16x) clock.

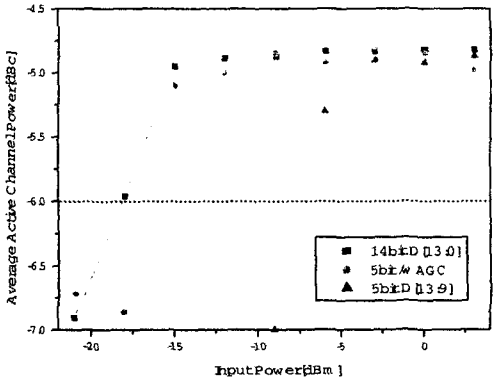

Figure 8. Results of the AGC experiment.

5. Conclusion and Discussions

This paper proposed and analyzed a new architecture of digital automatic gain control for a WCDMA receiver. The exponential gain lock-in behavior provides the linear slew rate property in dB scale.The simplicity of the architecture without using complicated mathematical functions greatly reduces the number of gates in FPGA/ASIC implementation and the power consumption. This algorithm has been successfully applied to commercial WCDMA base stations.

References

[1] 3rd Generation Partnership Project, "UTRA (BS) FDD; Radio Transmission and Reception," 3GPP TS 25.104 v3.5.0.

[2] M. E. Frerking, *Digital Signal Processing in Communication Systems*, Van Nostrand Reinhold, New York,1994.