Digital Gray-Scale/Color Image-Segmentation Architecture for Cell-Network-Based Real-Time Applications

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Abstract: This paper proposes a digital algorithm for gray-scale/color image segmentation of real-time video signals and a cell-network-based implementation architecture in state-of-the-art CMOS technology. Through extrapolation of design and simulation results we predict that about 300 × 300 pixels can be integrated on a chip at $100nm$ CMOS technology, realizing very high-speed segmentation at about $160\mu sec$ per color image. Consequently real-time color-video segmentation will become possible in near future.

Keywords—**Image segmentation, Cell network, LSI implementation, Digital CMOS**

1. Introduction

Image segmentation is the process by which the original natural image is partitioned into meaningful regions and is an important initial task for higher level image processing such as object recognition or object tracking. Several image segmentation algorithms have already been proposed and can be classified into five groups [3]; pixel classification, edge-based approaches, region-based approaches, model-based approaches, and hybrid approaches, which combine edge- and region-based approaches. Conventional gray-scale/color image segmentation algorithms are implemented in software and their complexity is usually high. Therefore, real-time processing and compact hardware implementation are difficult. For binary images, several types of fast labeling hardware have been proposed [2], [4], [5]. However these methods cannot easily extend to the segmentation of gray-scale/color images. The region growing algorithm [3] is a well-known region-based method suitable for coherent region extraction. Recently, D. L. Wang et al. proposed a differential-equation based region-growing algorithm for locally excitatory, globally inhibitory oscillator networks (LEGION) [6], which has been modified for analog VLSI integration [1].

In this paper, we propose a digital algorithm for gray-scale/color image segmentation of real-time video signals and a cell-network-based implementation architecture in state-of-the-art CMOS technology. Segmentation of gray-scale or color natural images can be achieved by changing only a preprocessing circuit for the weight calculation. The effectiveness of the cell-network-based architecture is verified by a semi-custom test-chip, which includes 10 × 10 cells, in 0.35μm 3 metal layer CMOS technology.

The paper organization is as follows. In Section 2, we describe the algorithm for gray-scale/color image segmentation. In Section 3, a cell-network-based architecture for digital VLSI implementation is presented. In Section 4, simulated performance and design area estimation of the proposed architecture are shown. Finally in Section 5, we describe our conclusions and the consequent aims of future research.

2. Image Segmentation Algorithm

The segmentation algorithm uses a region-growing approach, which can be viewed as a simplified digital version of a locally-excitatory globally-inhibitory oscillator network (LEGION) [6]. The flowchart of the proposed algorithm is shown in Fig. 1. It uses six functional steps; (a) initialization, (b) detection of a self-excitable cell (leader cell), (c) self-excitation of the leader cell, (d) detection of excitable dependent cells, (e) excitation of dependent cells, (f) inhibition of all excited cells of a segment. Steps (d), (e) and (b)-(f) are carried out in inner and outer loops, respectively.

The details of the algorithm are shown in Figs. 2 and 3. In the proposed algorithm, the inclusion of each pixel i in a given segment is decided by examination of its connection weights W_{ij} with the neighboring pixel j (Fig. 2). These weight are calculated from the differences of luminance $|I_i - I_j|$ between pixel i and its eight neighboring pixels j. First, in the initialization step, the connection weights W_{ij} of all cells are calculated with formulas (Fig. 3 (1.2)) slightly different for gray-scale or color images. A leader cell (a self-excitable cell, $p_i = 1$) is defined by a connection weight $\sum_{j \in N(i)} W_{ij}$ of eight neighboring pixels $N(i)$ is bigger than a predefined threshold ϕ_p. Next in the outer loops, one of the leader cells is excited and a new region is grown from this leader cell. If the sum of connection weights with neighboring excited cells is bigger than another predefined threshold ϕ_z, cell i is automatically excited. The above region growing operation is repeated in the inner loop of the proposed algorithm as long as excitable-cells exist. If there is no excitable cell, all excited cells of the determined segment are inhibited. The above excitation/inhibition operations are repeated until all leader cells are inhibited. Color and gray-scale picture segmentation differ only in the expressions of Fig. 3 (1.2) for the connection-weight calculation between the network cells.

The image segmentation algorithm has following important features: (1) Segmentation is realized in a very short time due to the simple processing. (2) Due to the simple structure of each cell, representing a pixel, compact integration of many cells on a single chip becomes

possible. (3) Further speedup of the segmentation process is possible by parallel operation of all cells, enabling large-scale image segmentation. (4) Fast software implementation is also possible, because simplicity and parallel excitation can be exploited on computer systems, too.

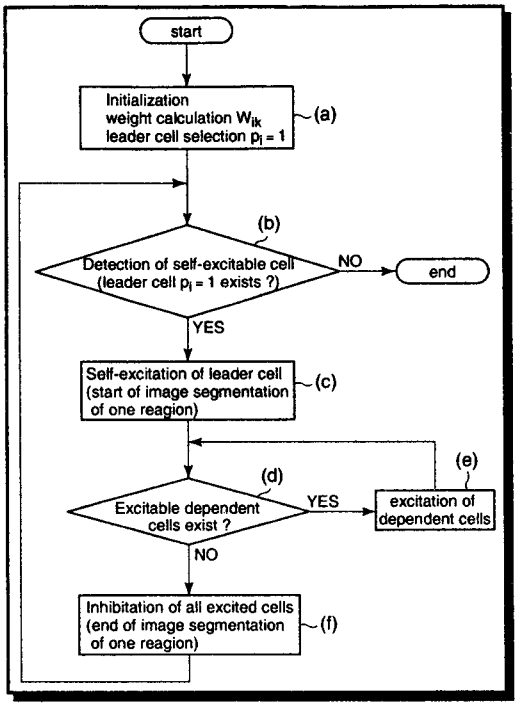

Figure 1. Flowchart of the proposed image segmentation algorithm.

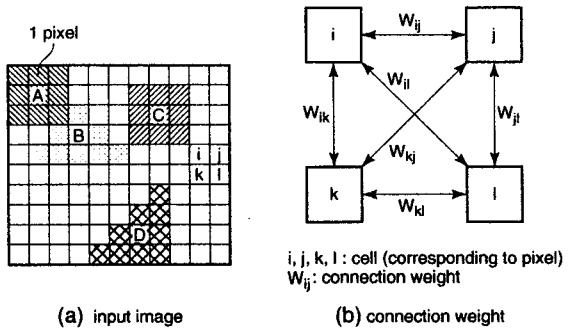

Figure 2. An input image (a) with leader cell A, B, C, D and connection weights (b) among cells. Each cell corresponds to a pixel.

3. Cell-Network-based Architecture for Digital VLSI Implementation

The proposed VLSI-implementation architecture (Fig. 4) consists of 4 functional stages for connection-weight calculation, leader-cell determination, image segmentation and segmentation-result restoring, respectively.

[Image Segmentation Algorithm]

1. Initialization
   1. Initialization of global inhibitor. $z(0) = 0$;
   2. Calclation of the connection weights.
      (a) gray scale images
      $W_{ik} = \frac{I_{max}}{1+|I_i - I_k|}$, $k \in N(i)$;
      (b) color images
      $W(R)_{ik} = \frac{I(R)_{max}}{1+|I(R)_i - I(R)_k|}$, $W(G)_{ik} = \frac{I(G)_{max}}{1+|I(G)_i - I(G)_k|}$,
      $W(B)_{ik} = \frac{I(B)_{max}}{1+|I(B)_i - I(B)_k|}$, $W_{ik} = \min\{W(R)_{ik}, W(G)_{ik}, W(B)_{ik},\}$.
   3. Detection of leader cells.
      if($\Sigma_{k \in N(i)} W_{ik} > \phi_p$) then $p_i = 1$; otherwise $p_i = 0$;
   4. Set all cell to non-excitation. $x_i(0) = 0$;
2. Self-excitation
   if (excitable cells = f) then stop; // terminate
   else if (find_leader( ) == $i \wedge p_i == 1$) then
   $x_i(t+1) = 1, z(t+1) = 1$; go to (3.Excitation) // self-excitation
   else go to (2.Self-excitation);
3. Excitation
   Setting of global inhibitor $z(t) = \vee_{\forall i} z_i(t)$; // logical OR of z_i
   if ($z(t) == 0$) then // no self-excited cells exist
   if ($x_i(t) == 1$) then
   $x_i(t+1) = 0$; $z_i(t+1) = 0$; $p_i = 0_i$ // inhibition
   go to (2.Self-excitation);
   else if ($x_i(t) == 0 \wedge z_i(t) == 0$) then // non-excitation
   $S_i(t) = \Sigma_{k \in N(i)} (W_{ik} * x_k(t))$;
   if ($S_i(t) > \phi_z$) then $x_i(t+1) = 1$; $z_i(t+1) = 1$; // excitation
   else $x_i(t+1) = 0$; $z_i(t+1) = 0$;
   else if ($x_i(t) == 1 \wedge z_i(t) == 1$) then $x_i(t+1) = 1$; $z_i(t+1) = 0$;
   go to (3. Excitation);

Figure 3. Detail description of the proposed image segmentation algorithm.

In the 1st stage the pixel data, i. e. luminance data $(I(L)_i)$ for gray-scale and RGB-data $(I(R)_i, I(G)_i, I(B)_i)$ for color pictures, are used to determine the connection weights W_{ij} between pixels according to the expressions of Fig. 3 (1.2) for picture columns in parallel. The calculated connection weights are transferred to the 2nd stage for determining leader pixels ($p_i = 1$) and ordinary pixels ($p_i = 0$). Leader pixels represent the seed pixels in the subsequent region-growing mechanism and require that the sum of the connection weights with their 8 nearest neighbors is larger than a predetermined threshold. The stages for connection-weight (W_{ij}) and leader/ordinary-pixel (p_i) calculation perform the initialization step in the algorithm of Fig. 3 and transmit W_{ij}, p_i to the cell-network of the image-segmentation stage in a column-pipelined mode. Each cell of the 3rd stage, the image-segmentation network, represents a pixel of the original picture. In this network, which consist of active cells and connection-weight registers, the self-excitation and excitation steps of the algorithm of Fig. 3 are carried out for all pixels of the picture in parallel. The structures of an active cell, a block of 4 connection-weight-registers, and the layout-floorplan for

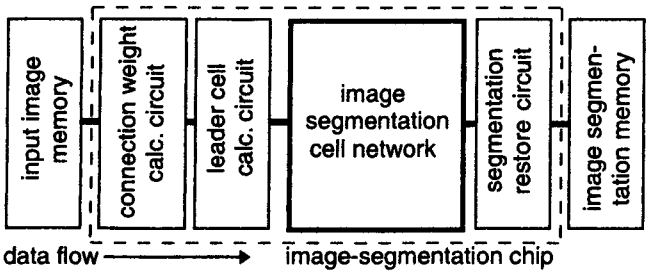

Figure 4. Block diagram of the cell-network-based image segmentation architecture.

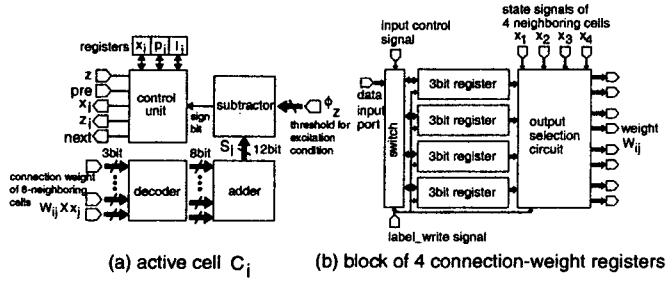

Figure 5. Structure diagram of active cells and connection weight-register blocks.

the network are shown in Fig. 5, 6 and 7, respectively. The active cell consists of decoder, adder/subtractor, control unit and three 1-bit registers. The connection weights are stored in blocks of 4 registers(Fig. 5) classified into horizontal and vertical register blocks as shown in Fig. 6. The horizontal (vertical) register blocks hold their four connection weights between pixels in positions of diagonal and horizontal (vertical) directions. As shown in Fig. 7, the complete cell-network can be implemented by alternately laying a cell, corresponding to a pixel, and a horizontal or vertical connection-weight register block. Thus the connection weights can be efficiently shared among neighboring cells, and the wiring length can be minimized. Since the cell structure becomes simple and compact, high speed and high density implementation is achieved.

In each region-growing cycle for a segment the new cell-state is decided by the states of the neighboring cells and the connection-weight registers. The 1-bit register l_i in each active cell is used as a flag for indicating whether this cell is included in the presently grown segment or not. After the growth of a given segment is completed, the segment number is stored in the upper-left connection-weight registers of all cells belonging to this segment. The segmentation process in the cell-network finishes, if new segments cannot be grown anymore, i. e. when all leader pixels have been used up. The segmentation result, i.e. pixel/segment-number pairs, is then read-out from the cell network in a column-parallel mode and transmitted to the image-segmentation memory by the final segmentation-restore stage.

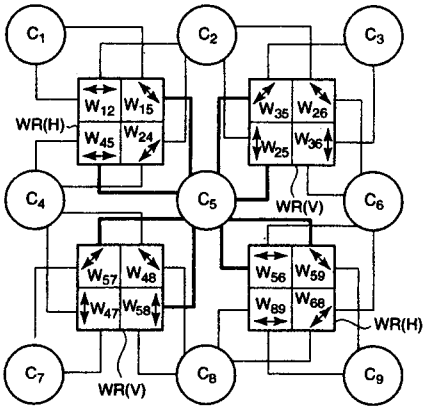

Figure 6. An example of connections among cell C_5 and its four neighboring connection weight register blocks. The connections related to C_5 are shown with bold lines.

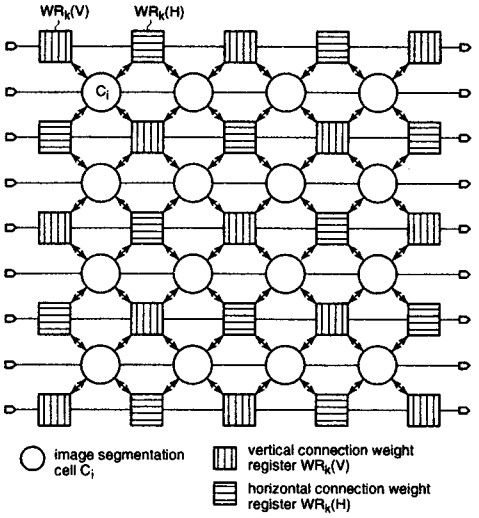

Figure 7. Block diagram of the cell-network construction.

4. Simulated Performance and LSI Implementation

We have written a software simulator of the cell-network-based segmentation architecture of Figs. 4 and 7 in C and Java languages and tested many sample images. Typical segmentation results are shown in Fig. 8. The simulated processing time of the cell-network-based architecture is shown in Fig. 9. For 400 × 400 (160,000 pixels) images, very high-speed image segmentation with about $50\mu sec$ (at 100MHz clock frequency) on the average and about $300\mu sec$ (at 100MHz clock frequency) in the theoritically estimated worst case is verified.

The cell-network core was designed in 0.35mm, 3 metal CMOS technology. All circuits of the cell-network core were designed and verified with the hardware description language VERILOG, and automatically generated by Synopsys' Design Compiler with a standard-cell

library from the high-level VERILOG design. The layout of the cell-network core is shown in Fig. 10, which includes 100(10 × 10) cells on about $13.3mm^2$. Since decoder and adder/subtractor of the active-cells consume the largest area portion, the full-custom design of these circuits will be made the large reduction of a design area. We have estimated the possible pixel density for full-custom high-speed (bit-parallel active cell) and high-density (bit-serial active cell) designs in scaled-down CMOS technologies (Table. 1), assuming just 3-metal layers. From this data we expect a one-chip integration of the proposed architecture for 300 × 300 pixel pictures at the 100nm technology node and for 800 × 600 pixel pictures at the 50nm technology node.

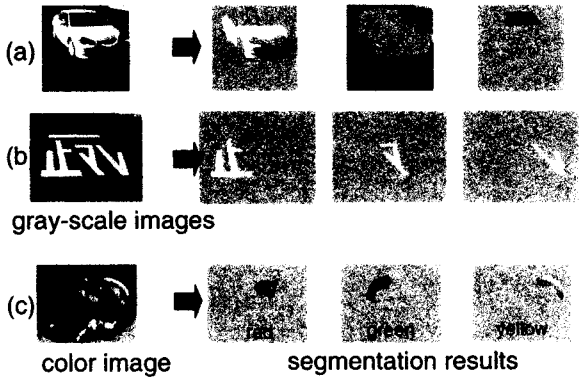

Figure 8. An example of image segmentation for gray-scale/color images.

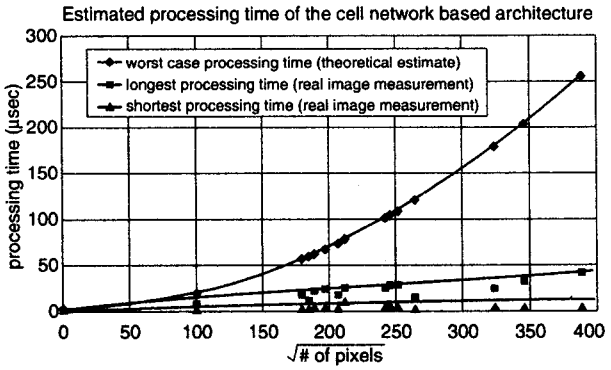

Figure 9. Simulated processing time of the cell-network-based image segmentation architecture at 100MHz clock frequency.

5. Conclusion

We proposed a digital algorithm for gray-scale/color image segmentation of real-time video signals and a cell-network-based implementation architecture in conventional CMOS technology. Segmentation of natural gray-scale or color images requires only a small change in the preprocessing circuit for weight calculation. Practical application in fully-integrated motion-picture-segmentation chips is estimated to become possible at the 100nm-technology node.

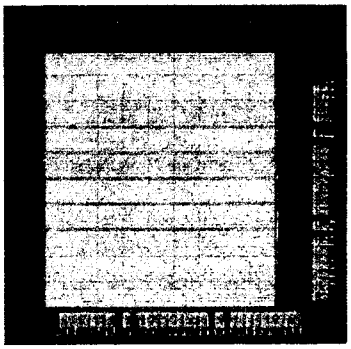

Figure 10. Layout of the the cell-network core with a standard cell library of $0.35\mu m$ 3 metal layer CMOS technology. The size of the semi-custom design is about $3.5mm \times 3.8mm$ (10 × 10 cells).

Table 1. Estimated pixel density by full-custom design.

technology node	integration density (pixel/mm^2)	
	high speed arch. (bit parallel)	compact arch. (bit serial)
$350nm$	22	43
$180nm$	81	163
$100nm$ (2003y)	263	527
$50nm$ (2010y)	1054	2107
$35nm$	2150	4300

The future research includes a further area reduction of the cell-network core by the full-custom design. The improvement of the architecture and the development of an image segmentation system are also considerable topics.

Acknowledgment

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