Image Processing LSI Design by C Base Language

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Abstract: In late years, the tendency to shift the design language of electronic circuits from HDL to C-based languages of C/C++ and so on is strengthened. The current of adopting these software languages thrives by necessity to solve the problem peculiar to HDL that verification of design is difficult. When we use C-based languages, we can describe the design by higher abstraction degree, mount the design as both hardware and software finally and so that express the design part which is not made clear at early stage the same one language. Therefore, the flexibility of design very improves, the design work in environment the range of applying the whole systems become possible. This paper introduces example at having applied C-based languages in image processing LSI design and describes that the design technique of C-based languages is effective for the system design.

1. Introduction

The technology of electronics holds leap with progress of LSI, and it is expected when LSI of 1M gate and over, high speed signal of GHz level, further low power, lightweight miniaturization become possible recently and continue this tendency in future and is found that we gets possible to realize system LSI having degree of integration of 1 billion transistor scale according to the prediction after about 7 years[1],[2]. We have to build new design technique in order to improve by design productivity. As key and means of this purpose, there are three of follows.

①Improvement of design abstraction degree
②Recycling of design assets
③Reduction of design itaration

They hits part of improvement of design abstraction degree with focus mainly and at first describes description method of current VLSI design flow and design and classifies simulation technique in upper-class design process of design next, and this report describes example and describes the C-based design technique that they explains it about these simulations technical characteristic technology, and gather interest of LSI developer recently more, applied this technique in image processing LSI design as follows[3],[4].

2. VLSI Design Flow

At first, we explain VLSI design flow, and show each step of VLSI design in Figure 1., and general procedure of upper-class design and lower-class design at calls it, and designing it using hardware description language (HDL) seems to become next from upper-class design, layout design and mask pattern from system level design.

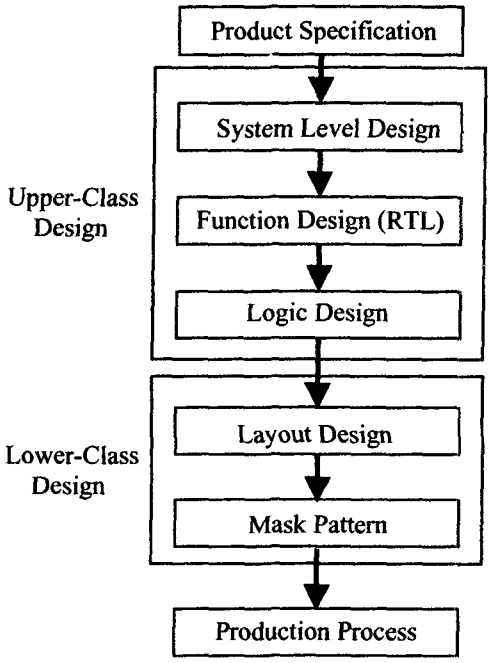

Figure 1. VLSI Design Flow

2.1 System Level Design

Based on given design specification (function specification) design description by system level is done. In addition, to be manufacturing processes deciding demanded movement and constitution in order to realize specification of a system with VLSI. Because generally system LSI has CPU and Digital Signal Processor, memory circuit built-in here, can realize a function with software, and so the system division to be decided by allotment by hardware/software each is done, and system is divided by this design level by component of plural number, and function confirmation of system is done by connection between these components and components (net list) is described and can describe system level movement of each component using behavior description, and executing function simulation for this description.

2.2 Function Design (RTL Design)

We express system here by register and combination circuit, call this register transfer (RT) level description. Based on design description by the system level mentioned above, function design of RT level is done. By design description by RT level, consist of movement description of connection description and a component of a component. However, it

is the point where the description level of each component is RT instead of behavior that be different from the description by system level. A register and operation at register interval and data flow are described RT description, and design begins to be realized.

2.3 Logic Design

Go into details about RT level description more here, and constitute logical circuit of a gate level. Can get the design of gate level by inputs design description of the RT level mentioned above into logic composition system, and doing logic composition. Work of logic composition is executed by step of logic design. Wiring between components (net list) is generated by doing logic composition[5].

2.4 Layout Design

Take out the gate and layout information of logic cell from the library which is the database which design specification of cell, circuit and layout information, electric characteristic were registered with here, and decide arrangement and wiring on a tip.

2.5 Mask Pattern

Pass, and, as for the mask pattern data of a necessary photo mask, be made the process that self inspects a process and a conversion result to convert designed drawing into production data of mask with CAD in order to form circuit of VLSI. In late years, in addition to increase of a quantity of design data, more minute wiring pattern is demanded, and there is processing time of data conversion from this CAD drawing and data inspection to guarantee reliability of photo mask in tendency to increase.

3. C-Based Design Technique

Generally, the system level design person analyzes C/C++ with definition of system in base and the environment that did, and hand the system specification that can execute compose complete, and, however, as for this method, there movement of system after decision to hardware design person and software design person. Let the HDL code is a problem that an act of man mistake is easy to occur while a hardware design person converts the specification that can execute written with C/C++ into HDL, and adding details description more after time suffers from work to renew C/C++ code in an equal HDL description. In addition, there become great many quantities of work in order to be accompanied with work to transfer test bench written with C/C++ to HDL usually. Furthermore, system level design person must participate again because you must analyze a different substitute design in the whole specification that C/C++ can execute when you were going to test trade off to influence movement of the whole system by a hardware design process. Do not transfer the specification that can execute of C/C++ which a system level design person made to HDL in order to solve this problem, and the technique how is smooth, and reliability is high that hardware design person oneself can go into details about to the form that can take advantage of as the input to a hardware composition tool is necessary. Can recycle test bench written with C/C++ by doing conversion from C/C++ to HDL unnecessarily. As a result, inspection time is shortened, and be guaranteed to be based on original specification. Get together, and compare it with RTL model by designing system LSI by C-based language, and simulation is possible, and can reduce the number of mechanic to hang in inspection by the speed of 1000-100 times. By it, can reduce total mechanic number, and early bug discovery, revision, examination become possible[5].

4. Image Processing LSI Design Example

As for the merit of using C-based language for LSI design than HDL, there are three of the following.

①Inspection to be higher-speed than HDL is possible
②We can use common language with hardware and software
③High abstraction degree making a dummy is possible

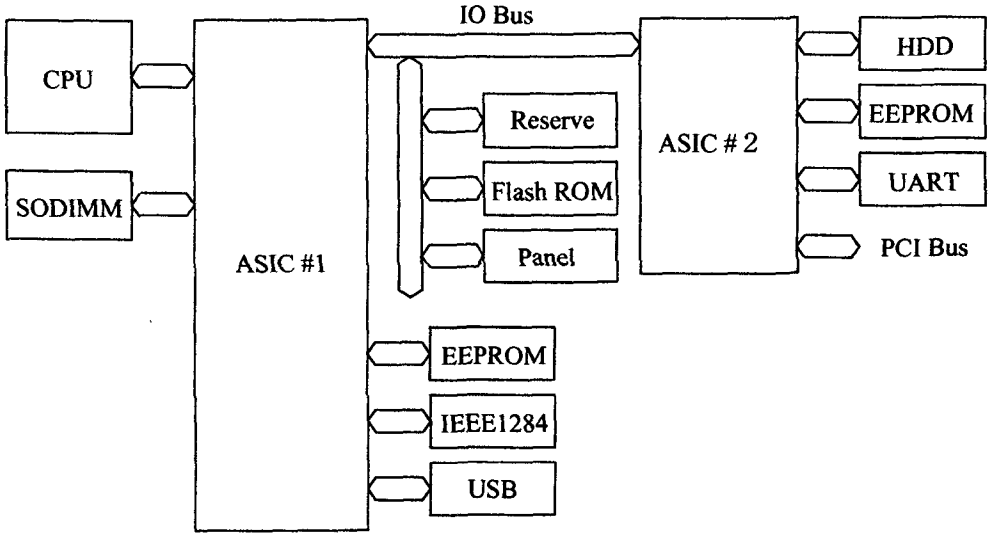

Figure 2. Component Structures

Theses describes the design example that used C-based language for image processing LSI design to need complicated processing this time. At first HDL and C-based language describe algorithm to change color image in arbitrary size for comparison examination, and simulation does each and compares the result. As a result, it became clear that C-based design was effective in LSI design.

We design the image processing LSI and Figure 2. shows that the component structures includes them. They are concretely the ASIC #1 of Figure 2.

The Table 1. shows traditional design technique. The specification design is written on the documents. And then, the function design described by HDL like a VHDL or Verilog-HDL. Therfore, the function verification is used HDL simulator and it necessary a lot of time for verification.

Table 1. Former Design Technique

Specification Design	Function Design	Function Verification
Documents	HDL	HDL Sim

The Table 2. shows futuer design technique of this time. The function design and function verification progress smoothly by using C/C++ language from the stage of specification design. Therfore, we can reduce TAT drastically.

Table 2. Future Design Technique

Specification Design	Function Design	Function Verification
C/C++	C Base	C Sim

5. Results and Discussion

We evaluated from C to HDL conversion in this time by using tools. The circuit is characterized by it with engine part for image processing, and there is not inside memory, and 82000 gate, frequency 100MHz. The evaluation environment used HP Pentium Ⅱ. Simulation contents carried out 1000 times of image composition, and executed the simulation cycle by 150000 times. Show HDL and comparison evaluation result by C base language next. The C-based language code size was 12400 lines in 272000 characters. We can reduce around 64% when compares code size of HDL with C base. In addition, the improvement of simulation speed was 138 times. Confirmed agreement of expectation by test pattern 50 pattern.(show Table 3.)

We evaluated design productivity by C base RTL design technique next. Understand what it grows by traditional design technique between 3weeks that development period of RTL was 9weeks and was able to shorten for about 6 weeks.(show Table 4.)

Table 3. Comparison List of Design

	HDL	C Base	Comparison
Characters	760000	272000	64% down
Lines	36800	12400	66% down
Sim Time sec	165	1.2	138 times

Table 4. Comparison List of TAT

Items	Specification Design	Function Design	Function Verification
HDL	2 week	1.5 week	2.5 week
C Base	1 week	1 week	1 week

It were the same, but, as for the specification development period, a function design period became the future as before for one week from three weeks because about around 60% design description quantity decreased as had explained. In addition, the verification period became that simulation speed became high-speed between 1week from 6weeks because of being reinstated design decreased. But two folds developed the same hard model with HDL and C before, but trouble evasion of consistency can by what simplification does this time about the number of design mechanic next. Because C-based language development is finished, be automatic, and the pivot progresses in a process to lose from HDL conversion to gate. By this, were able to shorten it from 28 weeks to four weeks.

6. Conclusions

A tendency to do a description of hardware and description of application software using common C-based language goes along currently. In co-design environment, do not distinguish hardware and software, and C-based language will describe function of system, and generate HDL description and object code of applications program which can compose the logic from this system description[6]. The C-based language is the mainstream, and, as for the system specification description language, main language includes SystemC, SpecC, Superlog, but be stages to be non-still clear which becomes normal for the moment.

In particular, in transition period of switchover from a current RTL design, design and the thing that a specification description and RTL description seem to coexist are expected. A rank composition tool introduces it in such situation, and a thing of fact.

However, by design example of this time, C base Design understood that it was effective in a system design. For example, as for the C base simulation, speed improved than HDL simulation. In addition, by what a development period and the number of design mechanic were able to reduce, the

thing that was effective for improvement of design productivity became clear[7].

Shortening of development period, reduction of quantity of code, improvement of high-speed simulation speed were able to come true. 1.75 men per month were able to decrease from 7 men per month number of design mechanic reduction. There was trouble evasion in matching by 1 yuan development. Scale of LSI was speed, but, as for the speed, 30% improved, but the scale became increase of 15% by a gate level.

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