Oscillation Frequency Estimation for Detecting Feedback Bridging Faults

Masaki Hashizume, Nobuyuki Inou, Hiroyuki Yotsuyanagi, Takeomi Tamesada
Department of Electrical and Electronic Engineering, Faculty of Engineering
The Univ. of Tokushima
2-1 Minamijyousanjima Tokushima-shi, 770-8506 JAPAN
E-mail { tume, yanagi4, tamesada}@ee.tokushima-u.ac.jp

Abstract: When a feedback bridging fault is activated in a circuit, logical oscillation may occur at a signal line. If the oscillation appears, the fault may not be detected by logic testing. In order to detect such bridging faults, output logic values of the circuit should be measured at higher frequency than frequency of the logical oscillation. In this paper, a method for estimating the maximum frequency of logical oscillation is proposed to detect such bridging faults in a circuit by logic testing. Also, it is shown by some experiments that such bridging faults can be detected by measuring output logic values at the frequency obtained by the method.

1. Introduction

It is well known that bridging faults often occur in logic circuits implemented with the state-of-the-art technology. The bridging faults are classified into 2 kinds of faults; I/O bridging fault and feedback bridging(FB) faults[1,2].

A bridging fault is activated by providing a logic value and the complement one to one of the bridging signal lines and the other ones, respectively. In the case of FB faults, oscillation of logic value may appear at the bridging signal lines. If the oscillation occurs, the fault may not be detected by measuring the output logic values. In order to detect it by logic testing, logic value of the primary output terminals should be measured more than one times after each test vector is provided.

All FB faults in a circuit under test(CUT) can be detected by measuring the output logic values at higher frequency than the maximum frequency of logical oscillation. Thus, in this paper, we discuss the derivation method of the maximum frequency of logical oscillation.

It should be identified which FB faults can generate logical oscillation to derive it. Furthermore, the oscillation frequency should be estimated for each of the FB faults. Since there are many FB faults in a logic circuit, it should be derived with as small computational cost as possible.

It depends on some requirements whether an FB fault can occur logical oscillation when the fault is sensitized. The requirements are classified into logical and electrical ones. The logical requirement is that there should be odd number of inversions between the bridging signal lines[1]. Even if the logical requirement is satisfied, logical oscillation may not appear. Some electrical requirements should be satisfied. The requirements have been proposed in [2] and [3].

An estimation method of logical oscillation frequency has been proposed in [2]. However, it is assumed in [2] that input threshold value of a CMOS logic gate is identical to the others. Usually, the assumption will not be held. Thus, we proposed an estimation method of the maximum oscillation frequency[4]. It is shown experimentally that the maximum frequency of logical oscillation can be estimated by using our method.

However, we found out that even if the method is used, the maximum frequency may not be always estimated. Thus, we attempted to improve the method proposed in [4] so that the maximum frequency can be estimated. We propose it in this paper. Also, we show the effectiveness of our new method by some experiments.

In this paper, our new estimation method for the maximum frequency is proposed in section 4 after introducing FB faults in section 2 and the test method in section 3, respectively. By using the method, the frequency is estimated for a CMOS circuit in section 5 and the effectiveness of the method is evaluated.

2. FB Faults with Oscillation

An FB fault is shown in Fig.1. As shown in Fig.1, the faulty logic value of one of the bridging signal lines, which is generated by the sensitization of the fault, is affected to the other ones by the fault propagation.

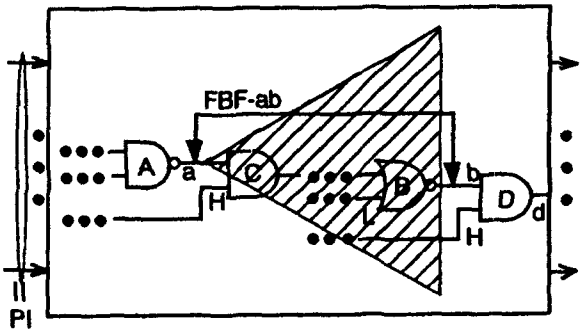


Fig.1 Feedback bridging fault.

All of the circuits having FB faults can be modeled as the circuit in Fig.2[3,4]. An example circuit having an FB fault is shown in Fig.3. In Fig.3, when PI_1=H and PI_2=L, the FB fault FBF-ab between the signal lines *a* and *b* can be excited. By the excitation, logical oscillation may be generated. Some waveforms generated by the excitation of the FB fault are shown in Fig.4.

It depends on the layout design of gates A, B and D and the propagation delay time of the sub-circuit between gates A and B whether oscillation occurs. We proposed in [3] how to identify FB faults with small computation

costs. By using the method, it can be determined whether an FB fault can generate oscillation.

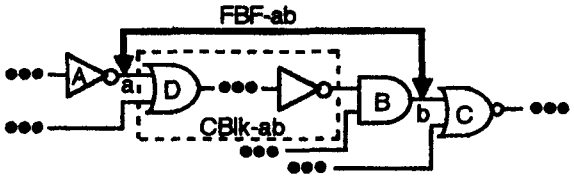


Fig.2 Circuit having FB fault

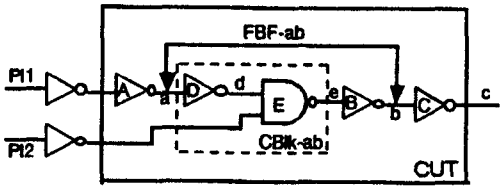


Fig.3 Circuit under test.

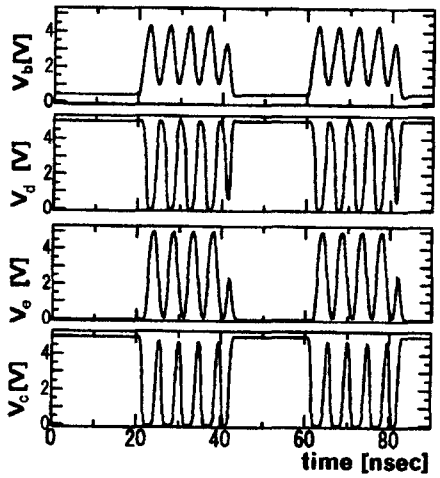


Fig.4 Example waveform of oscillation.

3. Detection of FB Faults with Oscillation

FB faults generating logical oscillation can be detected by sampling the voltage waveform at each primary output terminal at high frequency. The logical oscillation is shown in Fig.4 which can appear at a signal line *c* when FBF-ab is activated in Fig.3. The waveform of Vc is modeled as in Fig.5. If the period of the logic oscillation is assumed to be T_{osc}, the fault can be detected by sampling Vc per T_{smp} which satisfies Eq.(1).

$$T_{smp} \leq T_{osc}/2 \quad (1)$$

If a sampled logic value is different from the last sampled ones, the circuit can be determined as faulty, since a constant logic value will be measured in the fault-free circuits.

All of the FB faults which may occur logical oscillation in a logic circuit can be detected by measuring logic values of the primary output terminals per the half time of the minimum period of logical oscillation which can occur in the circuit. Thus, in this paper, it is discussed how to derive the minimum period, that is, the maximum frequency of logical oscillation.

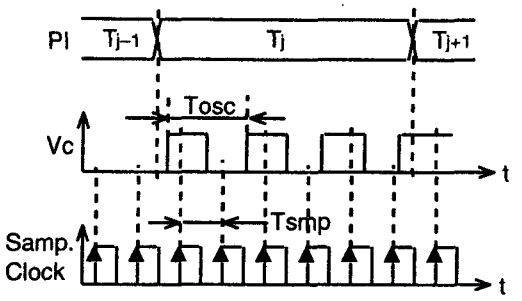


Fig. 5 Test method for FB fault with oscillation.

4. Oscillation Frequency Estimation Method

In order to estimate oscillation frequency preciously, circuit simulation should be executed for faulty circuits. However, it takes a long simulation time to obtain the oscillation frequency, since transient analysis must be executed. Furthermore, there are a lot of FB faults in a circuit. In order to derive the maximum frequency, circuit simulation must be executed for all of the bridging faults. Thus, it is impossible to derive the frequency by executing circuit simulation for all of the faulty CUTs.

It has been proposed in [2] how to estimate frequency of logical oscillation generated by an FB fault without executing circuit simulation for each faulty CUT. The method in [2] is based on an assumption that input threshold voltage of each gate is identical to other gates. In many practical ICs, the assumption can not be held. Thus, it is impossible to estimate the frequency precisely for many CUTs by using the method proposed in [2].

On the other hand, it is requested to derive the maximum frequency of logical oscillation in order to detect FB faults in a CUT. Thus, we proposed a method for estimating it[4].

The waveform of the voltage at the signal line *a*, Va, is shown in Fig.6, generated when logical oscillation occurs in the faulty circuit of Fig.3. In [4], the Va waveform is modeled as Fig.7 with piece linealized models.

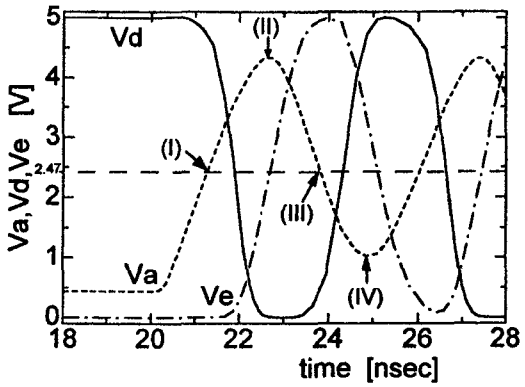


Fig.6 Waveforms in oscillation.

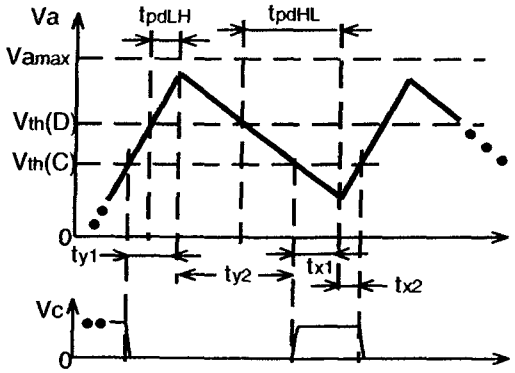


Fig.7 Modeling of circuit operation

The waveform of Va depends on t_r and t_f of Va obtained from the circuits in Fig.8(a) and the propagation delays, t_{pdLH} and t_{pdHL}, of CBlk-ab in Fig.3. In [4], t_r and t_f are defined as the time between P1 and P3, the time between P4 and P6 in Fig.8(b), respectively. However, when oscillation frequency becomes high, Va can not reach Va_{max} and Va_{min} in a short time by the transitions of Ve from L to H and from H to L, respectively. It may lead to estimation of lower oscillation frequency than the true one. Thus, in this paper, t_r and t_f are defined as the followings by means of Sl_1 and Sl_2, which are the slopes of Va at $Va=V_{th}(D)$ defined in Fig.8(b).

$$t_r=(Va_{max}-Va_{min})/Sl_1 \quad (2)$$

$$t_f=(Va_{max}-Va_{min})/Sl_2 \quad (3)$$

where Va_{min} is the final value of Va obtained from the circuit in Fig.8(a) and $V_{th}(D)$ is the threshold voltage of gate D in Fig.3. The values of t_r and t_f are smaller than the ones in [4]. Thus, higher frequency can be estimated by the method than the one in [4].

It is determined whether an FB fault can occur logical oscillation by the same method as in [4] with the parameters. If the following three conditions are satisfied, it is concluded that the FB fault can occur logical oscillation.

The first one is expressed by Eq.(4). Unless it is satisfied, oscillation will not be generated.

$$Va_{min}<V_{th}(D) \quad (4)$$

The second one is expressed by Eq.(5). In order to generate oscillation, Va should become much smaller than the threshold voltage($V_{th}(C)$) of gate C. If it is not satisfied, the change in Va can not be propagated to the output of gate C. Therefore, the following condition should be satisfied besides Eq.(4).

$$Va<V_{th}(C) \quad (5)$$

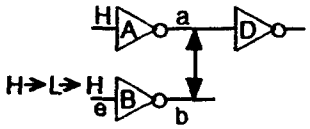
The third condition is one in a time domain. In order for logical oscillation to appear in the output of gate C, Va should be smaller than $V_{th}(C)$ until output logical change of gate C can be generated. The condition is specified by Eq.(6).

$$t_{x1}+t_{x2}\geq t_f(C) \quad (6)$$

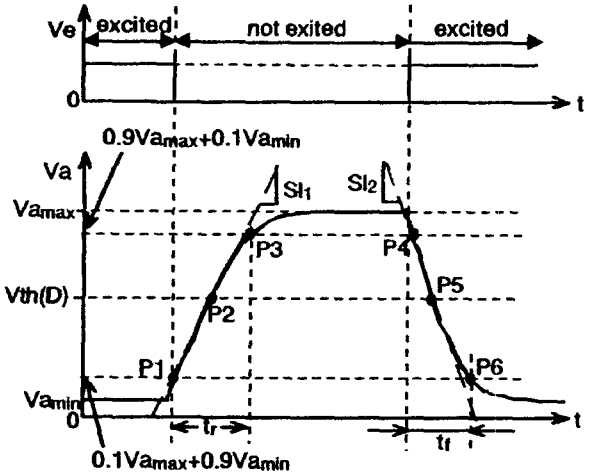
where $t_f(C)$ is rise time of gate C and t_{x1} and t_{x2} in Fig.7 are defined by Eq.(7) and Eq.(8), respectively.

$$t_{x1}=\frac{V_1-V_{th}(D)+V_{th}(C)}{Sl_2} \quad (7)$$

$$t_{x2}=\frac{V_1-V_{th}(D)+V_{th}(C)}{Sl_1} \quad (8)$$



(a) circuit to estimate t_r and t_f



(b)Estimation of t_r and t_b

Fig.8 Estimation of t_r and t_b in our new method

In Eq.(7) and Eq.(8), V_1 is used, which is defined by Eq.(9).

$$V_1=t_{pdHL}\cdot Sl_2 \quad (9)$$

It is apparent from Fig.7 that the minimum period of the generated oscillation, $Tosc_{min}$, can be obtained by Eq.(10).

$$Tosc_{min}=t_{x1}+t_{x2}+t_{y1}+t_{y2} \quad (10)$$

where t_{y1} and t_{y2} are defined by Eq.(11) and Eq.(12), respectively.

$$t_{y1}=\frac{V_2+V_{th}(D)-V_{th}(C)}{Sl_2} \quad (11)$$

$$t_{y2}=\frac{V_2+V_{th}(D)-V_{th}(C)}{Sl_1} \quad (12)$$

$$V_2=t_{pdLH}\cdot Sl_1 \quad (13)$$

The oscillation frequency($fosc_{max}$) is obtained from Eq.(14).

$$fosc_{max}=1/Tosc_{min} \quad (14)$$

5. Experimental Evaluation

Our method is based on piece-linealized model of the

transient behavior in each logic gate and needs circuit simulation for only a small size of circuit in Fig.8(a). Thus, the maximum frequency can be derived by our method in a practically reasonable time.

In order to examine whether the frequency of oscillation can be derived by our method, the oscillation frequency for the circuit in Fig.3 is derived. It depends on the W/L ratios of MOS transistors in gates A and B whether oscillation can occur. Also, the frequency of the oscillation depends on them. Thus, layouts of the circuits having different W/L ratios in gates A and B are designed with ES2 1.2μm CMOS process technology by using MSK[5]. After that, they are converted into SPICE files, in which parasitic capacitors between any two layers in the layout are included. The obtained SPICE files are simulated with PSPICE. From the simulation results, the frequency of oscillation f_S is obtained and is compared to the ones obtained by our previous method proposed in [4] and new one. The results are shown in Table 1.

Table 1 Experimental results.

W/L ratio				Estimated freq. [MHz]			Generated oscilation
gate A		gate B		SPICE	Prev. method	New method	
pMOS	nMOS	pMOS	nMOS	fs	fe	fe'	
20/1	5/1	5/1	5/1	—	—	—	No
5/1	5/1	15/1	5/1	—	—	—	No
5/1	3/5	5/1	5/1	537.98	461.40	686.56	Nonlogical
16/1	5/1	5/1	5/1	802.87	750.60	943.27	Nonlogical
5/1	5/1	25/1	5/1	538.43	564.28	658.98	Nonlogical
7/1	5/1	5/1	5/1	667.54	884.53	977.22	Logical
5/1	1/2	5/1	5/1	472.46	524.03	751.54	Logical
5/1	5/1	5/1	20/1	609.53	665.35	704.92	Logical
5/1	5/1	35/1	5/1	587.45	565.19	593.10	Logical

In the result of the 9-th experiment, smaller frequency is estimated by our previous method than the one obtained by SPICE simulation. It means that the fault may not be detected by measuring the voltage at the signal line c at the estimated frequency. On the other hand, as shown in Table 1, by using our method, larger frequency can be estimated than the one obtained by SPICE simulation in all of the experiments. It leads that by measuring output voltage of each primary output terminal per T_{smp} obtained by our new method, all of the FB faults can be detected.

6. Conclusion

In this paper, an estimation method of the maximum frequency of oscillation, which is generated by feedback bridging faults, is proposed. The frequency is indispensable for detecting feedback bridging faults in logic circuits. The method is evaluated by some experiments. The experimental results show that higher frequency than the one obtained by Spice simulation can be estimated by the method. The method is based on piece-linealized models. Thus, the frequency can be derived with small computational cost. Since there are a lot of feedback bridge faults in a large size of circuit, it is expected that our method is effective for estimating the maximum frequency of oscillation and also for detecting the faults.

References

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