A BANDWIDTH VARIABLE DIGITAL CHIRP GENERATOR FOR RADAR ALTIMETER

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Abstract -- This paper concerns the design and implementation of a Bandwidth Variable Digital Chirp Generator (DCG) for the radar altimeter. A double SRAM parallel structure is used to breakthrough the upper DCG bandwidth limited by the highest clock frequency of the digital chips. An experimental system working in the waveform storage method has been implemented. We show that the bandwidth changed according to the radar altimeter's requirement and the design released the stringent speed requirement of the chips for making a variable wide bandwidth DCG.

Keywords: Bandwidth Variable Digital Chirp Generator; DCG; the radar altimeter

1. Introduction

The radar altimeter operates in the pulse width limited mode, and uses the full deramp system of pulse compression. It is an active microwave instrument that transmits the linear FM Chirp pulses with a fixed frequency [5].

By processing of the radar echo signal, a curve (called waveform) was indicated as the convolution of three terms by BROWN in 1977 [3]:

$$W(t) = P(t) * Q(t) * S(t) \qquad (1)$$

where t is the propagation time. $W(t)$ is the echo's mean power. It depends on the altimeter features and the sea surface parameters. $P(t)$ is the average flat surface impulse response, $Q(t)$ is related to the sea surface height probability density, and $S(t)$ is the altimeter point target response.

The major purpose of the altimeter signal processing is to estimate the altitude above the sea, the sea wave height, and the sea reflectivity of the radar signals information from the received waveform. The signal processing results can be used to update the tracking loop and to select a different Chirp bandwidth for changing the radar resolution. The variable bandwidth characteristic makes the radar altimeter freely to explore ocean, sea ice, coastal zones, and land [5], [9]-[10] when necessary.

Linear FM Chirps can be generated by many methods. They have been traditionally generated by means of Surface Acoustic Wave (SAW) devices or others with the analog method. As the analog method could not reach a high linearity requirement, the digital Chirp generators have been used in the present time.

This paper concerns a bandwidth variable DCG design for the second generation China Multimode Microwave Remote Sensor (CMMRS)[5]. This design released the stringent speed requirement of the chips and has basically met the CMMRS requirement.

2. The linear FM Chirp

The linear FM Chirp waveform has a sinusoidal shape. Its frequency changes linearly over time. Its expression is:

$$f(t) = A \bullet rect(t/T) \bullet \cos(\omega_0 t - \pi\kappa t^2) \quad t \in [-T/2, T/2] \quad (2)$$

where

$$rect(t/T) = \begin{cases} 1, & -T/2 \le t \le T/2 \\ 0, & \text{others} \end{cases}$$

$rect(t/T)$ a rectangular pulse of duration T;

A the pulse amplitude;

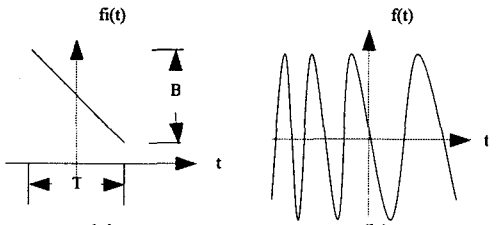
$\omega_0 = 2\pi f_0$ the carrier angular frequency;

$\kappa = B/T$ the chirp rate related to the pulse bandwidth B;

T the pulse width;

t the sampling interval.

and its waveform is:



(a) (b)

Fig. 1 (a) carrier frequency - time dependence
(b) linear FM Chirp waveform

3. Frequency Synthesis method

The frequency synthesis method generates one or more new frequencies with a single frequency or some reference frequencies. It includes the conventional Direct Frequency Synthesis, Indirect Frequency Synthesis (or called phase-lock-loop), and Direct Digital Frequency Synthesis methods [1], [2], [6], [8], [11]. There are two digital methods to generate the Chirp waveform. One is Direct Digital Synthesis (DDS) method and another is Waveform Storage method.

3.1 Direct Digital Synthesis method

The basic DDS architecture [6], [8] is given in Fig. 2.

In Fig. 2, $\Delta\theta$ is an input frequency control word and f_{clk} is used to establish a stable sampling time. The new phase is calculated by

$$\theta_{k+1} = \theta_k + \Delta\theta \quad (3)$$

where θ_{k+1} the new phase;

θ_k the previous phase.

The accumulator changes at each sampling time. The data in the accumulator will be reset after one period and then the new procedure will start again. The SINE table includes the digitized sine wave samples in one period. The result of the accumulator addresses the SINE table to determine a suitable amplitude value and then feeds to a D/A converter (DAC) to get the output f_{out}. A low-pass filter at the DAC output may be used to eliminate the alias frequency component. When $\Delta\theta$ is fixed, the output is a fixed frequency. If we want to get the Chirp signal, we need to add another frequency accumulator before the phase accumulator. The basic Direct Digital Chirp Synthesis (DDCS) architecture is given in Fig. 3.

3.2 Waveform Storage method

The basic diagram of the waveform storage method is given in Fig. 4. The calculated value is stored in the memory. At each sampling time, the circuit will use an address counter to generate the necessary address to orderly readout the stored sampling data and then send each of them to the DAC. It is the easiest way to obtain the Chirp waveform.

4. System Design

This linear FM Chirp generator is specially designed for the second generation CMMRS. As the bandwidth and pulse width have been relatively fixed, we decide to use the waveform storage method to generate the necessary Chirp signal in our design. It can neatly assist us to adjust the waveform to compensate the Chirp signal to become better. This is the best way to meet the CMMRS requirement.

The CMMRS requires several different but fixed

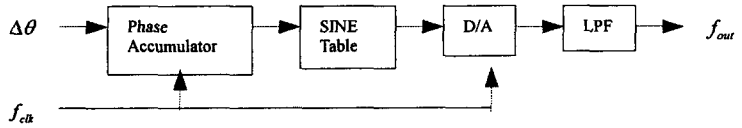


Fig. 2 The block diagram of the Direct Digital Synthesis method

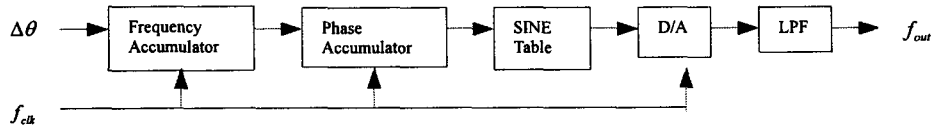


Fig. 3 The block diagram of the Direct Digital Chirp Synthesis method

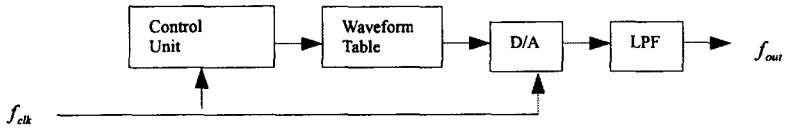


Fig. 4 The block diagram of the Waveform Storage method

bandwidths. We will discuss in the following on how to design a DCG and how to make its bandwidth variable. The main problem is how to get a relatively wide bandwidth based on the limited speed of the chips.

4.1 Reduce the D/A conversion frequency

According to the expression of the Chirp waveform in Eq. (2), the highest frequency is $f_0 + B/2$. The sampling frequency f_{clk} is at least $f_{clk} \geq 2(f_0 + B/2)$ by Nyquist.

If the carrier frequency f_0 is at the range of intermediate frequency, f_{clk} will become very high. We generate In-phase (I) and Quadrature (Q) signals as the base band signals. These two signals are modulated at the carrier frequency f_0 by the $I\&Q$ modulator. If the base band bandwidth is $B/2$, f_{clk} reduces to $f_{clk} \geq B$.

The expression of I and Q are

$$I = \cos(\pi\kappa t^2) \text{ and } Q = \sin(\pi\kappa t^2) \quad (4)$$

then the $I\&Q$ modulator's output is

$$\cos(\pi\kappa t^2)\cos(2\pi f_0 t) + \sin(\pi\kappa t^2)\sin(2\pi f_0 t)$$
$$= \cos(2\pi f_0 t - \pi\kappa t^2) \quad (5)$$

The parameters definition and the result of the $I\&Q$ modulator are the same as the Chirp waveform in Eq. (2). This method has been used to reduce the D/A conversion frequency in this radar altimeter. We plot the basic DCG diagram in Fig. 5. It will be called as the single SRAM method later in this paper.

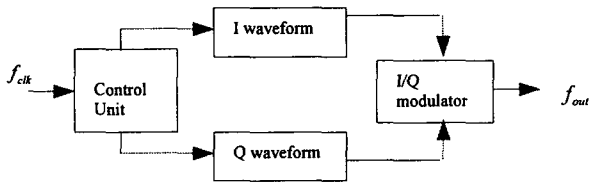


Fig. 5 Chirp generation diagram

4.2 The lower speed requirement of the digital chips

The upper bandwidth of the DCG is limited by the highest speed of the chips. A double SRAM parallel structure (called the double SRAM method) is used in our design (Fig. 6). The odd number and even number of the waveform sampling points are separately stored into the double SRAM. We use $f_{clk}/2$ to alternately select the double SRAM and synthesis the outputs into one way. The highest speed of the digital chips will be $f_{clk}/2$

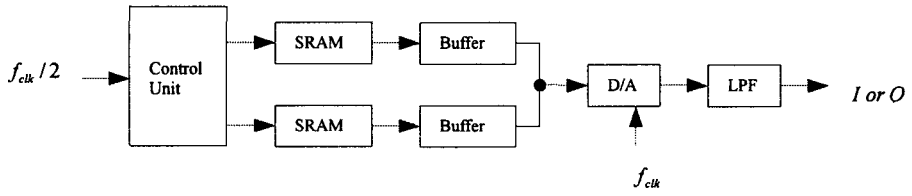


Fig. 6 A double SRAM parallel structure

instead of f_{clk} to generate the Chirp waveform with the same bandwidth. Therefore the double SRAM method can release the stringent speed requirement of the digital chips.

This method can be also used to breakthrough the upper bandwidth limited by the highest sampling frequency of the digital chips. Let's assume that the highest speed of the digital chips is f_{clk}, and the bandwidth is B_b. If the digital chip's speed and the D/A conversion's speed are $f_{clk} = 4B_b$ with the single SRAM method, the bandwidth is $f_{clk}/4$. If we use the double SRAM method, the bandwidth will be $f_{clk}/2$.

One more application of the double SRAM method is to double the sampling density of the Chirp waveform. It can increase the quality of the Chirp signal.

4.3 Bandwidth Variable method

This DCG need to change bandwidth in real-time at the same pulse width. There are two methods to get variable bandwidths. We will use the one easy to implement.

The first method uses different sampling frequency to control the address counter to get the different bandwidths. A Chirp signal has the time-bandwidth product is TB and its sampling frequency is f_{clk}. When we use f_{clk}/n clock frequency to control the same address counter, the Chirp signal's pulse width and bandwidth will be nT and B/n. The time-bandwidth product does not change. Using this method, we can store a series of data at the biggest bandwidth. Other B/n bandwidths can be got by different sampling frequencies.

The second method is to calculate the waveform data for the different bandwidths at the same pulse width. This method uses more memory space but only requires one address control. In our design, we used this method We stored the waveforms into the different memory locations, and got the results by controlling the starting and ending addresses.

5. Key Factors in the system

In order to obtain a high quality DCG, the following errors and noises must be considered and kept reasonably small [1], [4], [6]-[8].

The data stored in SRAM are a series of the finite word-length samples. A long word-length results in a small truncation error.

The DAC is an important part in any Chirp generators. It is difficult to make a perfect DAC. The major reasons are finite bit resolution, nonlinearity and glitches (or transient effects) in the DACs. The more conversion bits, the more output resolution of a DAC we can have. We have to consider about bit resolution, accuracy, settling time, and so on.

The $I\&Q$ modulator is also the key technique to generate the Chirp waveform. In order to get the nice Chirp waveform, we need to take care about several major criteria of the $I\&Q$ modulator: carrier rejection, sideband rejection and harmonic suppression.

We use 8 bits SRAM and 12 bits DAC here. The carrier and sideband rejection of the $I\&Q$ modulator are higher than 40dB.

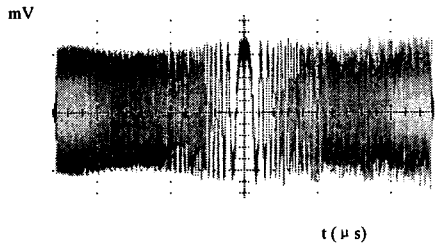


Fig. 7 I waveform in time domain

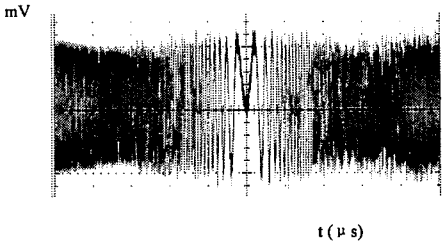


Fig. 8 Q waveform in time domain

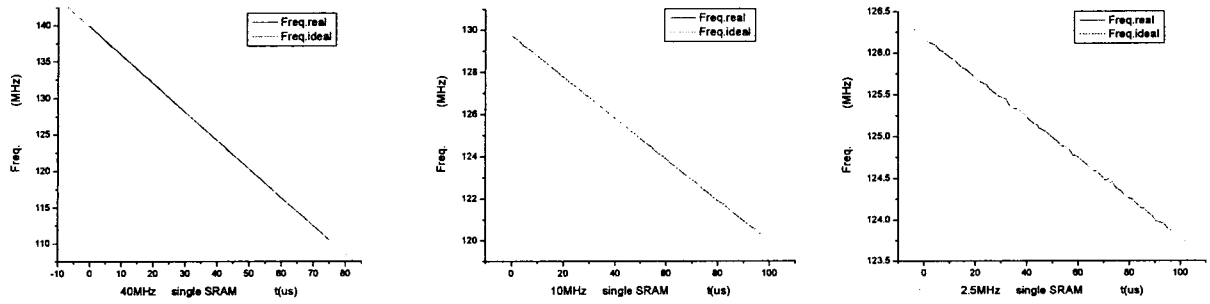


Fig. 9 The frequency linearity with single SRAM method

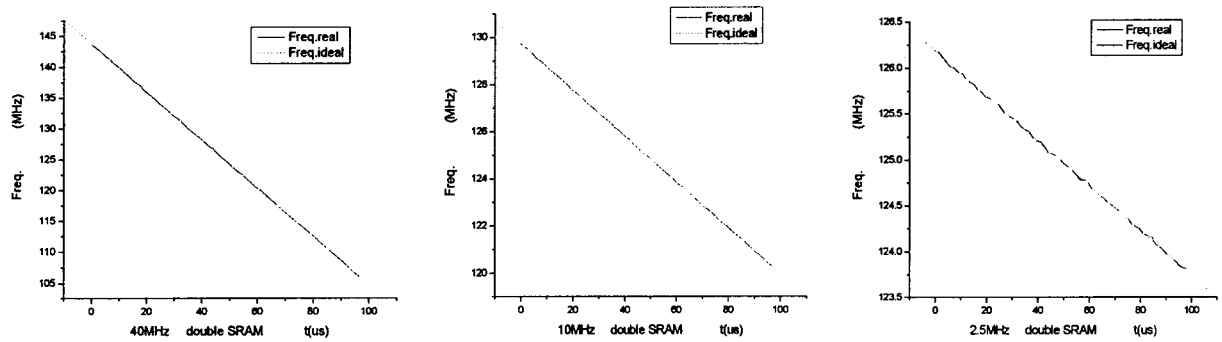


Fig. 10 The frequency linearity with double SRAM method

6. System implement and testing

According to the requirement of the second generation CMMRS and the scheme of this design, we carefully considered about the chips selection, the circuit design, and the PCB design. A FPGA chip is used to be the center control unit here.

We tested the properties of this design. The result shows that the signal-to-noise ratio in frequency domain is about 45dB. The basic I and Q time domain waveforms are shown in Fig.7 and Fig. 8. We have also changed this design slightly into a single SRAM method generator and kept the same quantity of the sampling points. It makes us easy to compare the properties of the single and double SRAM methods.

In our design, there are three bandwidths: 40MHz, 10MHz and 2.5MHz. The bandwidth can be changed when necessary. We compare the frequency linearity of the single and double SRAM methods in the following. The frequency linearity is equal to 0.99998, 0.99996 and 0.99974 for 40MHz, 10MHz and 2.5MHz bandwidths with the single SRAM method (Fig. 9). It is equal to 0.99996, 0.99995 and 0.99979 for 40MHz, 10MHz and 2.5MHz bandwidths with the double SRAM method (Fig.

10).

The testing result shows that the double SRAM method has the same frequency linearity as the single SRAM method. Preliminary results are very encouraging. As the double SRAM method will generate more harmonic than the single SRAM method, its spectrum is not so smooth compared with the single SRAM method. We will improve our design further in the future.

As we have known, the digital frequency synthesis method has two restrictions: the operating speed limited by the sampling theory and the problem on spectral purity. The double SRAM method can be used to increase the bandwidth, release the operating speed or increase more sample points at the same bandwidth to make spectral purity as better as possible.

7. Conclusion

The digital frequency synthesis method has many advantages. It has a high mobility, a high stability, and a high linearity. It is easy to change or improve and easy to control. In our design, we show that the bandwidth changed according to the radar altimeter's requirement and this design released the stringent speed requirement of the chips for making a variable wide bandwidth DCG.

8. References

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November 1, 2002 (Friday)

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