WLP and New System Packaging Technologies

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Abstract

The Wafer Level Packaging is one of the most important technologies in the semiconductor industry today. Its primary advantages are its small form factor and low cost potential for manufacturing including test procedure.

The CASIO's WLP samples, application example and the structure are shown in Fig.1, 2&3.
There are dielectric layer, under bump metal, re-distribution layer, copper post, encapsulation material and terminal solder.
The key technologies are "Electroplating thick copper process" and "Unique wafer encapsulation process".
These are very effective in getting electrical and mechanical advantages of package. (Fig.4)

CASIO and CMK are developing a new System Packaging technology called the Embedded Wafer Level Package (EWLP) together.
The active components (semiconductor chip) in the WLP structure are embedded into the Printed Wiring Board during their manufacturing process.

This new technical approach has many advantages that can respond to requirements for future mobile products.
The unique feature of this EWLP technology is that it doesn't contain any solder interconnection inside. In addition to improved electrical performance, EWLP can enable the improvement of module reliability. (Fig.5)

The CASIO's WLP Technology will become the effective solution of "KGD problem in System Packaging". (Fig. 6)

The EWLP sample shown in Fig.7 including three chips in the WLP form has almost same structure with SoC's.

Also, this module technology are suitable for RF and Analog system applications. (Fig. 8)

Contents

- WLP Technology
  - Structure
  - Features
  - Process
  - Applications
- EWLP Technology
  - Concept
  - Advantages
  - Applications
- Conclusions & Discussions

Profile

Takeshi WAKABAYASHI

- Joined CASIO Computer Company in 1980.
- Ten years of experience with the CMOS Semiconductor process development.
- Developed Wafer Bumping Process and launched volume production at CASIO MICRONICS (one of CASIO's subsidiaries).
- Conducted development of High Density Assembly Technologies for advanced mobile products.
- Developing Next-generation Wafer Bump Technologies (WLP) and System Integration Technologies (EWLP).
- General Manager of Advanced Packaging Technology Department, Core Technologies R&D Division /CASIO COMPUTER CO., LTD.
- Board of Director /CASIO MICRONICS CO., LTD.
- A member of the Electronic System Integration Technical Committee /Japan Electronics and Information Technology Industries Association.

Figure 1.

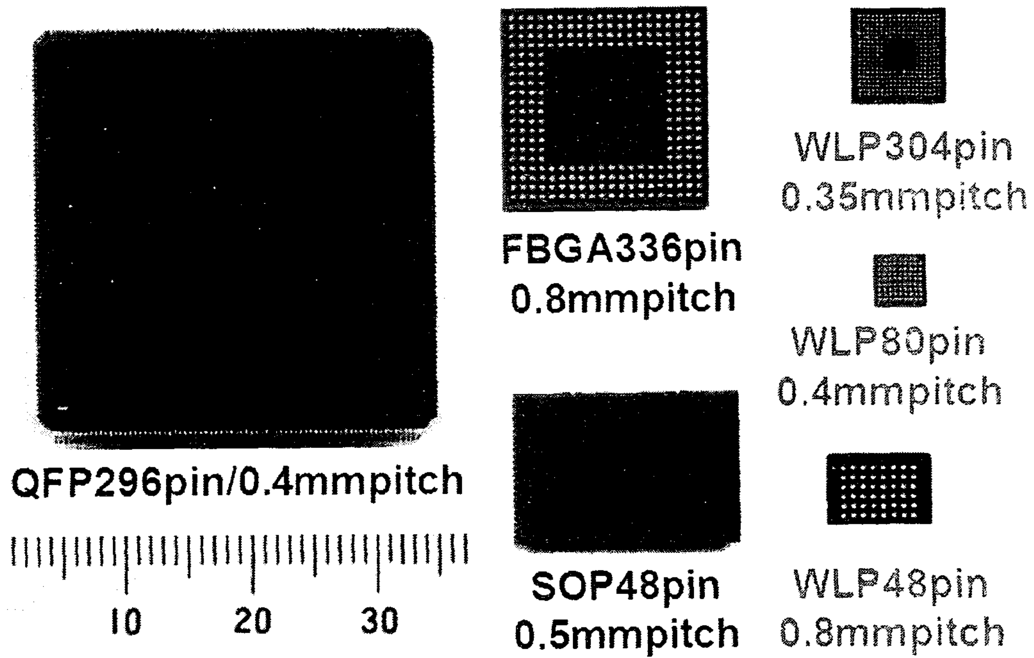


Figure 2.

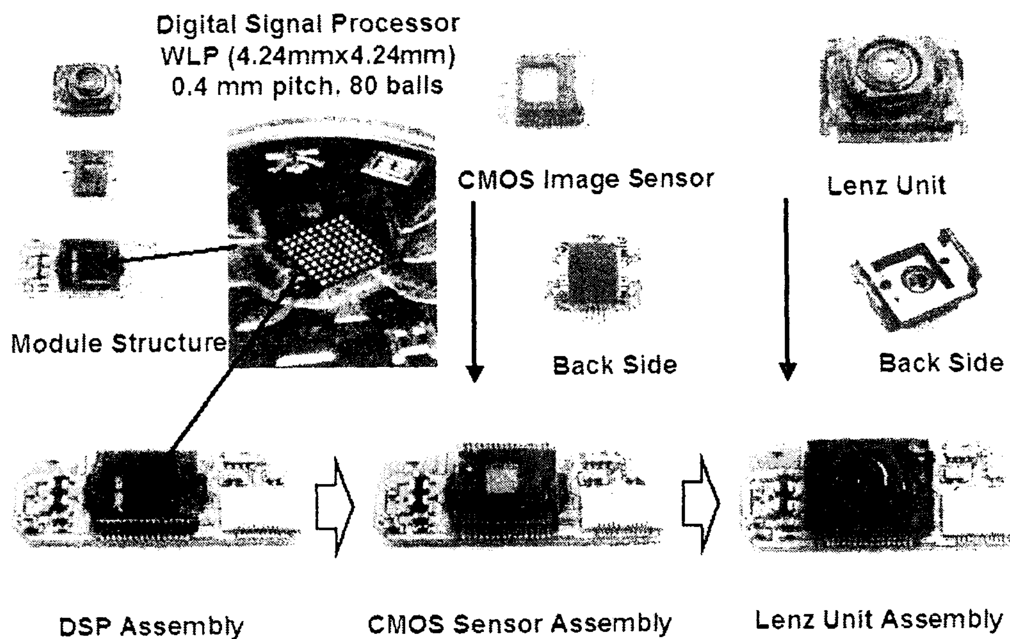


Figure 3.

Partial Cross Sectional View of WLP

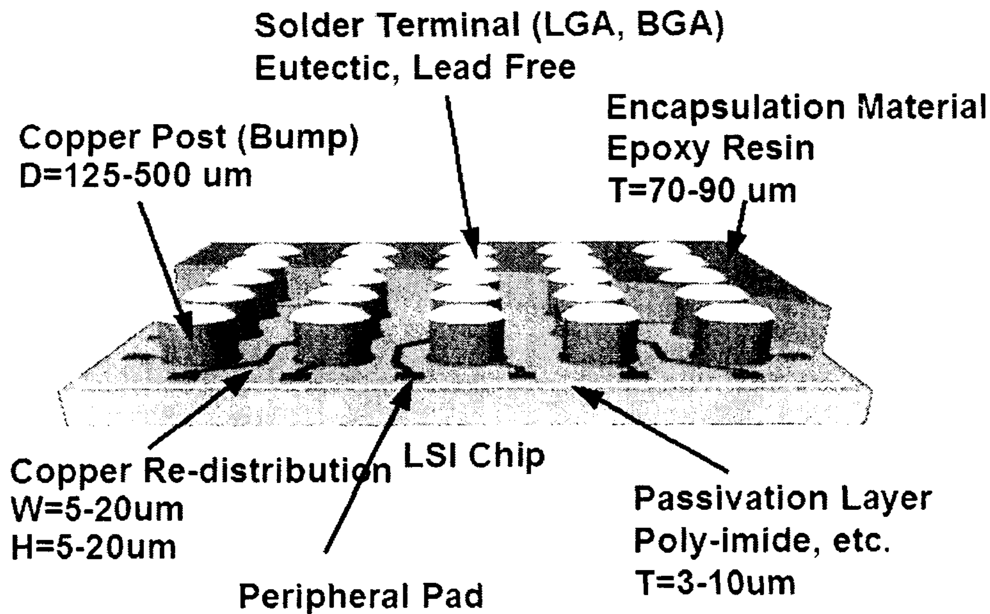


Figure 4.

Advantages of CASIO'sWLP

- **Basic Characteristic WLP**
  - Advanced Encapsulating Process (US PAT.) & Material
  - High Yield, Performance and Reliability
  - Easy to use
  - 300mm Wafer Processing

SMT Compatible
Perfect Protection
High Productivity

- **Low Cost Solution for Test Process**
  - Handling Cost
  - Wafer Level B/I Cost

Reliable Low Cost Contact
Protect from Mechanical Damage

- **EWLP Solution**
  - High Performance Module

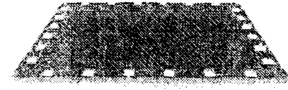
High Performance System
Solder Less Assembly

- **Stress Buffer (Leading-Edge Semiconductor)**
  - 90nm, 65nm, 45nm
  - Low-k Material

Figure 5.

Bare Die vs. WLP for Embedded Process

Bare Die Issue
- KGD Issue (Good Die ?)
- Finer Pad Pitch
- Semiconductor Pad Material
- Difficulty of Process Technology
- Imperfect Reliability



Advantages of WLP Embedded
- Easy Test and Wafer Level B/I
- Design Flexibility from WLP Re-distribution
- Copper Terminal Finish
- Perfect Protection
- High Reliability

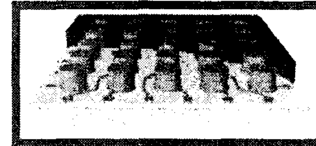


Figure 6.

CASIO's WLP

WLP = KGD Solution

- •SMT package
- •Flip Chip Module
- •EWLP Module

EWLP = Embedded Wafer Level Package

Figure 7.

EWLP Module (Multi WLP)

- ■High Performance Digital Processor Module
  - ●High Speed Signal
  - ●Bus Line
- ■Equivalent to System LSI
  - ●Form Factor
  - ●Plane Structure
- ■Copper Interconnect
  - ●High Performance
  - ●Solder Free

System LSI-Like Structure

EWLP Module
(EWLP Structure)

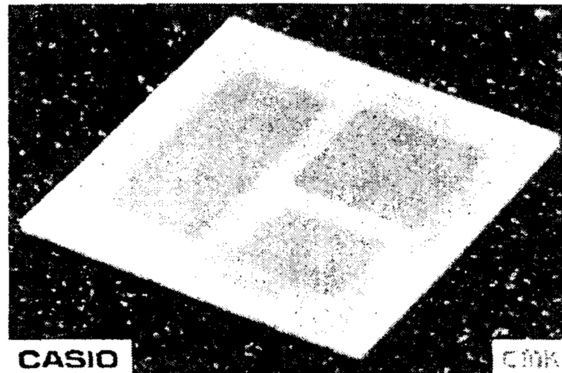


Figure 8.

EWLP, WLP & Passive Integrated Module

Passives are mounted on EWLP Terminal Side or the other Side

- ■By Conventional SMT
- ■EWLP, WLP and Passive
- ■Flexibility of Mounting Passives Devices
  - ●Analog, RF
- ■RF Module Application
  - ●GSM, CDMA
  - ●Bluetooth
  - ●RF LAN
  - ●GPS
  - ●Digital TV Tuner

RF Module Mechanical Sample