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완전 결핍 SOI MOSFET의 계면 트랩 밀도에 대한 급속 열처리 효과

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Effect of rapid thermal annealing on interface trap density by using subthreshold slope technique in the FD SOI MOSFETs

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Abstract

In this presentation, we investigated the abnormal subthreshold slope of the FD SOI MOSFETs upon the rapid thermal annealing. Based on subthreshold technique and C-V measurement, we deduced that the hump of the subthreshold slope comes from the abnormal D_{it} distribution after RTA. The local kink in the interface trap density distribution by RTA drastically degrades the subthreshold characteristics and mini hump can be eliminated by S-PGA.

I. Introduction

The fully depleted (FD) silicon-on-insulator (SOI) metal-oxide-semiconductor field effect transistors (MOSFETs) are the promising device structure for low-voltage, low-power, and high-speed applications in sub-50 nm regime [1-2]. Beside the immunities to short channel effect, radiation damage, and latch-up in complemental MOS technology, FD SOI MOSFETs present an ideal subthreshold slope about 60 mV/dec. at room temperature [2-3]. The subthreshold slope is an important parameter for low-voltage, low-power applications because the subthreshold region describes how the switch turns on and off [4].

The rapid thermal process (RTP) is a major annealing technology that replaces a number of the conventional furnace process due to low thermal budget and less turnaround time. The RTP is used for activation and redistribution of the implanted dopants, formation of the silicides, and reflow of dielectric layers [5]. However, the rapid rise and fall of temperature, which is inherent feature of the RTP, is known to affect the Si-SiO_2 interface properties, which play a central role in performances of MOSFET [6].

In this work, we report the abnormal behavior of subthreshold slope of the FD SOI MOSFETs upon the RTP. Based on subthreshold technique and C-V measurement, we deduced that the hump of the subthreshold slope comes from the abnormal D_{it} distribution after RTA. To evaluate this hypothesis, we compared the subthreshold slope of MOSFET upon RTA and and subsequent post gate annealing (S-PGA) in conventional furnace.

II. Experiments and Results

The edgeless FD SOI MOSFETs were prepared from (100) oriented, 14 ~ 22 Ω·cm, boron-doped SOI wafers (SOITECH) and the corresponding doping concentration is about 1.0×10^{15} cm^{-3}. The thickness of top Si layer and BOX are 90 nm and 200 nm, respectively. The active area was defined by mesa-isolation technique and the sharp corners of active edge were rounded using CF_4/Ar RIE. The gate oxide was thermally grown to the thickness of 5 nm and the gate electrode was the highly P-doped n-type polycrystalline silicon. The gate length was 2 μm and the width was varied from 20 to 2 μm. The source and drain were doped by phosphorus plasma doping and activated by RTA at the temperature of 850°C. Some devices were followed by S-PGA at 750°C for 5 min in conventional furnace in N_2 atmosphere and quenched slowly to room temperature. Then, Al contact electrode was deposited by thermal evaporation and no forming gas annealing was performed.

For C-V measurement, MOS capacitors were fabricated on bulk Si of the same doping concentration as SOI with area of $110\times110\ \mu m^2$.

It is required to extract D_{it} from slope at back bias, where the back interface is beginning to accumulate, due to a back accumulation layer effect [7]. Fig.1 shows the dependence of front gate threshold voltage with back bias. From Fig. 1, the back interface accumulation initiates at V_{G2} of –4.5 V. Fig. 2 shows the current-voltage characteristics and corresponding subthreshold swing of FD SOI MOSFETs at V_{G2} = –4.5 V and drain voltage of 0.05 V. The threshold voltage and minimum swing are 510 mV and 94.07 mV/dec. for devices upon RTA, and 180 mV and 89.94 mV/dec. for that followed by S-PGA, respectively. As depicted in Fig. 2, both MOSFETs with PGA and S-PGA start to flow current at the gate voltage of –0.5 V with the same value. However, after V_{G1} = 0 V, the subthreshold current of RTP annealed sample is severely degraded to orders of magnitude, as compared with that of S-PGA device. The corresponding subthreshold swings appear in Fig. 2. The swings are about 200 mV/dec. for devices upon RTA and 100 mV/dec for that upon S-PGA, respectively and increase rapidly when the applied gate voltage is larger than threshold voltage.

In FD SOI MOSFETs, where thickness of thin film Si is larger than twice of the maximum depletion width ($t_{Si} < 2x_{dmax}$), the surface potentials at gate oxide/Si and BOX/Si interfaces, ϕ_{s1} and ϕ_{s2}, are modulated by the front and back gate voltage, V_{G1} and V_{G2}, respectively [3]. When back interface is accumulated, i.e., $\phi_{s2} = 0$, the applied front gate voltage is given by

$$V_{G1} = V_{FB1} + \phi_{s1}\left(1 + \frac{C_{itf} + C_{Si}}{C_{oxf}}\right) + \frac{Q_{depl}}{2C_{oxf}} \quad (1)$$

, where V_{FB1} is the flat band voltage of the front interface and C_{oxf}, C_{Si}, and C_{itf} are the gate oxide (ε_{ox}/t_{oxf}), the thin film Si (ε_{Si}/t_{Si}), and the front interface trap (qD_{it}) capacitances per unit area, respectively and Q_{depl} is the charge per unit area due to the depleted impurities in the SOI film.

The front oxide interface trap density can be extracted from the subthreshold slope with the back interface accumulation (S_{acc}) [7].

$$D_{it} = \frac{1}{q}\left[\left(\frac{S_{acc}}{(kT/q)\ln 10} - 1\right)C_{oxf} - C_{Si}\right] \quad (2)$$

, where S_{acc} is $dV_{G1}/d(\log I_d)$ and I_d is drain current.

The surface potential ϕ_{s1} is calculated from the difference of (1) and the front threshold voltage, $V_{th,1}^{A}$ when the back interface is accumulated.

$$\phi_{s1} = (V_{G1} - V_{th,1}^{A})/\left(1 + \frac{C_{itf} + C_{Si}}{C_{oxf}}\right) + \phi_{s,th} \quad (3)$$

, where $\phi_{s,th}$ is the front surface potential at the threshold voltage, typically 2 times Fermi potential Φ_F. According to (3), the effect of C_{itf} on ϕ_{s1} cannot be ignored, when C_{itf} is the same or higher order of C_{oxf} and varied with gate voltage. By incorporating the value of C_{itf} obtained from (2) to (3), surface potential is determined with regard to V_{G1}.

$$\phi_{s1} = (V_{G1} - V_{th,1}^{A}) \times \frac{\ln 10 \times (kT/q)}{dV_{G1}/d(\log I_d)} + \phi_{s,th} \quad (4)$$

Fig. 3 shows the interface trap densities for FD SOI MOSFETs, obtained through the subthreshold slope method given by (2) and (4) and that for MOS capacitors, determined

through HF/QS C-V measurement. It is generally known that RTA significantly increases local Si/SiO_2 interface trap density at surface potential in vicinity of center of weak inversion and can be eliminated by following furnace annealing [5-6, 8]. The D_{it}s obtained by the subthreshold slope technique show the effect of RTA and furnace annealing on interface property and match well with that from C-V measurement, although D_{it}s by subthreshold method are slightly larger than those of the capacitors. The differences of D_{it}s between MOSFETs and MOS capacitors are thought to be due to low thermal conductivity of SOI, when stressed with RTA [3]. The measured D_{it}s are order of 1×10^{13} and 1×10^{12} $eV^{-1}cm^{-2}$ for samples with RTA and S-PGA, respectively. In addition, local peak in the interface trap density can significantly distort the I_d-V_g characteristics in MOSFETs. As depicted in Fig. 4, the subthreshold 'mini' hump appears, which is different from edge-related subthreshold hump, i.e., the parasitic edge transistor effect [9], in I_d-V_g curve of FD SOI MOSFETs upon RTA. The subthreshold 'mini' hump can be eliminated by subsequent low temperature S-PGA in conventional furnace, as appeared in Fig. 4.

III. Conclusion

In this work, we report the abnormal behavior of subthreshold slope of the FD SOI MOSFETs upon the RTP. Based on subthreshold technique and C-V measurement, we deduced that the hump of the subthreshold slope comes from the abnormal D_{it} distribution after RTA. The local kink in the interface trap density distribution by RTA drastically degrades the subthreshold characteristics and mini hump can be eliminated by S-PGA.

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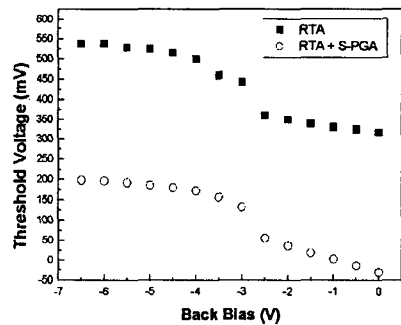

Fig. 1. The front gate threshold voltage shift with back bias in FD SOI MOSFETs annealed with RTP and S- PGA.

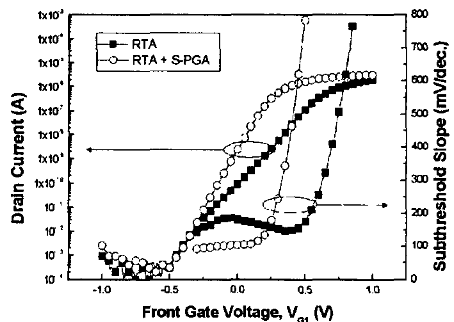

Fig. 2. The I_d-V_g curve and swing of FD SOI MOSFETs as a function of V_{G1} at V_{G2} of –4.5 V and V_d of 0.05 V.

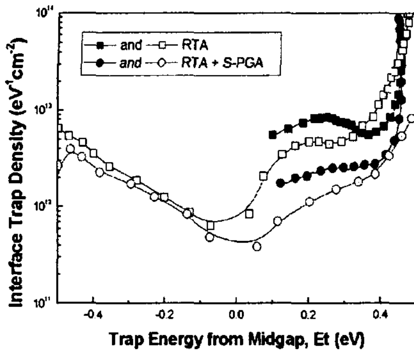

Fig. 3. The D_{it} distribution of gate oxide for FD SOI MOSFETs. The closed symbols represent the trap density through subthreshold slope method and the open symbols represent that for C-V measurement.

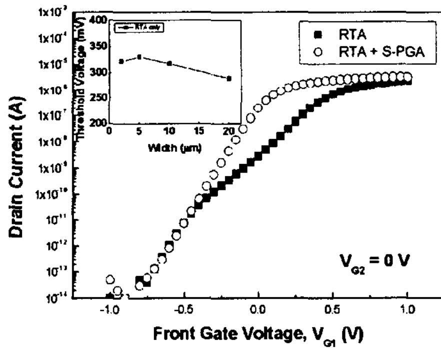

Fig. 4. The I_d-V_g curve of FD SOI MOSFETs at V_{G2} = 0 and V_d = 0.05 V. The inset shows threshold voltage variation as a function of channel width.