Erbium 실리사이드를 이용하여 제작한 *n*-형 쇼트키장벽 관통트랜지스터의 전기적 특성

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Characteristics of Erbium silicided *n*-type Schottky barrier tunnel transistors

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Abstract

The theoretical and experimental current-voltage characteristics of Erbium silicided *n*-type Schottky barrier tunneling transistors (SBTTs) are discussed. The theoretical drain current to drain voltage characteristics show good correspondence and the extracted Schottky barrier height is 0.24 eV. The experimentally manufactured *n*-type SBTTs with 60 nm gate lengths show typical transistor behaviors in drain current to drain voltage characteristics. The drain current on/off ratio is about 10^5 at low drain voltage regime in drain current to gate voltage characteristics.

Introduction

Recently, many experimental studies on the current-voltage characteristics for the Schottky barrier tunnel transistors (SBTTs) were reported [1]-[5]. In SBTTs, the impurity doped regions for source and drain are replaced by silicide regions, which behave as metal. Moreover, the structure is quite simple and the ultra shallow junction can be formed easily and accurately, since the junction depth is controlled by the deposited metal thickness and annealing temperature. Thus, SBTTs have been proposed as an alternative to the conventional metal-oxide-semiconductor field-effect transistors (MOSFETs) for sub-100 nm application. Recently, the leakage current of SBTTs, manufactured on the bulk silicon, was significantly suppressed [1]. SBTTs on thin body silicon-on-insulator (SOI) have been reported which has the 15 nm and 20 nm channel length, for *n*-type and *p*-type SBTTs, respectively [2]. But most of the experimental works were done in *p*-type SBTTs, especially by using Platinum silicide [1], [3]-[5]. Also, there were many theoretical efforts to describe the current transport mechanism in SBTTs, which have different physical mechanisms with conventional MOSFETs, i.e., tunneling through the Schottky barrier exists in silicon/silicide interface [6]-[10]. But most of the previous theoretical results were not incorporated with experimental results.

Modeling of SBTTs

Carrier transport of *n*-type SBTTs at the Schottky barrier can be modeled by a combination of the thermionic emission current I_{TH} and the tunneling current I_{TN}. The current in the channel region can be expressed by applying the classical

MOSFETs model. To satisfy the current continuity condition, the sum of two components I_{TH} and I_{TN} should have the same value with the channel current I_{CH}.

$$I_{CH} = I_{TH} + I_{TN} \quad (1)$$

By using the simple boundary condition in (1) the current-voltage characteristics of SBTTs can be described [6].

Fig. 1 shows the simulated drain current as a function of the drain voltage in n-type SBTTs. The gate voltage is 1 V. The gate length is chosen as 1 ㎛ to remove the short channel effect. The saturation current increases as the barrier height decreases, which implies the increased tunneling current due to the low Schottky barrier height. As the barrier height increases, the drain current raises slowly with the drain voltage because the higher field is needed to tunnel the higher and thicker Schottky barrier. The suppression of drain current in low drain voltage can be found in previous experimental results [1]-[5].

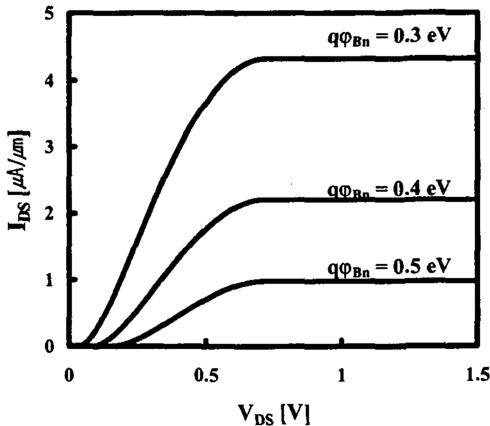

Fig. 1. Drain current versus drain voltage characteristics of n-type SBTTs with various Schottky barrier heights of electron. The electrical gate oxide thickness is 3 nm and gate flatband voltage is assumed as –0.3 V. The threshold voltage of channel region (V_{BT}) is 0.3 V and the mobility at low field (μ_0) is 650 $cm^2/V \cdot sec$. The doping concentration of p-substrate is 1.0×10^{15} cm^{-3} and the temperature is 300 K.

Fig. 2 shows the drain current as a function of the gate voltage. As the barrier height increases from 0.3 to 0.5 eV, the tunneling current begins to flow at higher gate voltage. The off-current of SBTTs is determined by thermionic current and the on-current by tunneling current. This is confirmed in the numerical simulation, by dividing the drain current (I_{DS}) with I_{TH} and I_{TN} components. The ratio I_{TN}/I_{TH} is about 10^8 when the barrier height is 0.5 eV and gate voltage is 2.0 V and the ratio I_{TN}/I_{TH} is nearly zero in the plateau region. Although the barrier height is 0.3 eV, the tunneling current begins to flow around the 0.5 V gate voltage. It is not desirable to dope the channel region to control the threshold voltage of SBTTs because the doping can significantly degrade the Schottky diode characteristics [11]. Finally, the threshold voltage of SBTTs can be lowered by adopting metal instead of polycrystalline silicon as gate electrode material. The metal electrode bends the silicon conduction band downward and closer to Fermi level because of the work function difference between metal and silicon.

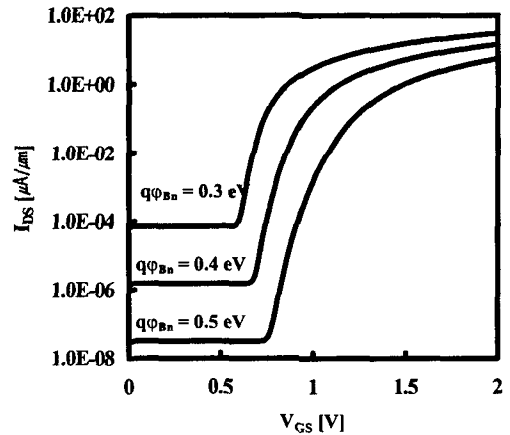

Fig. 2. Drain current versus gate voltage characteristics of SBTTs with various Schottky barrier heights of electron. The parameters used for calculation are the same as those used in the Fig. 1.

Experimental and discussion

The <100> p-type silicon-on-insulator (SOI) wafer is used to manufacture Erbium silicided n-type SBTTs. SOI wafer is boron doped with a resistivity of 13.5-22.5 Ω·cm and the corresponding doping concentration is about 1.0×10^{15} cm^{-3}. The thickness of the SOI and buried oxide (BOX) layer is 90

nm and 200 nm, respectively. The annealing temperature and time for the silicidation is 500 ℃ and 5 min, respectively. The remained Erbium is removed using the mixture of H_2SO_4 and H_2O_2 (Sulfuric Peroxide mixture: SPM) for 10 min. The volume mixture ratio is 1:1.

Fig. 3 shows the drain current to drain voltage characteristics of Erbium silicided *n*-type SBTTs. The gate length and gate oxide thickness is 10 ㎛ and 3 nm, respectively. The gate voltage varied from 1.0 to 2.0 V with 0.5 V step. In Fig. 3, the line and circle represents experimental and theoretical results, respectively. The experimental and theoretical results show good correspondence, which shows the validity of the suggested model. From the curve fitting, the extracted Schottky barrier height is 0.24 eV, which is slightly lower than typical value of Erbium silicide formed on *n*-type silicon [2].

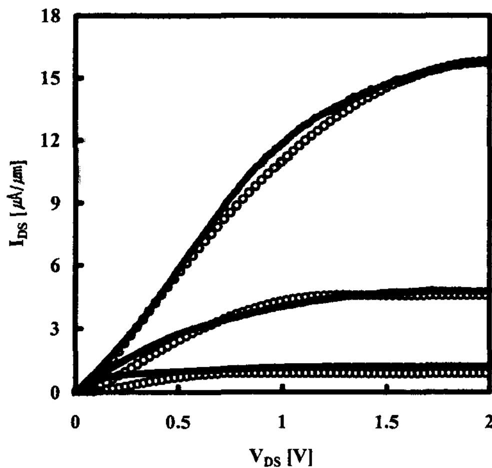

Fig. 3. Drain current versus drain voltage characteristics of 10 ㎛ long channel *n*-type SBTTs with various gate voltages. The solid line and circle represents experimental and simulation result, respectively.

The extracted threshold voltage of SBTTs is 1.0 V. Note that the extracted channel region threshold voltage is 0.3 V, which is the function of gate flat band voltage, gate oxide thickness and channel region doping concentration. Although the channel is strongly inverted, the current begin to flow at more higher gate voltage because of the suppression of tunneling current at low gate voltage as discussed in Fig. 2. The increase of threshold voltage in SBTTs can be found in the previous experimental works [1]-[5].

Fig. 4 shows the variation of drain current as a function of the drain voltage. The physical gate length and channel width is 60 nm and 100 nm, respectively, which is confirmed from the atomic force microscopy (AFM) measurements. The thermally grown gate oxide thickness is 20 nm and the gate electrode is highly phosphorus doped *n*-type polycrystalline silicon. Drain voltage varied from 0 to 1 V and the gate voltage varied from 0 to 15 V with 3 V step. The measured current-voltage characteristics show typical transistor behaviors. The saturation current at the gate voltage of 15 V is 8.3 μA/㎛. The low saturation current is attributed to the high parasitic source and drain resistance. The total parasitic resistance of source and drain, measured from test pattern, was 23 KΩ, which corresponds to 230 Ω/square, if converted into sheet resistance. The sheet resistance of large width pattern is 17 Ω. The width dependency of sheet resistance is studied in various kinds of silicide materials [12], [13].

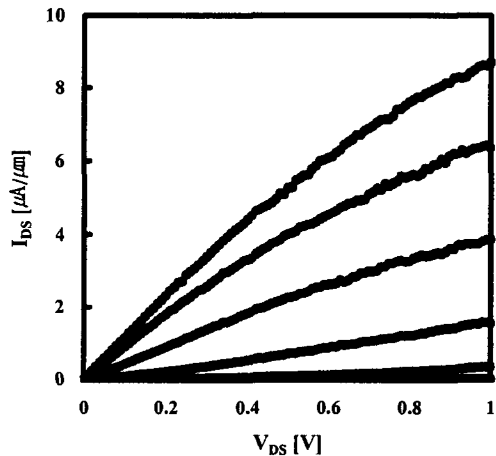

Fig. 4. Drain current versus drain voltage characteristics of the 60 nm channel Erbium silicided *n*-type SBTTs at room temperature. Gate voltage varied from 0 to 15 V with 3 V step.

Fig. 5 shows the drain current as a function of the gate voltage. The gate voltage varied from 0 to 15 V and the drain voltage varied as 0.05, 0.1 and 1.0 V, respectively. At 0.05 V

drain voltage, the off-leakage current is less than 10^{-4} $\mu A/\mu m$, and increases up to 5×10^{-3} $\mu A/\mu m$ with the increase of drain voltage. Moreover, the drain current increases with the drain voltage. The drain current on/off ratio is about 10^5 at 0.05 V drain voltage regime in drain current to gate voltage characteristics. The increase of the off-current is mainly attributed to the thermionic current and the increase of the drain current is mainly attributed to the tunneling current component, respectively. This is confirmed from the detailed numerical simulation [14, 15].

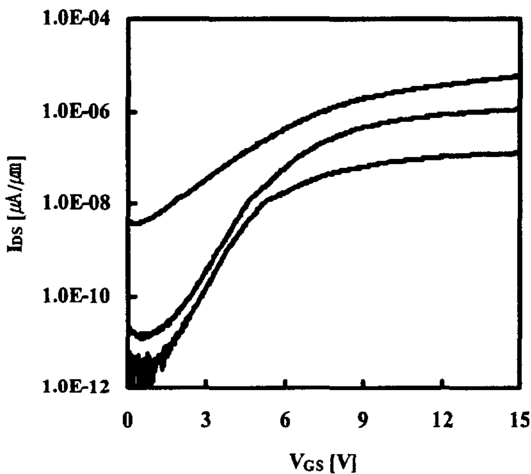

Fig. 5. Drain current versus gate voltage characteristics of the 60 nm Erbium silicided *n*-type SBTTs with various dr ain voltage at room temperature. Drain voltage varied as 0. 05, 0.1 and 1.0 V.

Conclusion

The current-voltage characteristics of Schottky barrier tunnel transistor are simulated by considering the internal voltage and using the current continuity condition between tunneling current from Schottky barrier and channel current. The experimental and theoretical results show good correspondence in 10 μm long channel Erbium silicided *n*-type SBTTs, which shows the validity of the suggested model. From the curve fitting, the extracted Schottky barrier height is 0.24 eV. The *n*-type SBTTs with 60 nm gate lengths show typical transistor behaviors in drain current to drain voltage characteristics. The drain current on/off ratio is about 10^5 at low drain voltage regime in drain current to gate voltage characteristics. However, the on/off ratio tends to decrease as the drain voltage increases.The increase of off-current is mainly attributed to the thermionic current and the increase of drain current is mainly attributed to the tunneling current.

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