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Single-Chip Eye Ball Sensor using Smart CIS Pixels

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ABSTRACT

An Eye Ball Sensor (EBS) is a system that locates the point where the user gazes on. The conventional EBS using a CCD camera needs many peripherals, software computation causing high cost and power consumption. This paper proposes a compact EBS using smart CMOS Image Sensor (CIS) pixels. The proposed single chip EBS does not need any peripheral and operates at higher speed and lower cost than the conventional EBS. The test chip was designed and fabricated for 32×32 smart CIS pixel array with a 0.35 μm CMOS process occupying 5.3mm^2 silicon area.

Ⅰ. INTRODUCTION

The common interface between human and the computer is a keyboard and mouse. However, these interfaces are difficult to use in mobile environment and for the handicapped. One of alternative Human Computer Interface (HCI) is EBS that acquires the center point of the eye ball. With EBS the computer can acquire the point on the screen that an user gazes on [1][2]. Infrared light is commonly used in EBS because it eliminates influence of ambient illumination and improves discrepancy between pupil and the white of eye. Under infrared illumination, the pupil is the biggest black region in the eye image. The point that the eye gazes on can be obtained by finding the center point of the pupil [3].

A CCD camera is commonly use to acquiring the image . The image from the a CCD camera is translated to digital data through A/D converter. By performing Digital Signal Processing (DSP), the center point of the eyeball can be obtained. However this EBS needs many peripherals and causing high cost. This paper proposes a single-chip EBS that does not require additional peripherals. The proposed EBS is implemented by single chip containing smart CIS pixels and the system that can generate digital data indicating the center point of the eyeball. Thus, the proposed system can operate at higher speed and the lower cost than a conventional EBS.

Section Ⅱ proposes the new EBS architecture. Section Ⅲ represents simulation results and layout. Finally, Section Ⅳ provides the conclusion.

Ⅱ. PROPOSED SYSTEM ARCHITECTURE

The proposed EBS is composed of smart CIS pixels, Winner-Take-All (WTA) circuits and encoders as shown in Fig. 1.

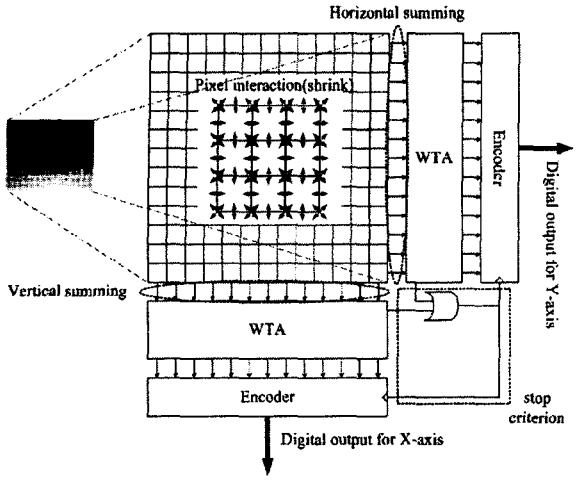

Fig. 1. Block diagram of the proposed EBS

Each smart CIS pixel is interconnected with its surrounding pixels as shown Fig. 2. These inter-pixel feedback perform shrink operation. The white pixels beside a black region force the black pixel to be changed white. As the boundary black pixel is changed to the white continuously, the size of the black region is shrinked as shown in Fig. 3. The shrink operation stops when the total number of survival pixel (black) is lower than ceratin limit.

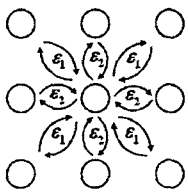

Fig. 2. Shrink operation weight
($0 < \varepsilon_1 < \varepsilon_2 < 1$)

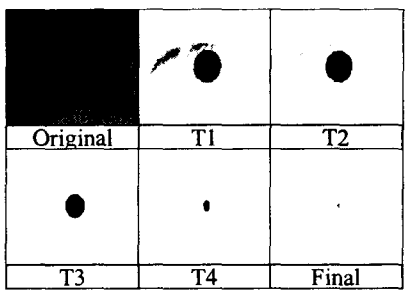

Fig. 3. Shrink operation

Each pixel generates current corresponding its state and the current is summed column-wise and row-wise, respectively. The WTA [4][5][6] looks for the column/row that has highest current The only column/row that has highest current remains logic high output. The column/row with highest current represent the center of the survival pixels. The WTA also select the winner current, I_{WIN} and compare it with a reference current, I_{STOP}. If I_{WIN} is smaller than I_{STOP}, then the address register latches the address of the winner.

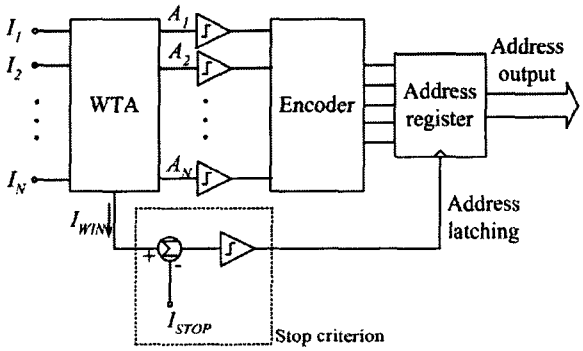

Fig. 4. Black diagram of WTA and Encoder

A schematic diagram of smart CIS pixel is shown in Fig. 5. One cycle is composed of 4 phases as shown in Fig. 6. First, a photo diode parasitic capacitor C_S is charged to V_{REF1} and C_F is reset during T_rst phase. By turning on *RST* and *CTL*, all eight interconnection transistors are turned-off and do not give any feedback to surrounding pixels. Second, *RST* is turned-off and C_S is charged to $(V_{REF1}-V_P)$ where V_P is proportional to the incident light intensity. Third, the charge in C_S is transferred to C_F, by turning on *RST*. Eight interconnection transistors are turned-on and generate current corresponding the state voltage of the pixel, V_B. The state current is copied by M_R and M_C and these current is summed out at column bus and row bus, respectively. The inter-pixel dynamics are started by turning on the STR switch.

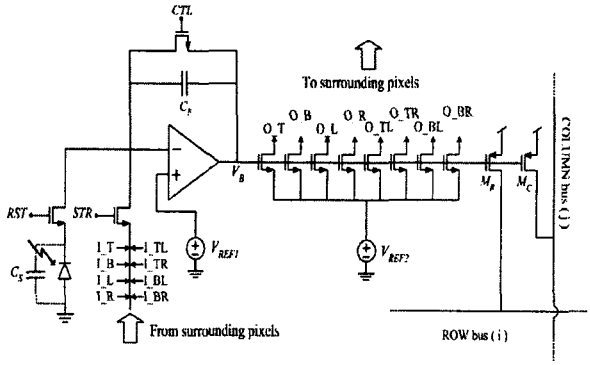

Fig. 5. Smart CIS pixel circuit diagram

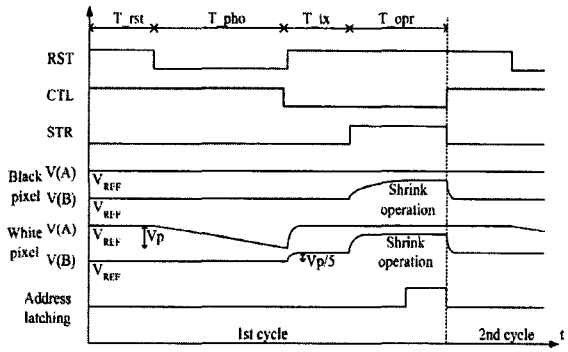

Fig. 6. Smart CIS pixel timing diagram

A schematic diagram of WTA is shown in Fig. 7. V_S is decided when only the winning transistor is turned on and all other input transistor turned off [5]. Then I_{WIN} is equal to the winning input current. $A_{1\cdots N}$ are connected to encoder and V_{STOP} is connected to address encoder through buffer.

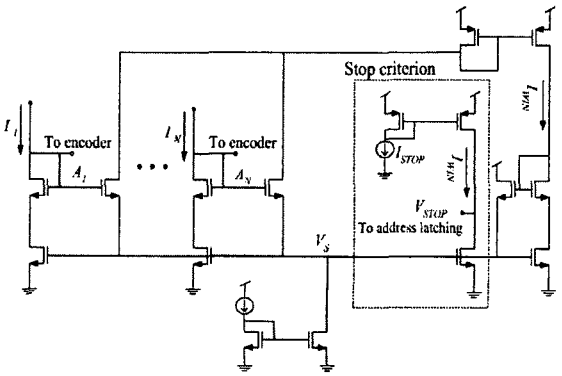

Fig. 7. WTA circuit diagram

III. SIMULATION RESULTS AND LAYOUT

The proposed smart CIS pixels is simulated in block level. Fig. 8 shows the simulated output current of each column and row at the end of shrink operation. The graphs labeled vertical and horizontal represent that how many black pixels each row(column) are remained. The output image shows 6 remaining pixels at the end of shrink operation.

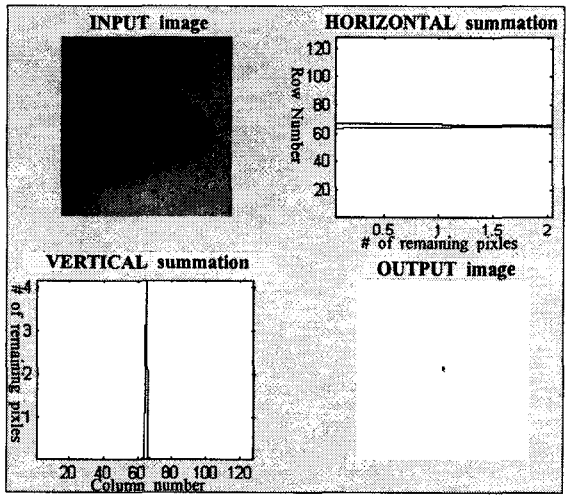

Fig 8. Block level simulation

The proposed EBS is simulated in transistor level. The proposed system has 32×32 smart CIS pixel array. Fig. 9 shows simulation results. The white cross marker on the image represents digital output coordinates of the proposed system and it is matched with the center of the pupil.

Fig. 10 shows the layout of the designed EBS. The EBS is design for 0.35μm CMOS process and the total area is 5.3mm^2 for 32×32 pixel array.

	Row Output	Column Output
Center	01111	10000
Left	01111	01010
Right	01110	10101
Up	01101	01111
Down	10010	01111

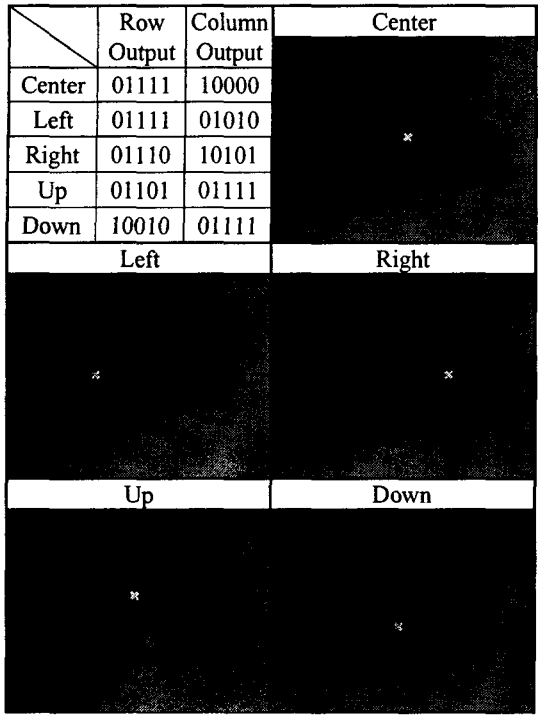

Fig 9. Simulation results for input of 5 eye images

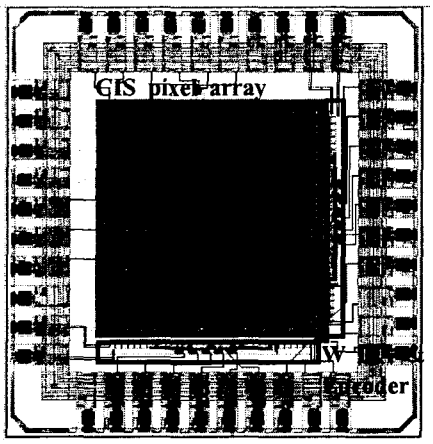

Fig. 10. Chip layout

IV. CONCLUSION

This paper proposed a compact single-chip EBS. Analysis and simulation results indicates that the proposed system can generate address indicating the center point of the eyeball at higher speed and the lower cost than conventional EBS. The proposed system use 0.35 *um* CMOS process occupying 5.3mm^2 silicon area.

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