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# Low–Power, High Slew-Rate Transconductance-Boosted OP-AMP for Large Size, High Resolution TFT-LCDs

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## Abstract

*For the analog output buffer in the data driver for large size and high resolution TFT-LCDs, we proposed operational amplifier (op-amp) which contains newly developed transconductance-boosted input stage which enables the low-power consumption and the high slew-rate. The slew-rate and the quiescent current of the proposed op-amp are 6.1V/μsec and 8μA , respectively.*

## 1. Introduction

As the size and resolution of TFT-LCDs become larger and higher, capacitive and resistive loads of data lines increase according to the longer length of the data lines and one row line time decrease according to the more gate lines. In AMLCDs, a various voltage levels of signals must be transmitted to a pixel precisely through the data lines wherever the pixels are located at the front-end or at the rear-end of the line. At the rear-end of data lines, the signals are delayed by the distributed resistance and capacitance of the data lines and, if the one row line time is not sufficient, exact voltage level of signal can not be transferred to the pixels at the rear-end of the data lines due to the RC-delay of the data lines.

Moreover, if the op-amps which are being used as analog buffers in the data driver of TFT-LCDs have low slew-rate, which means a term used to describe how quickly the potential on a circuit node must change with respect to time, the delay of signal in the data lines become more increase as shown in figure 1. So, the op-amps for large size and high resolution TFT-LCDs must have the high slew-rate.

Generally, in the conventional two-stage op-amps which are used in the data driver of TFT-LCDs, the slew-rates of op-amps are proportional to the quiescent currents. For that reason, power consumptions must be increased in order to increase the slew-rates of the conventional op-amps.

In this paper, in order to overcome the limitation between the slew-rates and the power consumptions of the conventional two-stage op-amps, we proposed newly developed transconductance-boosted input stage and its two-stage op-amp which shows low-power consumption and high slew-rate compared to the conventional two-stage op-amps.

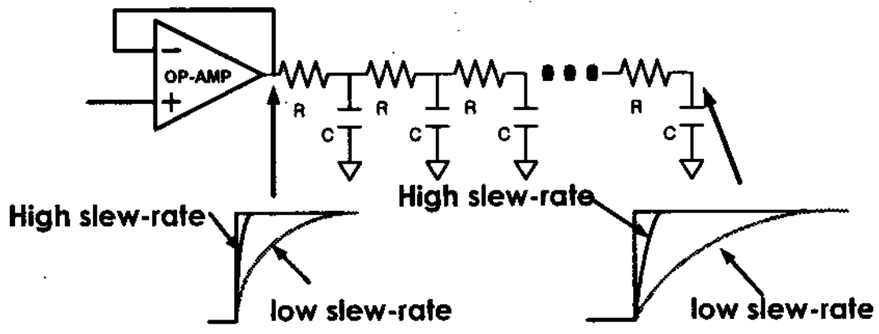


**Figure 1. The delay of signal in the data line. (high vs. low slew-rate)**

## 2. The conventional two-stage op-amps in the data driver for TFT-LCDs

Conventionally, in order to achieve high dc gain and rail-to-rail input/output driving voltage range, a rail-to-rail folded cascode op-amp is used in the data driver for TFT-LCDs. In the conventional rail-to-rail folded cascode op-amps, as shown in figure 2, contains a rail-to-rail input stage, M1-M4, a summing circuit, M7-M14, class-AB output stage, M17-M20, and floating current source, M15-M16 [1,2].

In the conventional rail-to-rail folded cascode op-amp, as shown in figure 2, slewing occurs when the differential input voltage is larger than ΔV (i.e. $I_{tail}/g_m$) of the differential input pair transistors. During this period one of the differential input pair transistor (M1 or M2) is completely turn off while the other one is completely on. The tail current completely flows through transistor M1 or M2. At that time, the slew-rate is proportional to the current which charges and discharges the compensation so that the slew-rate is proportional to the tail current ($I_{tail}$) which flows through transistor M5 and M6, as shown in equation (1).

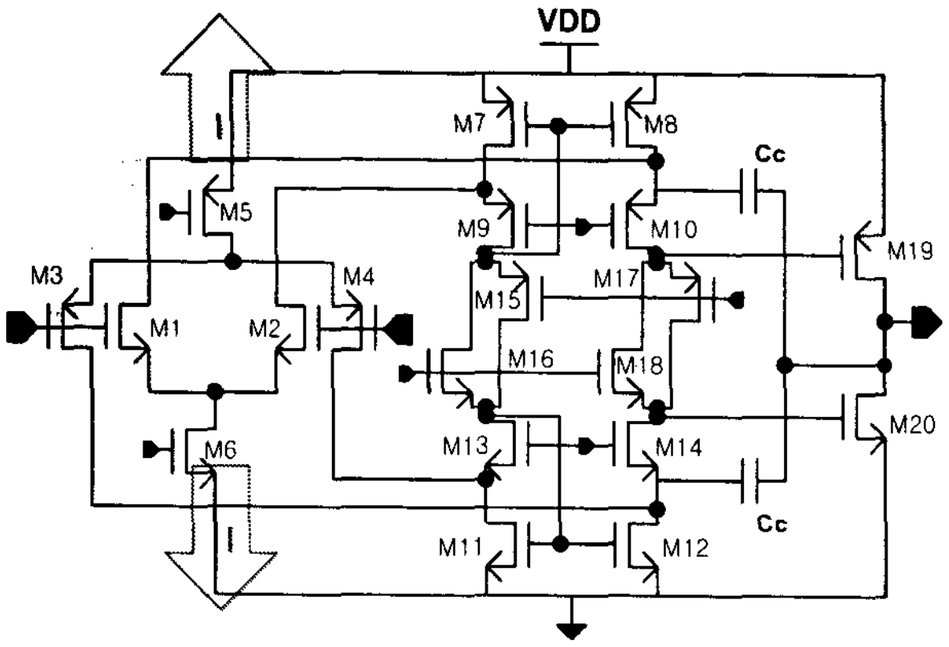


**Figure 2. Schematic diagram of the conventional rail-to-rail folded cascode op-amp.**

$$S \cdot R = \frac{I_{tail}}{C_c} \qquad (1)$$

If the tail current (i.e. quiescent current) of op-amp increases for high slew-rate, the power consumption will also increase, consequently.

## 3. Newly developed transconductance-booted op-amp

Figure 3 shows the proposed op-amp with transconductance-boosted input stage. The proposed op-amp is consist of the input stage, M1-M4, transconductance-boosted input stage, M21-M28, a summing circuit, M7-M14, class-AB output stage, M17-M20, and floating current source, M15-M16. This op-amp is basically the same as the conventinal rail-to-rail folded cascode op-amp as shown in figure 2, except for the transconductance-boosted input stage.

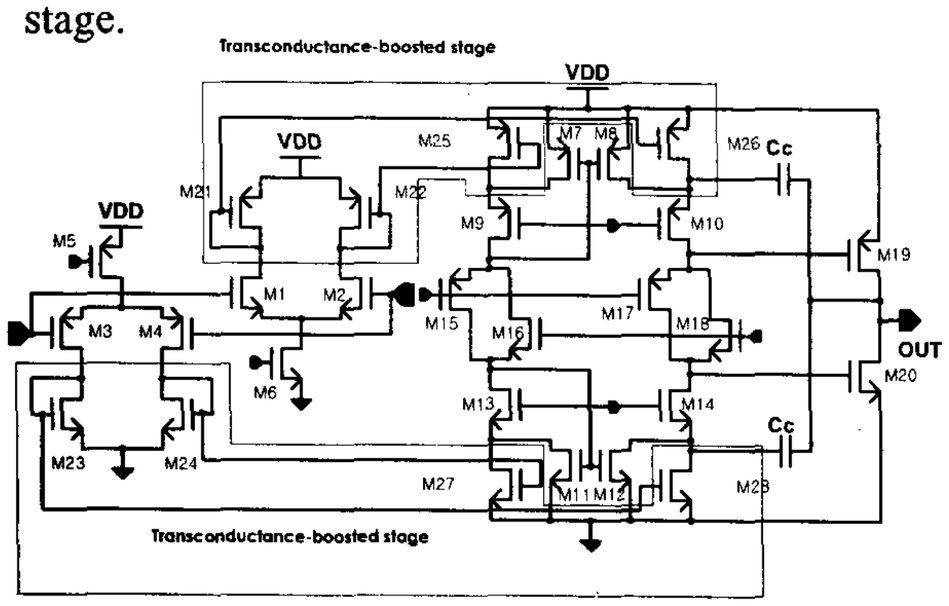


**Figure 3. Schematic diagram of the proposed transconductance-boosted op-amp.**

stage is shown in figure 3. Transistor M21 and M26 form a current mirror[3]. The maximum current flowing through the transistor M26 can be made large if the device size W/L of transistor M26 is made large with respect to M21. However, if device size is too large, the quiescent current of the proposed op-amp will be increased and extra power will be wasted during normal operation the op-amp. So, we design the transconductance-boosted input stage that the device size of M26 is three times as larger than that of M21 so that the current of flowing through M26 is three times than that of flowing through M21.

In order to know the slew-rate both the proposed op-amp and the conventional op-amp, we compared the current flowing through the compensation capacitor of the proposed op-amp with that of the conventional op-amp. When the tail current flowing the transistor M5 or M6 is I, the first stage quiescent current of the conventional folded cascode op-amp is 3I as shown in figure 4. While slewing, the current flowing through compensation capacitor is I as shown in figure 5. The other hand, the first stage quiescent current of the proposed transconductance-boosted op-amp is 8I* as shown in figure 6. In order to distinguish form tail current I of the conventional op-amp, the proposed op-amp use I*. In the proposed op-amp, during slew, the current flowing through compensation capacitor is six times as larger than the tail current flowing through differential input stage, as shown in figure 7. If the first stage quiescent current of the conventional op-amp and the proposed op-amp is the same, the first stage quiescent current of the proposed op-amp express by equation (2).

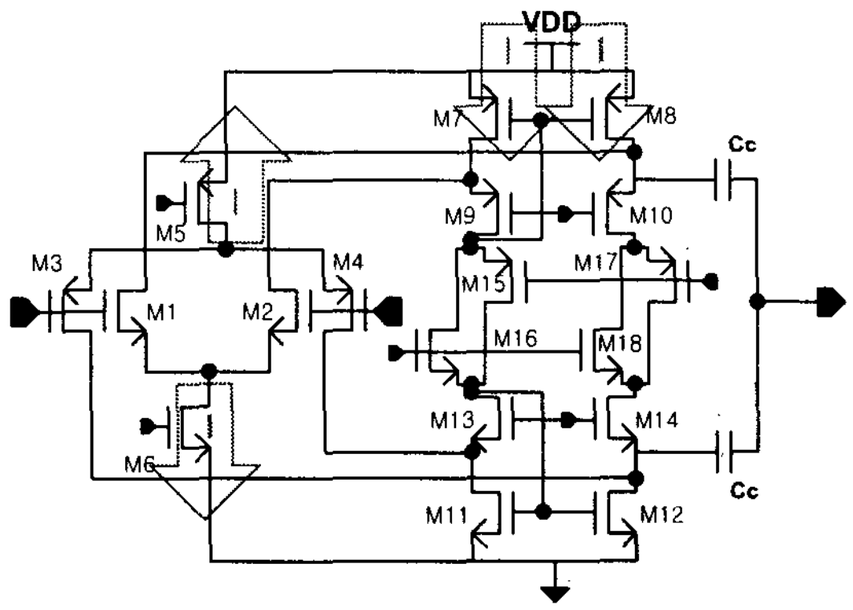


**Figure 4. The quiescent current flow of the conventional op-amp.**

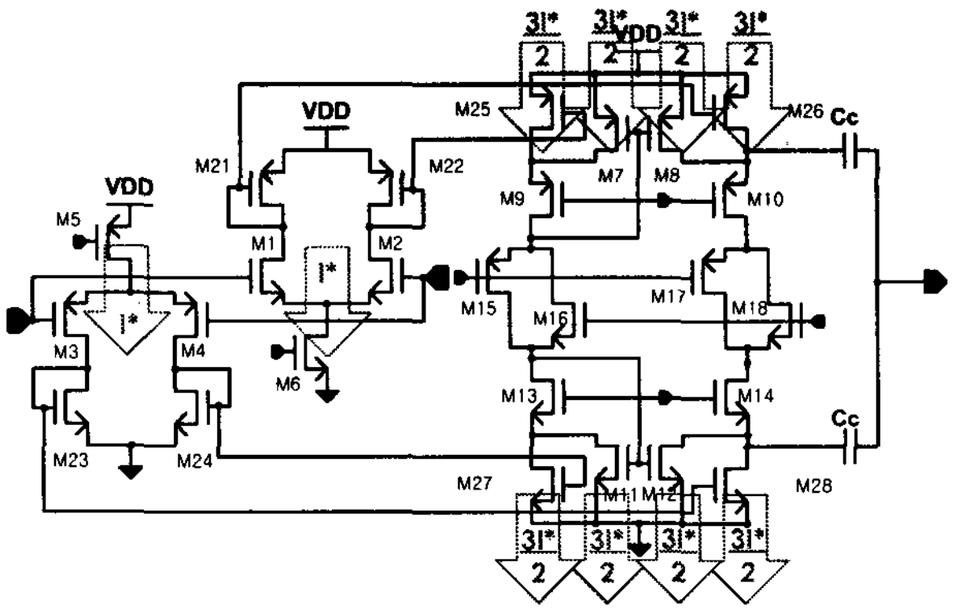


**Figure 5. The quiescent current flow of the proposed transconductance-boosted op-amp.**

$$8I^* = 3I \qquad (2)$$

$$I^* = \frac{3}{8}I \qquad (2)`$$

Arranging about I*, we can get equation (2)`. In the proposed op-amp, the current flowing through compensation capacitor is 6I*. In equation (3), I* can be substituted as 3I/8 and finally we can get equation (3)`. Equation (3)` means that the current flowing through compensation capacitor of the proposed op-amp is more than two times than that of the conventional op-amp. Because the slew-rate is proportional to the current flowing through compensation capacitor, the slew-rate of the proposed op-amp is more than two times of that of conventional one in case of the same quiescent current, consequently.

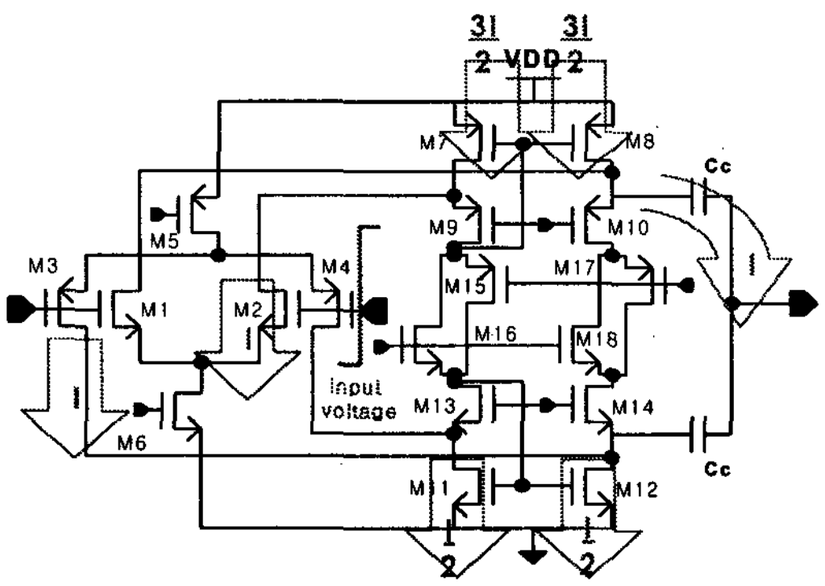


**Figure 6. The current flow of the conventional op-amp, while slewing.**

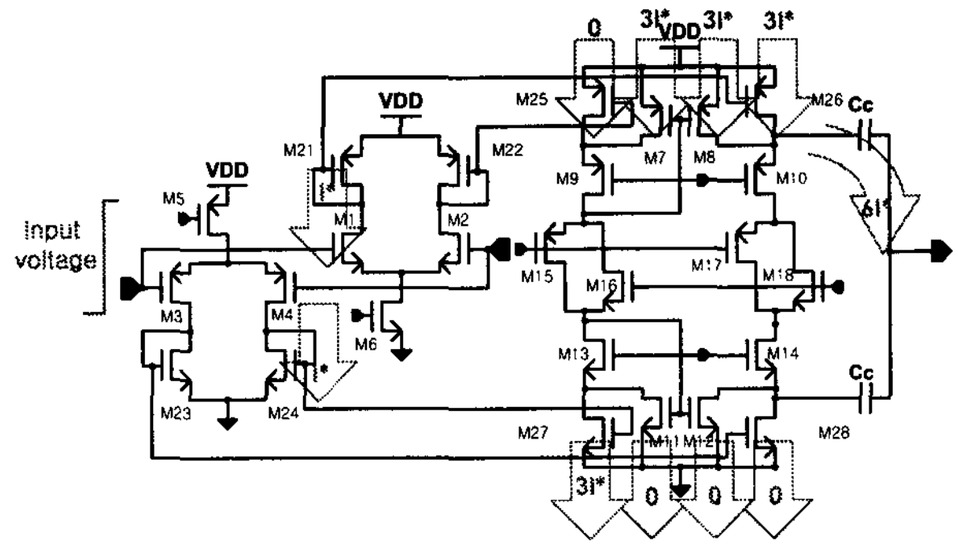


**Figure 7. The current flow of the proposed op-amp, while slewing.**

$$6I^* = 6 \times \frac{3}{8}I \qquad (3)$$

$$6I^* = 2.25I \qquad (3)`$$

## 4. Simulation results

Simulation conditions are VDD=10V, VSS=0V, temperature=25°C and the simulation model for step response is shown in figure 8. The loads are modeled as a data line of TFT-LCD panel and figure 9 shows the transient simulation results when input voltage is the step pulse which swings from 0.5V to 9.5V.

The slew-rate of the proposed op-amp is about 6.1V/μsec at the mid point of the transition when the quiescent current is about 8μA. In case of the conventional op-amp of figure 2, slew-rate is about 3.2V/μsec when the quiescent current is about 8μA. The above results show that the proposed op-amp haves high slew-rate nevertheless the quiescent current is less than the conventional op-amps. The simulation results are summarized in table 1 compared to the op-amp as shown in figure 2.

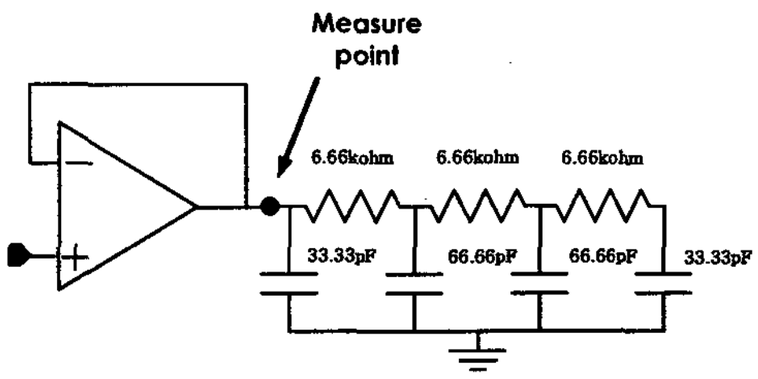


**Figure 8. The simulation model for transient characteristics.**

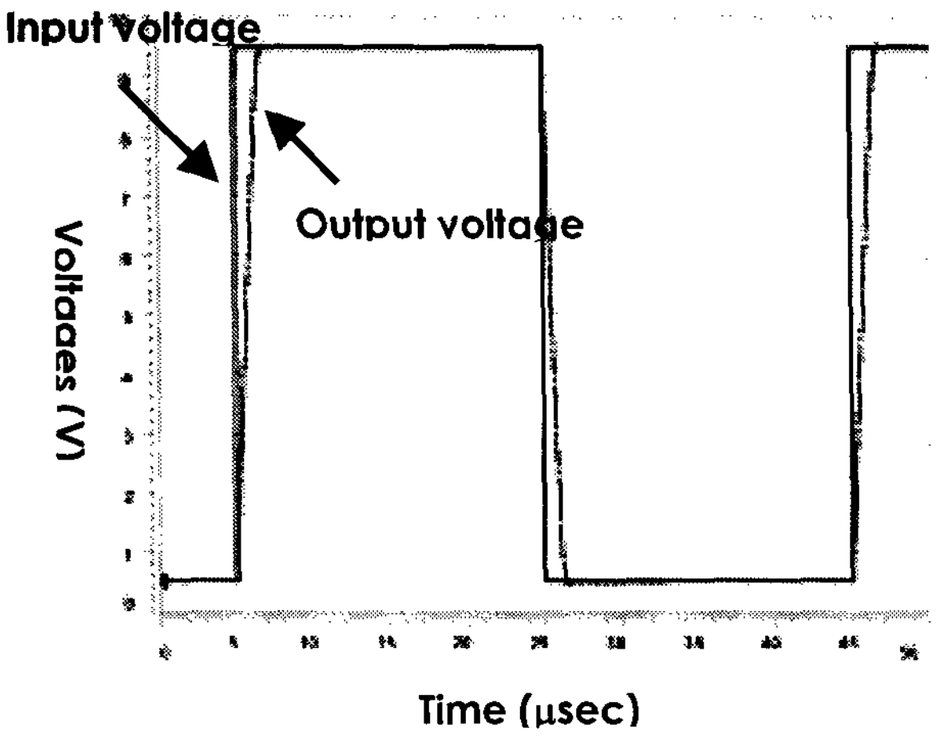


**Figure 9. The transient simulation waveform.**

**Table 1. Comparison of characteristics. (conventional vs. proposed op-amp)**

| | Conventional | Proposed |
|---|---|---|
| VDD | 10V | 10V |
| Slew-rate | 3.2V/μsec. | 6.1V/μsec. |
| Quiescent current | ≈ 8μA | ≈ 8μA |
| Open loop gain | ≈100dB | ≈100dB |
| Phase margin | ≈ 60° | ≈ 60° |

## 5.Conclusion

In the conventional op-amp, the slew-rate and the quiescent current are 3.2V/μsec and 8μA. However, the slew-rate and the quiescent current of the proposed op-amp are 6.1V/μsec and 8μA. Therefore, the proposed op-amp is suitable for the data drivers of large-area and high-resolution TFT-LCDs.

## 6. References

[1] Botma, J. H., *et. al.*, "A Low-voltage CMOS Operational Amplifier with a Rail-to-Rail Constant-gm Input stage and a Class AB Rail-to-Rail Output Stage", Proceeding ISCAS 93, pp.1314-1317.

[2] R. Hogervorst, *et. al.*, "A compact Power-Efficient Rail-to-Rail Input/Output Operational Amplifier for VLSI Cell Libraries", IEEE J. of solid-State Circuits, SC-29, Dec 1994, pp.1505-1512.

[3] P.R Gray and R.G Meyer, "Analyses and Design of Analog Integrated Circuits", Wiley, New york, USA, 1894.