Capacitor DAC (Digital to Analog Converter) With Gamma-correction for TFT-LCD driver

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Abstract

The Capacitor DAC with gamma correction is proposed for TFT-LCD (Liquid Crystal Display) driver application. It is based on two ideas. First, 6bit digital code is converted 8bit digital code by memory circuit (Look Up Table) for gamma correction. second, weighted voltage ratio DAC is proposed for reducing area and power consumption.

1. Introduction

Recently the importance of display devices has been increased because it is a novel tool that information goes through in multi-media era[1,2]. In contrast with the conventional display (CRT), flat panel displays have been rapidly growing in the display market[3]. Among them, TFT-LCD is distinguishable because of its great features like light weight thin thickness, high resolution and low power consumption. Therefore many R&D activities and investments of TFT-LCD are still going on [4,5]. The purpose of the DAC is to transform the digital representation (input word) of a signal into its analog corresponding representation. High performance DAC is required for TFT-LCD driver applications.

The conventional resistor DAC (Digital to Analog Converter) architecture uses one resistor DAC per output to convert the digital data into analog voltage levels. As shown in figure 1, digital data is loaded and stored in data latches until the conversion takes place. Because each output has an independent DAC, the data conversion only needs to occur once per line, typically at the end of the line[6]. Note that a N:2^N decoder will be required to provide the 2^N signal controlling the switches. The advantage of the resistor string DAC is that the output will always be guaranteed to be monotonic. But resistor string DAC is limited problem that DAC output is always

connected to 2^N-1 switches that are off and one switch that is on. For high resolution, a large parasitic capacitance appears at the output node, resulting in slower conversion speeds. An integrated version of this converter will lead to a large chip area for high resolutions because of the large number of passive components are necessary. However, as the resolution increases, the relative accuracy of the resistors becomes an important factor. Although the size of resistor must be made small to minimize the chip area required, power dissipation would then become the critical issue as current flows through the resistor string at all times. The disadvantage of resistor DAC cannot use high resolution TFT-LCD application[7].

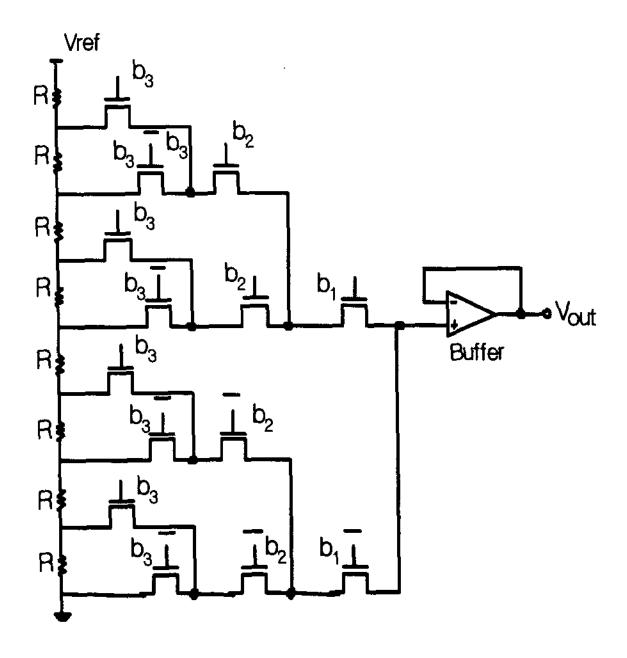


Figure 1. A conventional resistor string DAC.

Weighted capacitor DAC has been smaller chip area and power consumption than conventional resistor DAC (in case of 6bit DAC). But weighted capacitor DAC is not use TFT-LCD driver. Because of weighted capacitor DAC is not realized gamma correction and induced a parasitic capacitance. This will prohibit its use as a high-resolution data converter. Also, capacitor DAC is the precisely ratioed capacitors. [8] As the number of bits increase, the ratio of the MSB capacitor to the LSB capacitor becomes more difficult to control. Another problem is that capacitor DAC increased the area exponential. In addition weighted capacitor DAC cannot to achieve gamma correction. Gamma correction is need high resolution TFT-LCD driver[9,10].

This paper proposed that gamma correction with weighted voltage ratio DAC for TFT-LCD driver application. It is based on two new ideas. First, 6bit digital code is converted 8bit digital code by memory circuit (LUT) for gamma correction, second weighted voltage ratio DAC circuit is driven that which is reduced area and power consumption.

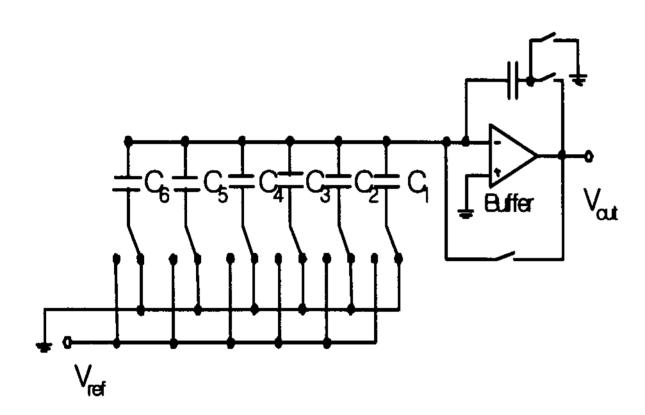


Figure 2. A conventional capacitor DAC.

2. The proposed Capacitor DAC with gamma correction for TFT LCD driver.

Gamma correction is realized that 6bit digital code converted 8bit digital code to use memory circuit (Look Up Table). As shown in figure3, Output voltage of weighted capacitor DAC is linearly increased a straight line. So, weighted capacitor DAC cannot to achieve gamma correction.

We proposed that digital code converting method to achieve gamma correction. For example, digital input code a_1 (a_1 indicate weighted capacitor DAC reference

voltage V₀) could not indicate V₁ (gamma-voltage). So, digital input code is converted a₁ to a₂. The value is that a₂ digital input code is indicated V₁ voltage and V₁ voltage is matched gamma-correction S-curve. 6bit digital input code could not express gamma correction (reference voltage). So digital input code is increased 8bit digital input code to achieve gamma correction. As shown in figure 4. 6bit digital input code is converted 8bit digital input code by memory circuit (LUT).

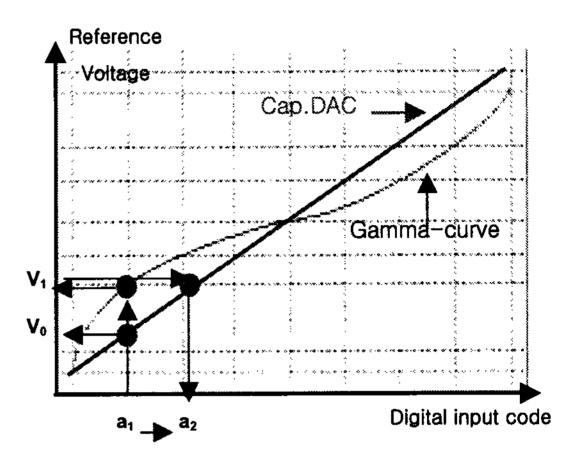


Figure 3. Binary weighted capacitor DAC vs. gamma curve.

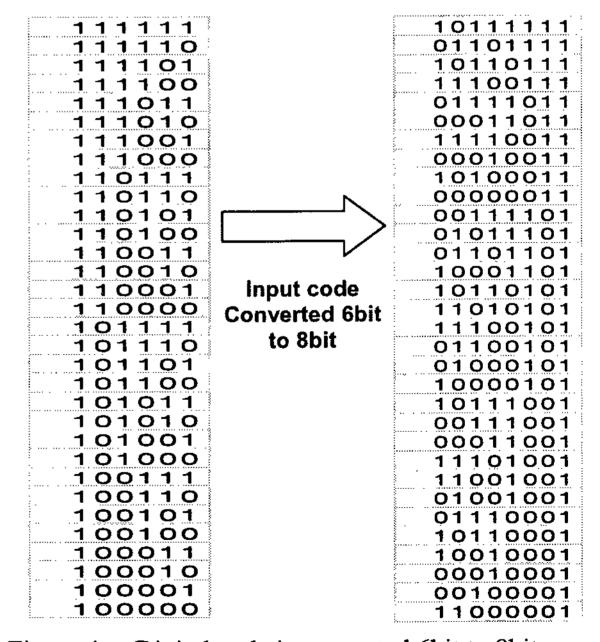


Figure 4. Digital code is converted 6bit to 8bit.

3. Proposed Circuit Design.

Look Up Table offer to use binary digital code is converted 6bit to 8bit binary digital code. As shown in figure 5, conventional 6bit weighted capacitor DAC. The charge redistribution DAC is a switched capacitor circuit, where the charge stored on a number of binary weighted capacitors is used to perform the conversion. For example of an N-bit converter found in conventional weighted capacitor DAC. The most significant capacitor C_{N-1} is 2^{N-1} times larger than the least significant capacitor $C_0 = C$, i.e., $C_{N-1} = 2^{N-1} \cdot C$. Typically, the weighted capacitor are created using a number of unit capacitors. Weighted capacitor DAC is needed precisely ratio capacitors. As the number of bits increase, the ratio of the MSB capacitor to the LSB becomes more difficult to control. This paper proposed that weighted voltage ratio DAC. As shown in figure 6, for weighted voltage ratio DAC driving, it is needed to generate adaptive voltage, which is to supply external memory circuit. This circuit increased accuracy, reduced area and power consumption than conventional weighted capacitor DAC.

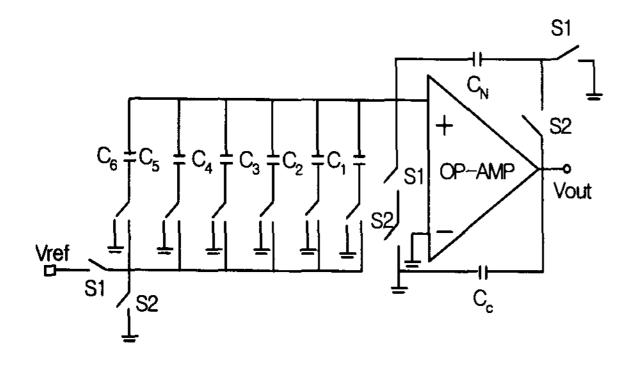


Figure 5. A conventional 6bit weighted capacitor DAC.

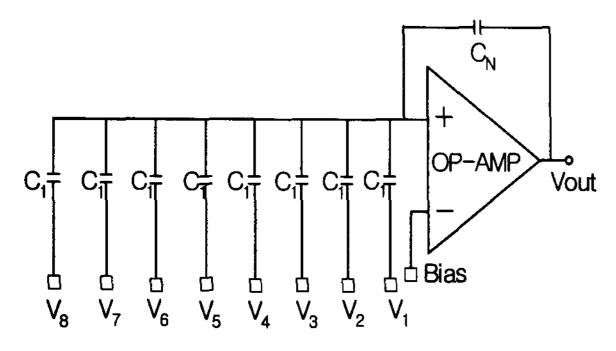


Figure 6. A proposed weighted voltage ratio DAC.

4. Simulation Result.

As shown in figure 8, waveform is represented digital code converting to achieve gamma correction for TFT-LCD driver application and weighted voltage ratio DAC circuit simulation result. Weighted voltage ratio capacitor DAC is increased accuracy DNL value is 0.2LSB. Also, weighted voltage ratio capacitor DAC is reduced area 30% rather than conventional weighted DAC. Proposed weighted voltage ratio DAC is reduced power consumption 28% compared with weighted capacitor DAC. conventional The specifications of weighted voltage ratio DAC driving circuit and the unity gain OP-AMP, which are used in the Hspice simulations, are summarized in table 1.

Table 1. Specifications of the weighted voltage DAC driving circuit and the unity gain OP-AMP

Parameters	Specifications
PMOS size in switches(W/L)	6μm/3μm
NMOS size in switches(W/L)	3μm/3μm
Capacitor C ₁	0.1pF
Capacitor C _N	0.64pF
Slew-rate of OP-AMP	4V/μs

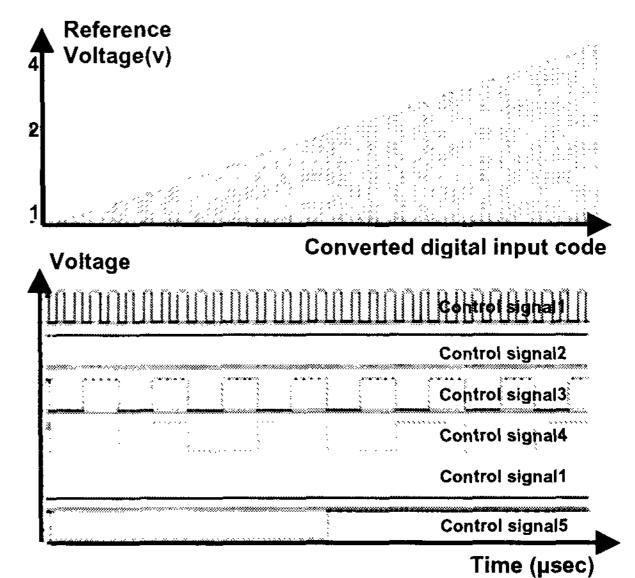


Figure 8. Converted digital input code vs. control signal.

5. Conclusion

We proposed that weighted voltage ratio capacitor DAC with gamma correction for TFT-LCD driver application. 6bit digital code is converted 8bit digital code by memory circuit (Look Up Table) for gamma correction, and weighted voltage ratio DAC is reduced the area (30%) and power consumption (28%).

5. References

- [1] SUAREZ, R.E., GRAY, P.R., and HODGES, D.A.: 'All-MOS charge redistribution analog-to digital conversion techniques- part 2', IEEE J. Solid-State Circuits, 1975, SC-10, (6), pp.379-385
- [2] Hisashi Sasaki, Takashi Taguchi Toshiba Corp. Semiconductor Company "Perceptually Linear Gamma correction for LCDs" SID2003 25.3
- [3] P. Rombouts and L. Wiyten "Linearity improvement fir the switched-capacitor DAC. ELECTRONICS LET TERS 1996 Vol. 32 No. 4
- [4] J. Steensgaard, U. Moo and G.C. Temes "Mismated-shaping switching for two-capacitor DAC" ELECTRONICS LETTERS 1998 Vol. 34 No.17

- [5] Y. S. LEE, L. M TERMAN, and L. G. HELLER "A Two-Stage Weighted Capacitor Network for D/A-A/D Conversion." *IEEE 1979*
- [6] Un-Ku Moon, Jose Silba, Jesper Steensgaard and Gabor C. Temes "A Switched-capacitor DAC with analog mismatch correction" *ISCAS 2000 0-7803-5482-6/99/*
- [7] P. Ju, K. Suyama, P. Ferauson, Jr. W. Lee "A highly linear switched-capacitor DAC for Multi-bit Sigma-Delta D/A Applications" *IEEE 1995 0-7803-2570-2/95*
- [8] Peicheng Ju., Ken Suyama, Paul F. Ferguso, Jr. and Wai Lee "A22-kHz Multibit Switched-Capacitor Sigma-Delta D/A Converter with 92 dB Dynamic Range." *IEEE 1995 0018-9200/95*
- [9] D.A. Johns and K. Martin, *Analog Integrated Circuit Design*, John Wiley & Sons, New York, NY, USA, 1997, *ISBN 0-471-14448-7*
- [10] R. L. Suarez, P. R. Gray, and D. A. Hodges, "All-MOS Charge Redistribution Analog-to-Digital Conversion Techniques-Part 2," *IEEE Journal of Solid State Circuits*, Vol. 10, No. 6, pp.379-385, December 1975.