Printed Active-Matrix Displays

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Abstract

We present a process for printing active matrix displays. In this process, transistors are fabricated using soluble semi-conducting and conducting materials. Accurate definition of the transistor channel and other circuit components is achieved by direct inkjet printing combined with surface energy patterning. We present results on our 4,800 pixel, 50 dpi, active matrix displays.

1. Objectives and Background

The formation of thin film transistors (TFTs) by solution processing and direct printing is recognized as having applications in active matrix display fabrication [1-3]. We have developed a process where complete transistor circuits can be fabricated from solution by direct ink-jet printing. TFTs manufactured using our process have had mobilities of up to $2x10^{-2}$ cm^2/Vs, approaching that of amorphous silicon. They have furthermore had on/off current ratios of 10^5, low hysteresis and good operating stability [4].

We have used this process to fabricate 4,800 pixel, 50 dpi, active matrix back planes and displays. These back planes can be combined with any voltage controlled display effect such as liquid crystal and electronic paper. The advantages of a print based process compared to conventional thin-film silicon TFT technology include being environmentally friendly, low temperature, compatible with flexible substrates (and ultimately enabling roll to roll production), cost effective, advantageous for short run length and appropriate for large display sizes. It is anticipated that this process will produce active matrix back planes for commercially available displays in the coming years.

2. Results

2.1 Printing Active Matrix Backplanes

Starting with a glass substrate patterned with ITO source lines and pixels, the thin film transistors are built up from solution in several stages to form an array or active matrix back plane of 4800 transistors.

The sources and drains of the transistors are formed by a combination of surface energy patterning and printing, a feature that allows printing with a resolution of 2 microns or less, which is required to define the critical channel between the source and drain electrodes of a transistor. This high resolution is achieved by confining spreading of water-based ink droplets of the conducting polymer poly(3,4 – ethylene dioxy thiophene) doped with polystyrene sulfonic acid (PEDOT/PSS) on a hydrophilic substrate with a pattern of narrow, hydrophobic

surface regions that define the critical device dimension, the channel length L (Fig. 1.a.).

The semiconducting polymer is then deposited either as a continuous film or patterned into an active layer island by ink jet printing selectively over the transistor channel. For the semiconducting polymer we use liquid-crystalline polyfluorene block copolymers, the chains of which can be uniaxially aligned parallel to the transport direction in the transistor to improve mobility [4]. Then a continuous film of gate dielectric is deposited and the gates and gate interconnects are deposited by ink jetting either PEDOT/PSS or patterned from printed metal ink to form the structure shown in Fig. 1.b.

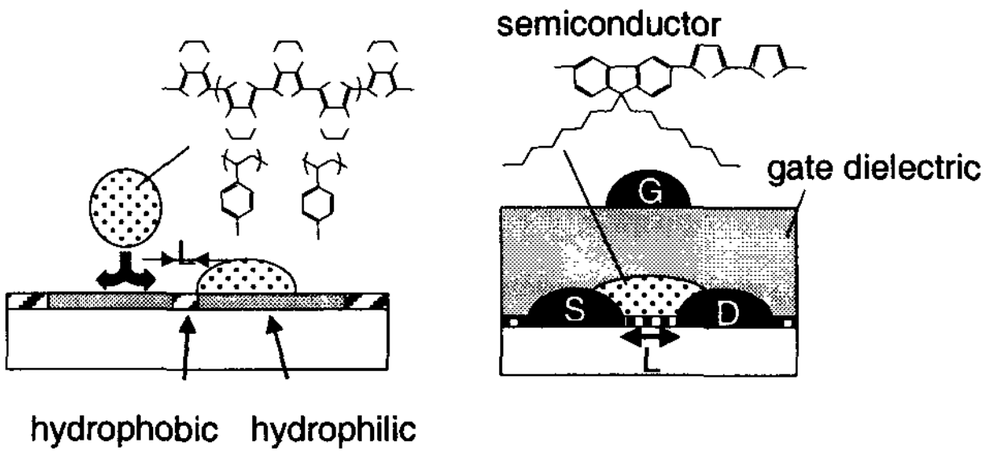

Figure 1: (a) Schematic diagram of high-resolution surface-energy assisted inkjet printing. (b) Cross section of one printed TFT.

2.2 Active Matrix Back Plane Performance

The transfer characteristics for a typical thin film transistor on a printed active matrix back plane is shown in figure 2. The "on" current is ~10^{-7}A at a gate voltage of –40V and a source-drain voltage of –40V. The off current is below 10^{-11}A. The on/off ratio is greater than 10^{4}.

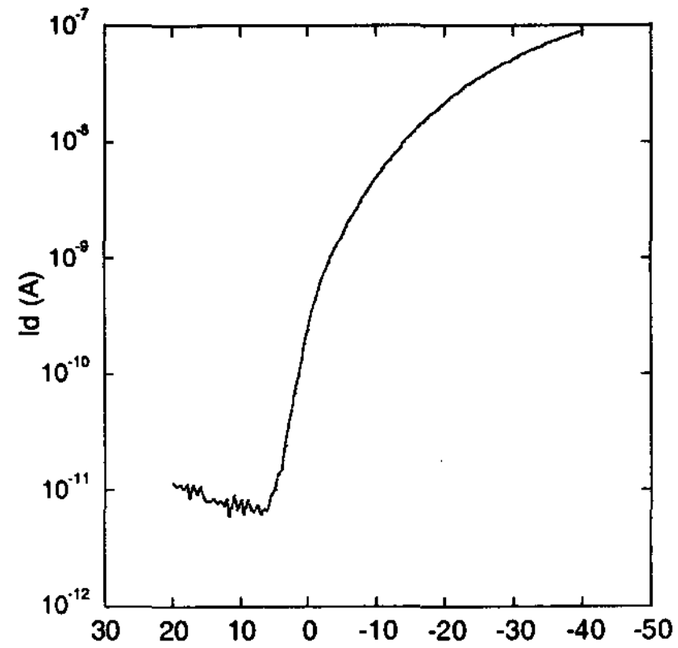

Figure 2. Typical transfer characteristics for a transistor on a printed active matrix back plane.

In order to demonstrate the consistency TFT performance 125 thin film transistors were tested at regular intervals on an active matrix back plane using an automated probe station. Figure 3 shows the On and Off currents, the consistency of which is testimony to the applicability of our print based process.

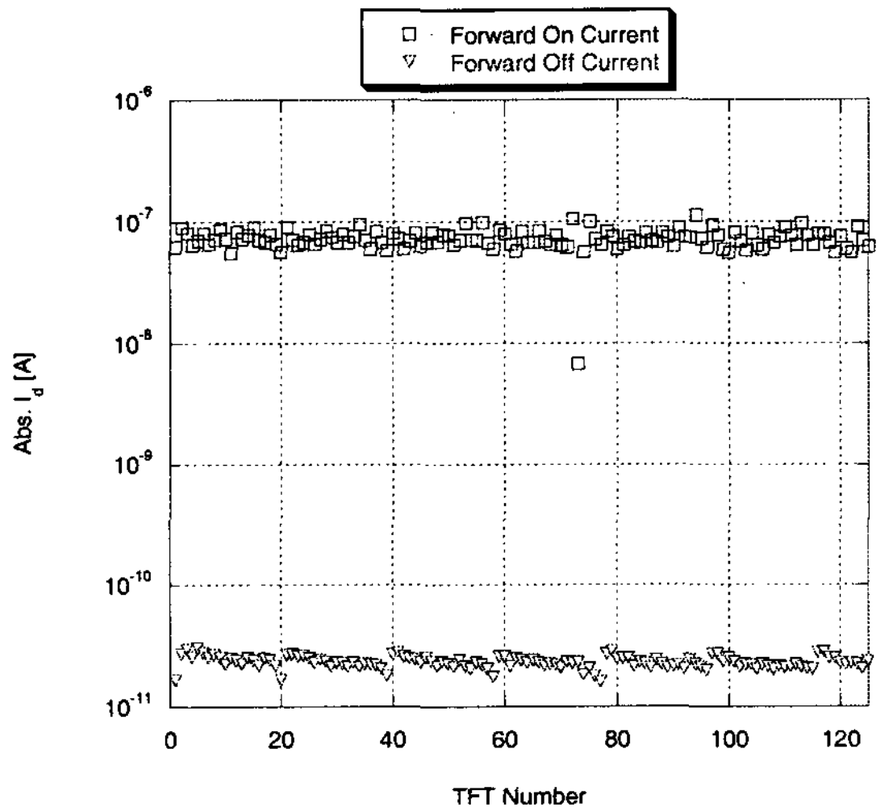

Figure 3. On and Off currents for 125 transistors on a printed active matrix.

2.3 Display Structure and Performance

To fabricate a display, the back plane is laminated with a commercially available PDLC foil. A thin polymer interlayer is first deposited onto the back

plane to protect the transistors from the liquid crystal. The PDLC foil consists of the polymer dispersed liquid crystal emulsion on an ITO coated mylar substrate. Figure 4 shows a schematic of the display after lamination with PDLC, where the ITO layer forms the common top electrode for the display.

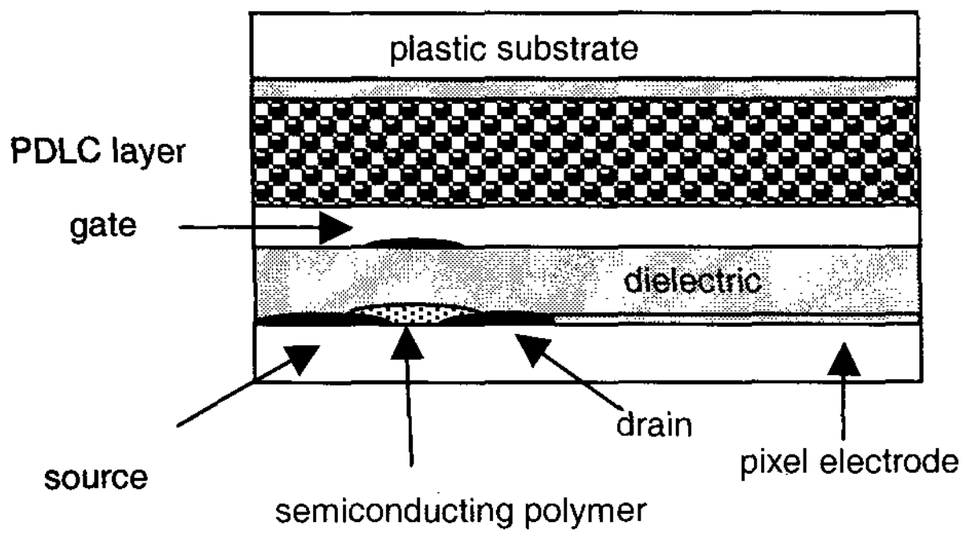

Figure 4: Schematic of active matrix PDLC display showing 1 TFT and 1 pixel in cross section.

With the transistors controlling the voltages on individual pixels, the display is driven with line-at-a-time addressing with a line address time of down to 0.2 ms and frame rate of 80Hz. Figure 5 shows pictures of the 80x60 display in operation. There are no visible pixel defects and the display performance is uniform.

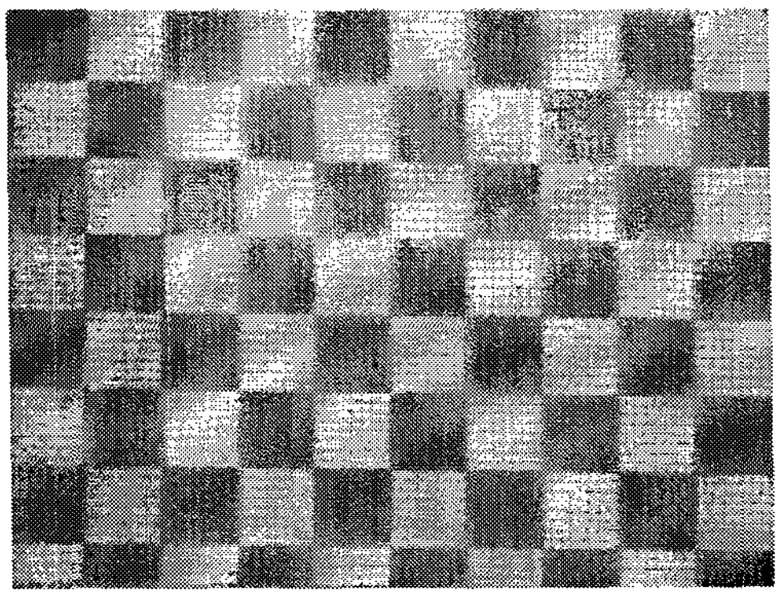

Figure 5. Fully printed display running at 80Hz showing an 8x8 cheque pattern and the company logo.

3. Impact

Using a print based process we have produced 4,800 50 DPI pixel active matrix PDLC displays. Printed back planes can be combined with any voltage controlled display effect such as liquid crystal and electronic paper. It is anticipated that this process will produce active matrix back planes for commercially available displays in the coming years.

4. Acknoledgements

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5. References

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