High Performance TFTs Fabricated Inside a Location-Controlled Grain by Czochralski (grain-filter) Process

Vikas Rana, Ryoichi Ishihara, J.W.Metselaar and C. I.M Beenakker
Delft Institute of Microelectronics and Submicrontechnology (DIMES)
Delft Univ. of Technol., Delft, The Netherlands
Yasushi Hiroshima, Daisuke Abe*, Seiichiro Higashi*, Satoshi Inoue*, Tatsuya Shimoda**
*Technology Platform Research Center, Seiko-Epson Corp., Nagano, Japan
Tel: +31 15 2781651, Fax: 31 15 2622163
Email: v.rana@dimes.tudelft.nl, ishihara@dimes.tudelft.nl
(Invited Paper)

Abstract
This paper reports the characteristics of TFTs, formed inside a location-controlled grain: "single-crystalline" Si TFTs (c-Si TFTs). Position of the grains were controlled with a great precision by "μ-Czochralski (grain-filter) process". Effects of process parameters, such as, deposition method of gate SiO_2, crystallization energy density and position of the channel with respect to the grain filters on TFT characteristics is investigated. It is concluded that the characteristics of TFTs drastically improved by avoiding the grain filter from the channel region. With TFTs having the current-flow direction parallel to radial direction from the grain-filter, electron mobility and subthreshold swing of 600 cm^2/Vs and 0.21 V/dec. respectively are obtained.

1.Introduction
Location-control of large Si grains is an attractive and ultimate approach as TFTs can be formed inside a single grain without electrically active grain boundaries. For realization of integration of system circuits in driver integrated AMLCD, high performance of the TFTs is demanded. The c-Si TFTs fabricated inside a location-controlled grain by μ-Czochralski (grain filter) process showed a very high mobility of 430 cm^2/Vs on average [1]. The rather high subthreshold swing S (0.70 V/dec.) was improved to 0.45 V/dec. by employing a high quality ECR-PECVD SiO_2 as a gate insulator [2]. These characteristic values, however, might be limited by radially grown twin defects inside the grain and by defects near/at the bottom of grain-filter, since the c-Si TFTs were fabricated on top of the grain-filter. Therefore, it is important to find out a position of the channel where characteristics of TFTs are less influenced by these defects, inside a location-controlled grain. The objective of this paper is to investigate the dependence of TFT characteristics on the channel position inside a location-controlled grain.

2. Experiments
The TFTs used in this experiment were fabricated with μ-Czochralski process [3] as follows. Thermally oxidized c-Si wafers were patterned into the grid of 0.75 μm deep cavity with the diameter of 1.0 μm by plasma etching. Subsequently, diameter of the larger cavity was decreased to a final value of below 100nm, by depositing silicon dioxide in plasma-enhanced chemical vapor deposition (PECVD) at 350 °C. Next, a 250nm thick a-Si was deposited by LPCVD using silane at 545 °C. The samples heated at 450 °C were crystallized with excimer-laser (λ=308nm, pulse duration=50ns) with various energy densities. Subsequently, oxygen plasma treatment was carried out. The c-Si TFTs were made with top gate structure having ECR-PECVD SiO_2 (120nm) as a gate insulator, deposited at room temperature and annealed in water vapor at 333 °C [4], Some samples are having low-pressure chemical vapor deposition (LPCVD) SiO_2 as a gate insulator. The source and drain were doped of phosphorus by ion shower using Al gate pattern as a mask, subsequently annealed at 300 °C for four hours in nitrogen ambient. No hydrogenation was done later.

3.Results and Discussions
For investigation of the channel position effect inside a location-controlled grain, as shown in Figure 1, the position of TFT channel having width and length of 2.03μm and 1.87μm respectively, was shifted in X, Y or combination (XY) with respect to the center of grain-filter (C) while the current flow direction was kept to be directed towards the X direction.

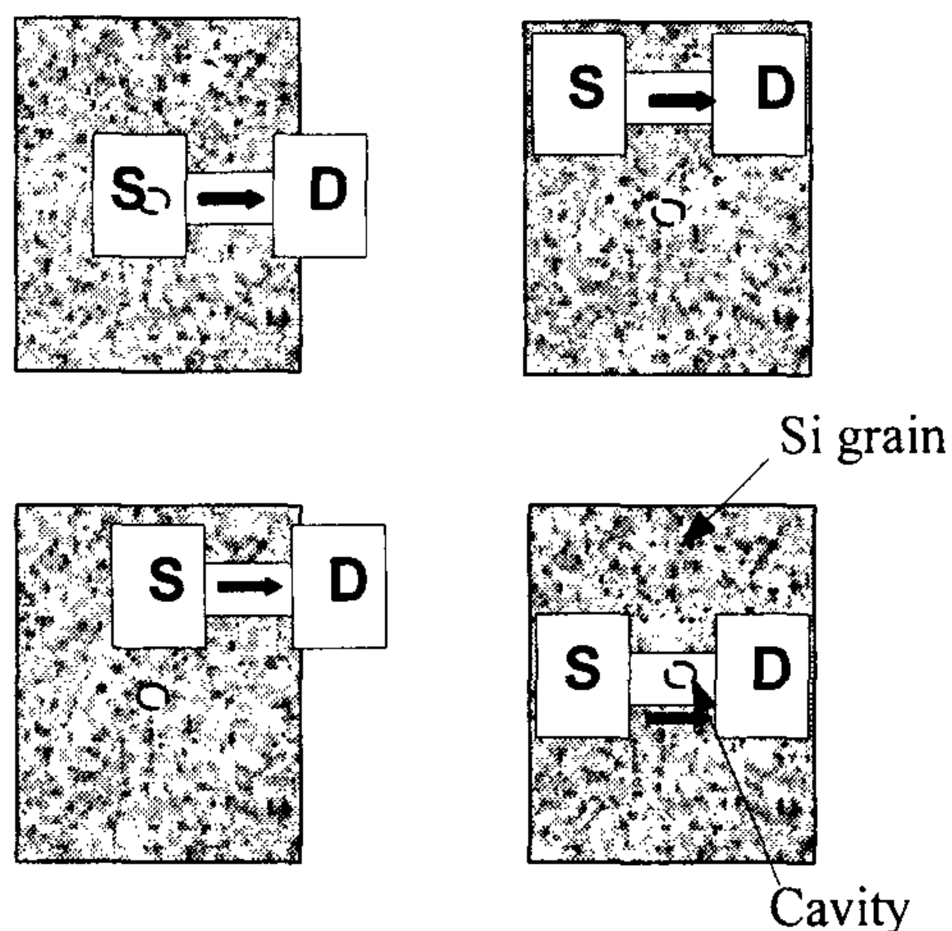

Figure 1 Top view of channel positions of TFT inside the grain

The amount of the channel shift with respect to the center of grain filter is 1.5μm. Figure 3 shows transfer characteristics of the c-Si TFTs having ECR-PECVD SiO_2 as a gate insulator fabricated at the various positions. The energy density of excimer-laser was 1.025 J/cm^2.

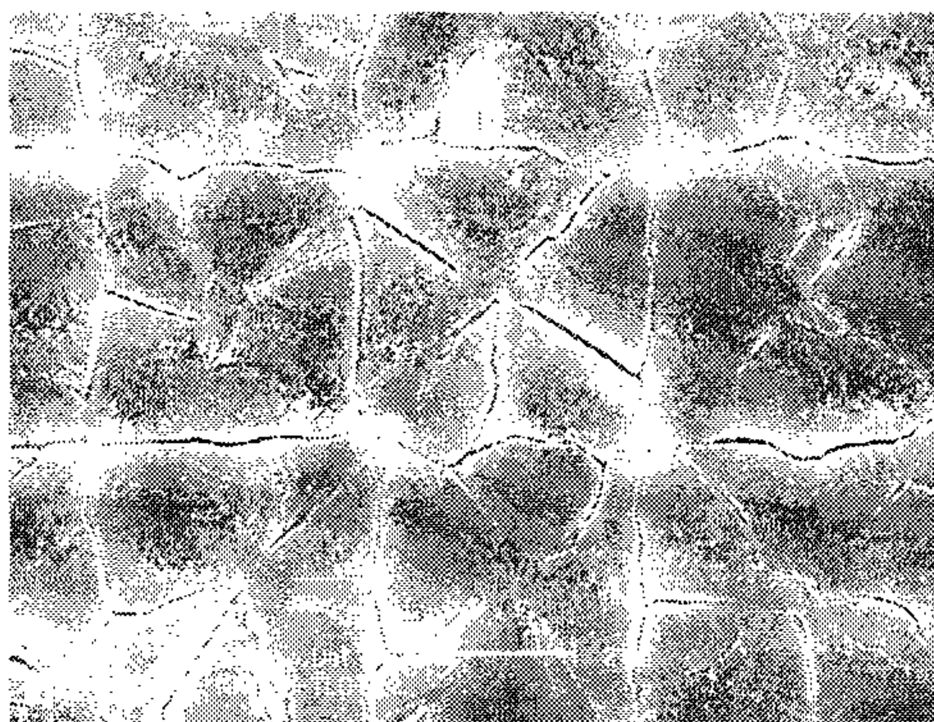

Figure 2 SEM image showing the distribution of planar defects

By shifting the channel position from the top of the grain-filter (C), the transfer characteristics were dramatically improved. Table 1 shows the field effect mobility μ_{fe}, subthreshold swing S, off-current and threshold voltage V_{th} for c-Si TFTs having ECR-PECVD SiO_2 as a gate insulator. It is obvious from the table 1 that c-Si TFTs at the X position give the highest μ_{fe}, lower S, and lower off-current, while c-Si TFTs on the C position give the lowest μ_{fe}, the highest S, and the highest off current.

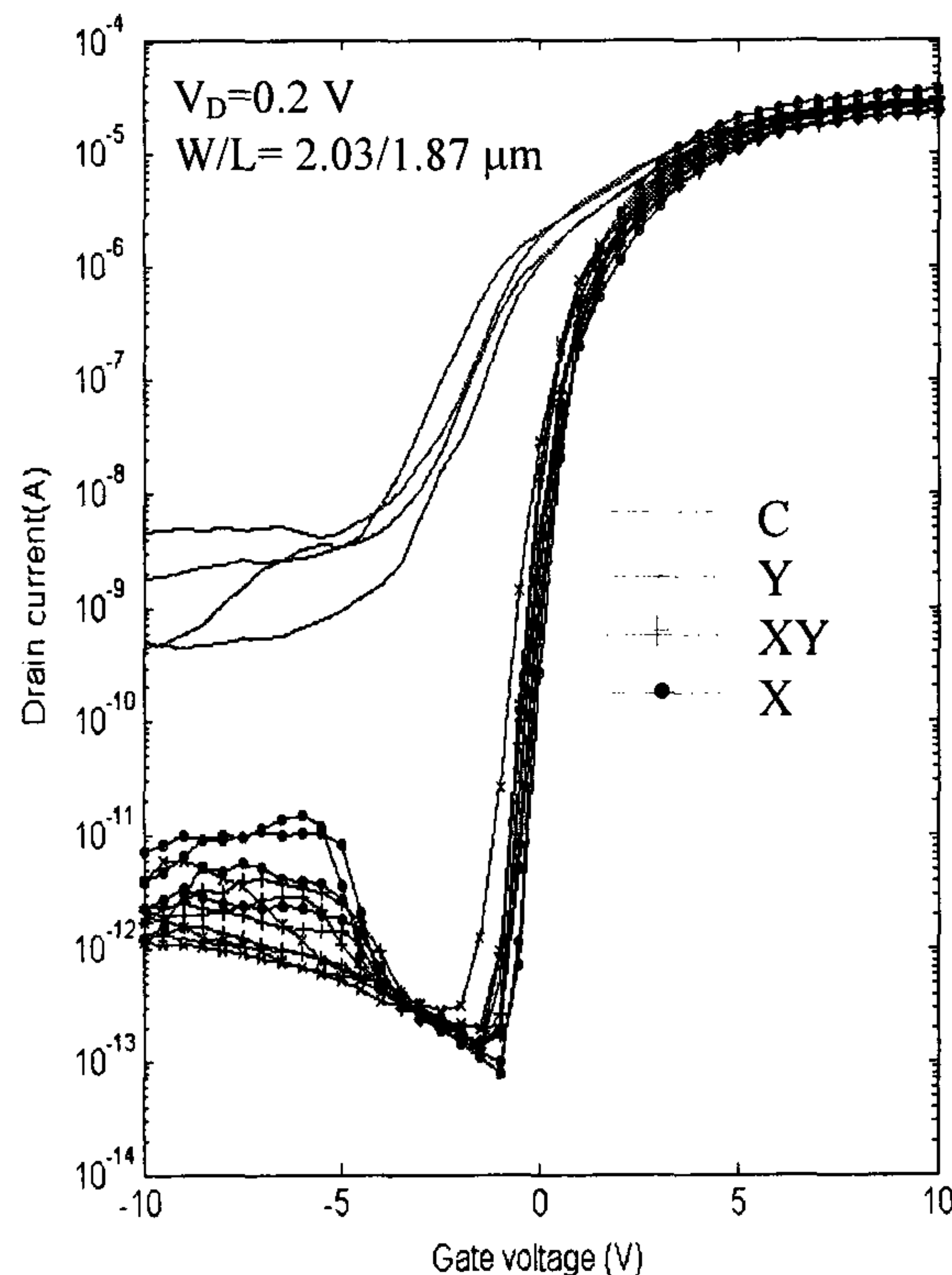

Figure 3 I_D-V_G characteristics of c-Si TFTs at various positions inside a grain-filter having ECR-PECVD SiO_2 as a gate insulator

The high μ_{fe} of the c-Si TFTs (597 cm^2/Vs) at X position is attributed to the fact that the carriers do not experience the twin boundaries because it is parallel to the direction of current flow. The S value and off current of TFTs on the C position are much higher than others, which suggest higher trap states density in the grain-filter. Figure 4 shows the μ_{fe} value as a function of laser energy density for each position of TFTs having ECR-PECVD SiO_2 as a gate insulator. The μ_{fe} value was increased with energy density up to the maximum value. This is because of deeper melt depth and hence decreased planar defects (random or twin grain boundaries), which are generated during crystallization with higher irradiated energy. The mobility slightly decreases with high-irradiated energy densities. This could be because of increased surface or interface roughness.

Table 1 Characteristics of c-Si TFTs having ECR-PECVD SiO_2 as a gate insulator for different channel positions

Channel Position	Mobility (cm^2/Vs)	S (V/dec)	Off-Current (A)*1E-13	V_{th}(V)
X	597 ±121	0.21 ±0.028	1.3 ± 0.53	1.67 ± 0.18
Y	528 ±67	0.25 ± 0.035	1.65 ± 0.77	1.77 ± 0.26
XY	505 ±66	0.22 ± 0.014	1.43 ± 0.095	1.9 ± 0.11
C	471 ±38	1.13 ± 0.13	16800 ± 16900	0.86 ± 0.27

Figure 5 shows S as a function of laser energy density for TFTs having ECR-PECVD SiO_2 as a gate insulator. The similar trend as mobility was observed for the S value except the behavior of TFTs at C: abnormal peak at the moderate energy densities. It is not well understood but this might be attributed to the facts that melt depth reaches void inside the grain-filter, increases the total number of trap states.

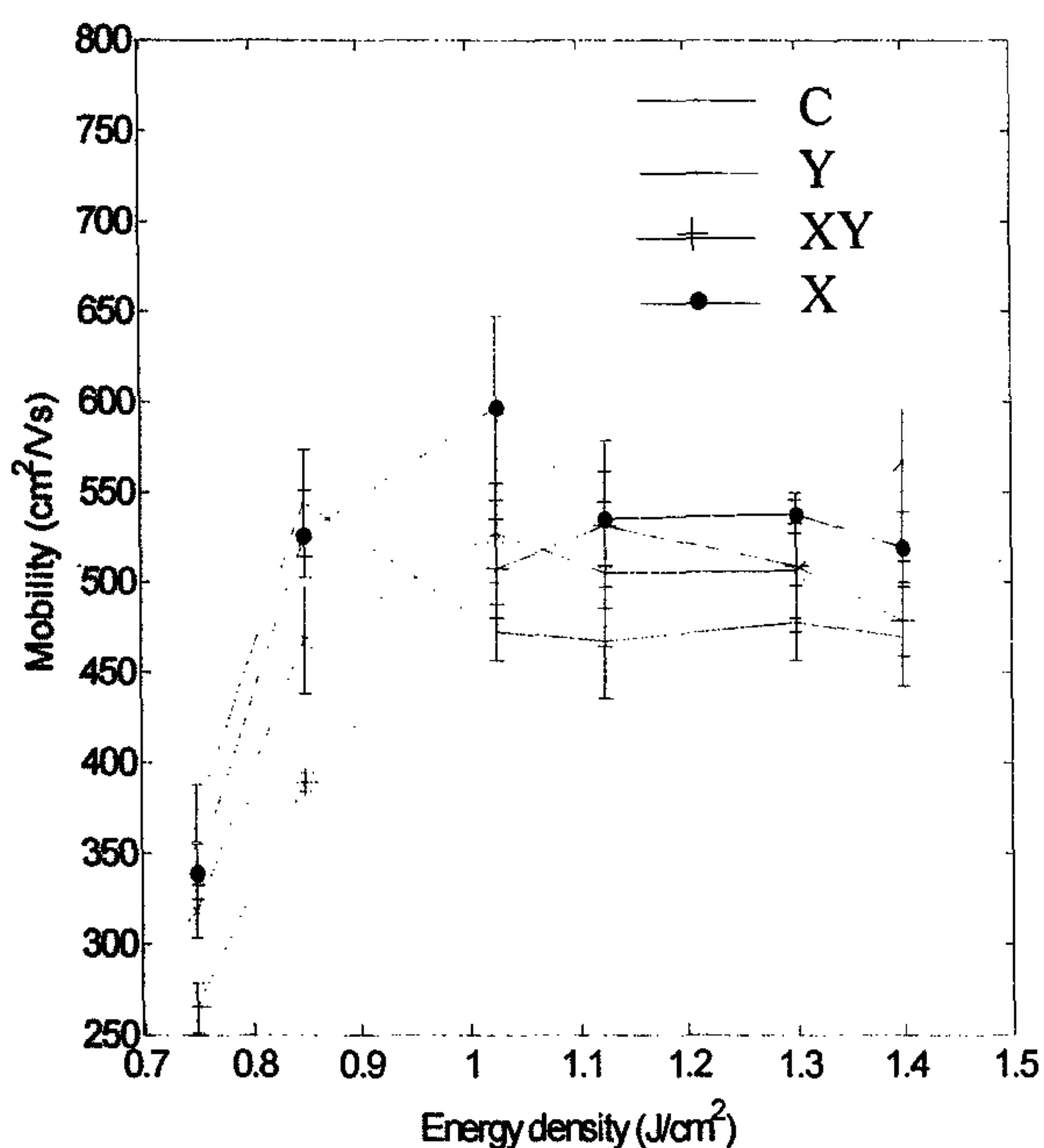

Figure 4 Field effect mobility for electron as a function of laser energy density

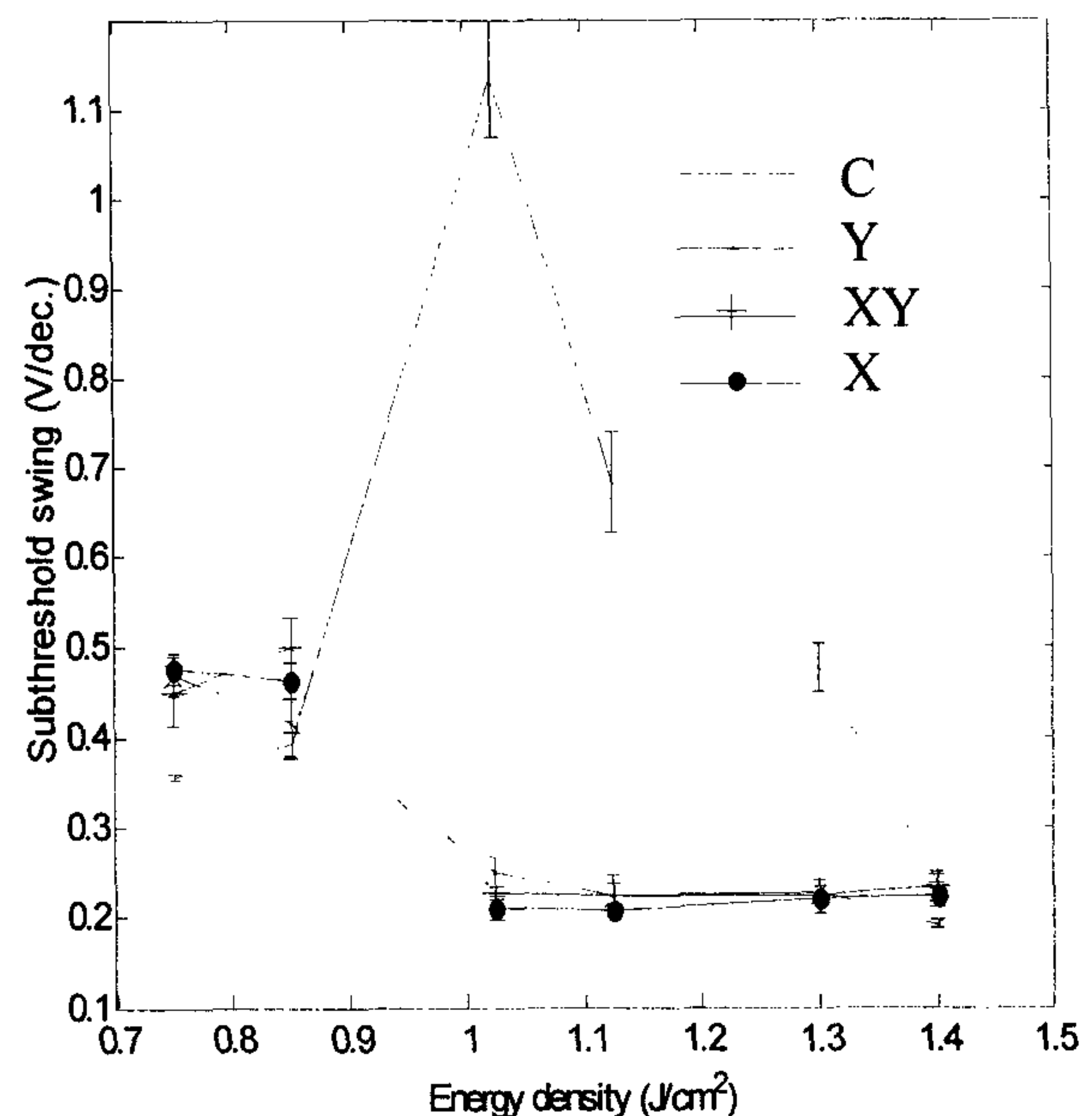

Figure 5 Subthreshold swing for electron as a function of laser energy density

Table 2 shows the μ_{fe}, S, off-current and V_{th} for c-Si TFTs having LPCVD SiO_2 as a gate insulator. There is not much improvement in the characteristics by shifting the channel position from the center of grain-filter. This difference originates from the worse interface characteristics of LPCVD SiO_2, which screens the effects of trap states in the grain filter. The density of interface states for ECR-PECVD and LPCVD SiO_2 are measured to be $2x10^{10}$ and $5x10^{11}$ $cm^{-2}eV^{-1}$ respectively with the C-V characteristics of MOS capacitor [4].

Table 2 Characteristics of c-Si TFTs having LPCVD SiO_2 as a gate insulator for different channel positions

Channel Position	Mobility (cm^2/Vs)	S (V/dec)	Off-Current (A)*1E-13	V_{th}(V)
X	415 ±56	0.59 ± 0.05	20.9 ± 4.4	1.05 ± 0.18
Y	428 ± 100	0.53 ± 0.06	15.3 ± 0.62	0.6 ± 0.37
XY	351 ±68	0.57 ± 0.04	19 ± 3.13	1.03 ± 0.22
C	366 ±69	0.74 ± 0.13	24.8 ± 5.6	0.44 ± 0.48

4.Conclusion

The location-controlled grain by μ-Czochralski process has twin boundaries and random grain boundaries, which impede the flow of current. However we can avoid these defects by positioning the channel with respect to center of grain filter (C) in such way that these defects do not impede the flow of current. By avoiding the grain-filter from the channel region, subthreshold swing was drastically improved to 0.2 V/dec.. This suggests a higher trap state density in the grain-filter. The c-Si TFT, shifted in the current flow direction with respect to the center of the grain filter gave a high mobility of 600 cm^2/Vs successfully. This is because planar defects, which are mainly twin grain boundaries that are often grown radially from the grain-filter, are parallel to the current flow-direction of TFT and that do not impede the carrier motion.

5. Acknowledgements

This work is part of the research program of the Dutch Fundamental Research for Matters (FOM), project number 97TF05, which is financially supported by the Netherlands Organization for Scientific Research (NOW).

6. References

[1] R. Ishihara P.C van der Wilt, B.D.van Dijk, A.Burtsev, J.W. Metselaar and C.I.M. Beenakker, Technical Digest of AMLCD'02, Pg.53

[2] R. Ishihara P.C van der Wilt, B.D. van Dijk, A.Burtsev, J.W. Metselaar and C.I.M. Beenakker, Y. Hiroshima, D. Abe, S. Higashi, S. Inoue, T. Shimoda, Proceedings of Eurodisplay2002, Pg.407

[3] P. Ch. Van der Wilt, B.D. van Dijk, G.J. Bertens, and R. Ishihara, Mater. Res. Soc.Symp. Proc. Vol.685E(2001)

[4] D. Abe, S. Higashi, S. Inoue and T. Shimoda, Technical Digest of AMLCD'01, Pg.49