P2.6

V_{th} Variation Insensitive Current Source and Current Mirror Circuits using poly-Si TFTs

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Abstract

We proposed new current source and mirror circuits insensitive to V_{th} variation of poly-Si TFTs. The proposed circuits have been verified by SPICE simulation using poly-Si TFT model. The error currents of the proposed current source and current mirror circuits caused by V_{th} variation reduced less than 6.6% and 4.5% of that of conventional ones, respectively.

1. Introduction

Low temperature poly-Si(LTPS) thin fim transistor(TFT) has a potential to implement driver circuits on a glass substrate due to a high current driving capability. So there are several researches of poly-Si TFT-LCDs, enhance the integration level from pixel circuits with SRAM[1], DRAM memory[2] to digital data driver[3, 4, 5] and timing controller[6].
However, it is very difficult to design basic analog circuits such as current source and current mirror circuits with poly-Si TFT because of its process variation, especially the variation of the threshold voltage and mobility.
In this paper, we propose new current source and current mirror circuits with insensitivity to variation of threshold voltage of poly-Si TFT. The main concept of the proposed circuits is used in analog buffer which is composed complementary source follower to compensate V_{th} variation in poly-Si TFT[7].

2. The proposed current source and current mirror circuits

Figure 1 (a) and (b) show the conventional current source and current mirror circuits, respectively. In these structure, if threshold voltage of the TFTs(P0, P1 and P2) varies, the circuits can not source(or sink) accurate level of current .
Figure 2 shows the circuit diagram of proposed current source. Compared with the conventional one, four additional switches and one capacitor are used for the circuit in figure 2. Figure 3 shows the driving waveforms of proposed current source circuit. The operation is divided into two phases ; V_{th} detection time and driving time as shown in figure 3. During T1 and T2 in figure 3, V_{th} of P0 is stored on capacitor C0. During T3 in figure 3, the current through P0, I_{bias}, is decided according to gate voltage of P0. I_{bias} is expressed in equation (1).

$$\begin{aligned} I_{bias} &= \frac{1}{2}\mu_P C_{ox}\frac{W}{L}(V_{bias}-V_{dd}-V_{thp}+V_{thp})^2 \\ &= \frac{1}{2}\mu_P C_{ox}\frac{W}{L}(V_{bias}-V_{dd})^2 \end{aligned} \quad (1)$$

As you see, there is no threshold term in this equation. Therefore, the proposed current source circuit is insensitive to threshold voltage variation of poly-Si TFT. Figure 4 shows the proposed current sink circuit, which consist of NTFT.

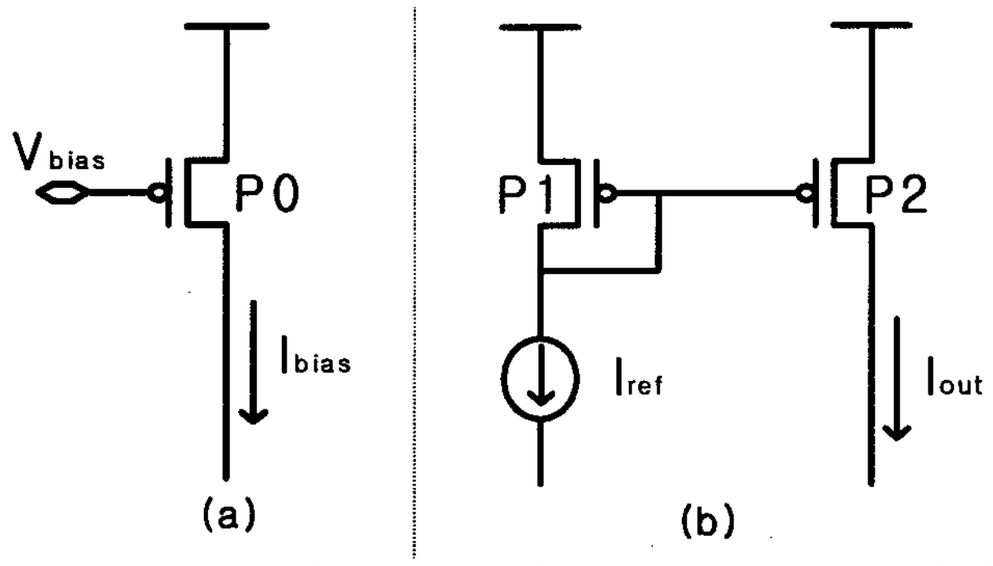

Figure 1. (a) Conventional current source and (b) conventional current mirror circuits.

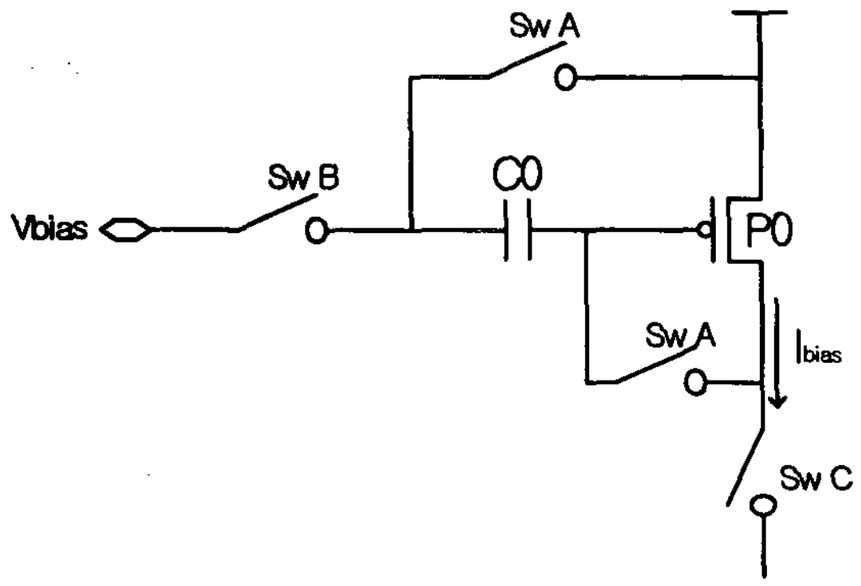

Figure 2. The circuit diagram of proposed current source.

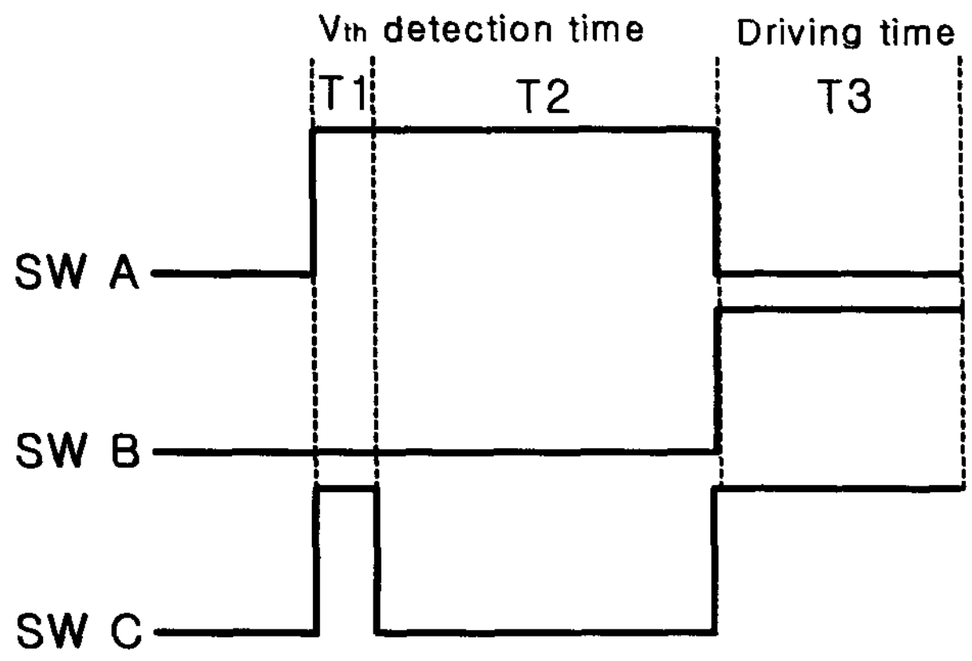

Figure 3. Driving waveforms of proposed current source circuit.

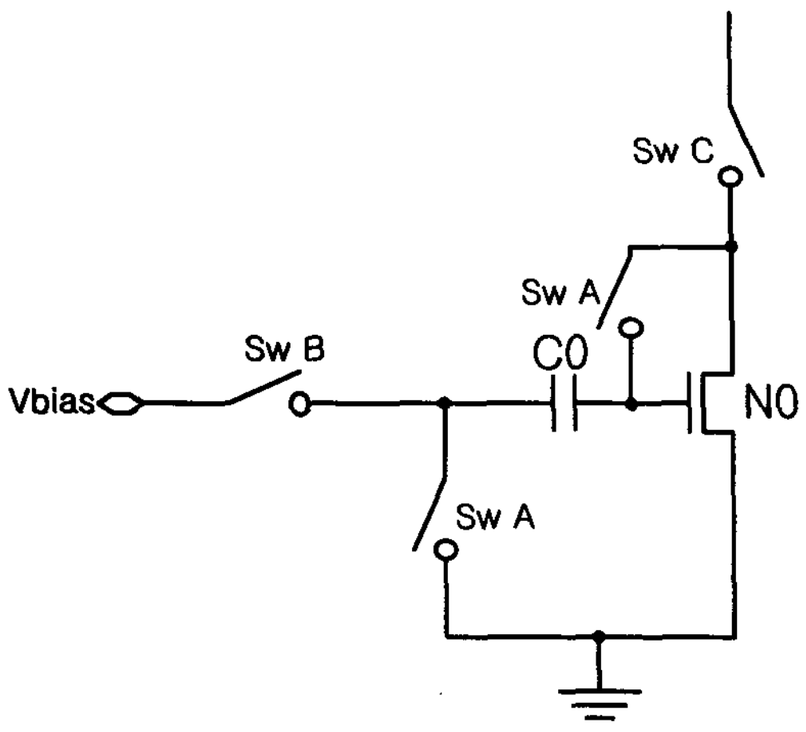

Figure 4. The circuit diagram of proposed current sink, which consist of NTFT.

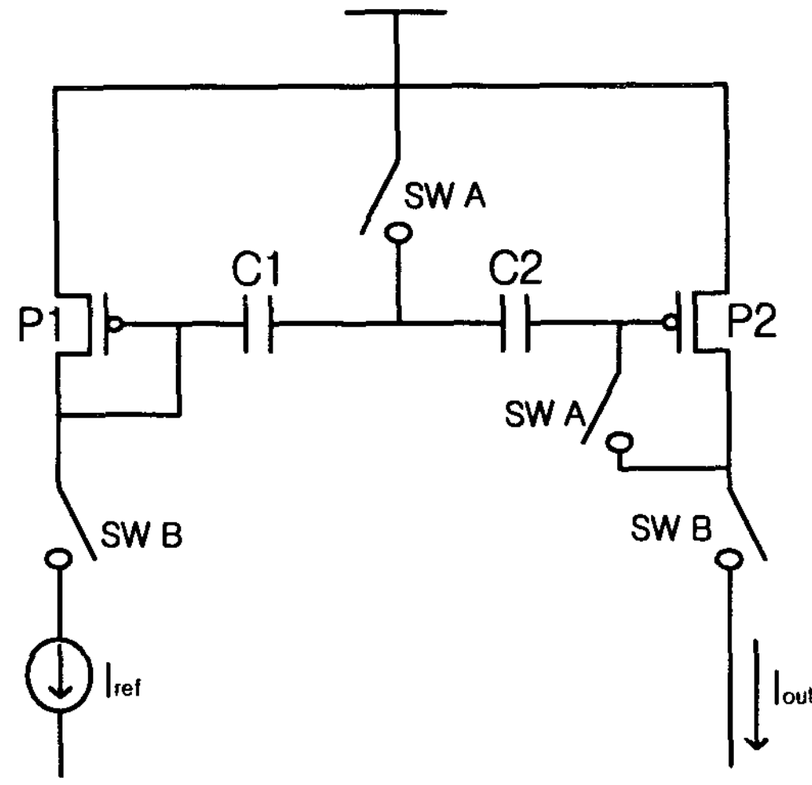

Figure 5. The circuit diagram of proposed current mirror.

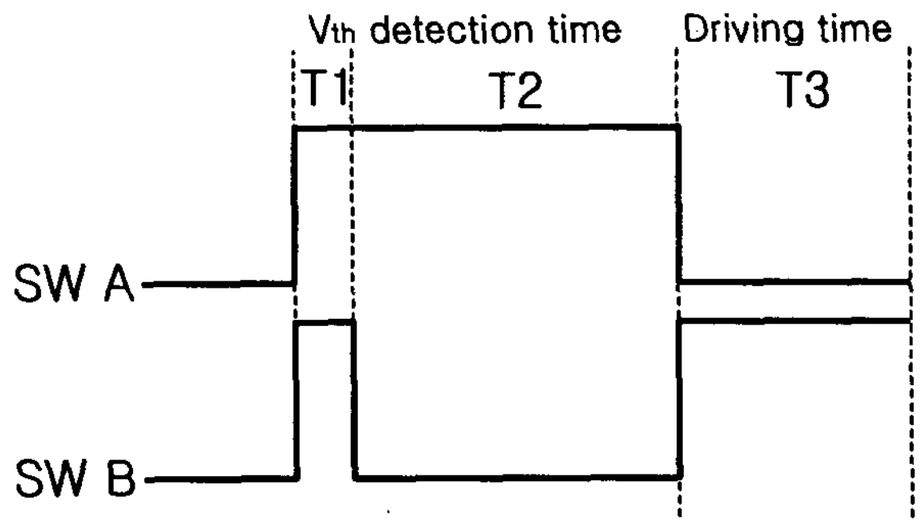

Figure 6. Driving waveforms of proposed current mirror circuit.

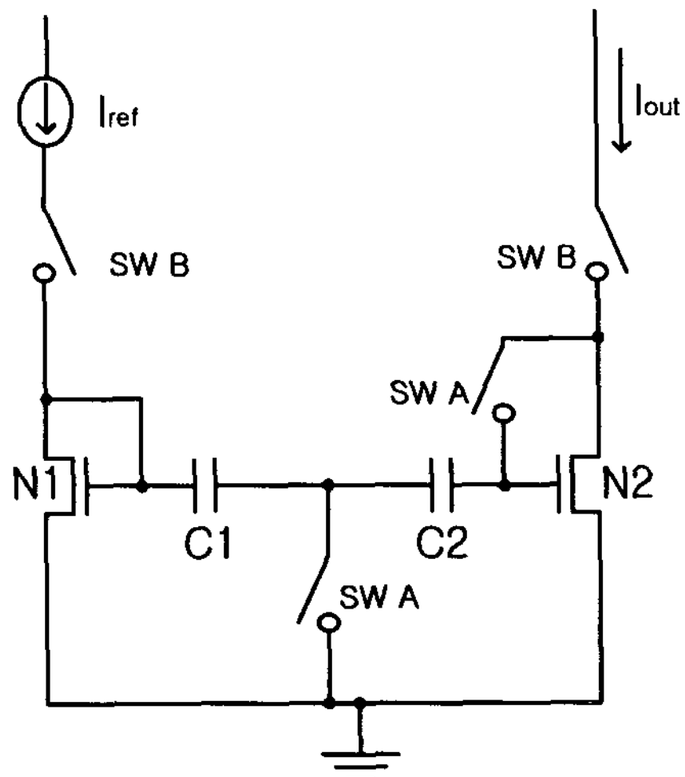

Figure 7. The circuit diagram of proposed current mirror, which consist of NTFT.

Figure 5 shows the circuit diagram of proposed current mirror. Compared with the conventional one, four additional switches and two capacitors are used for the circuit in figure 5. Figure 6 shows the driving waveforms of proposed current mirror circuit. The operation is divided into two phases; V_{th} detection time and driving time as shown in figure 6. During T1 and T2 in figure 6, V_{th} of P1 and P2 are stored on capacitor C1 and C2, respectively. During T3 in figure 6, the current through P2, I_{out}, is decided according to gate voltage of P2. Gate voltage of P2 is the value of adding difference between V_{th} of P1 and V_{th} of P2 to gate voltage of P1.
Therefore, the proposed current mirror circuit is insensitive to threshold voltage variation of poly-Si TFT. Figure 7 shows the circuit diagram of proposed current mirror, which consist of NTFT.

3. Simulation results

Table 1 shows the simulation conditions and figure 8 shows the simulated waveforms of the proposed current source circuit. Under these simulation conditions, the difference of I_{bias} is less than 2μA in proposed current source circuit. On the contrary, the difference of I_{bias} is about 30.5μA in conventional one. Figure 9 shows the simulated waveforms of the proposed current mirror circuit. Under the simulation conditions mentioned in table 1, the difference between I_{ref} and I_{out} is less than 3μA in proposed current mirror circuit. On the other hand, the difference between I_{ref} and I_{out} is about 66.6μA in conventional one.
In conclusion, the error currents of proposed current source and current mirror circuits caused by V_{th} variation reduced less than 6.6% and 4.5% of that of conventional ones, respectively.
The error currents in proposed current source and current mirror circuits are inversely proportional to the value of the compensation capacitor and table 2 shows the output currents of the proposed current mirror circuit according to the value of the compensation capacitor. As you see, the output current becomes more close to reference current(27μA) as the value of the compensation capacitor is bigger. This is because voltage variation in the compensation capacitor resulted from the charge injection and clock feed-through becomes small as the compensation capacitor is bigger.

Table 1. The simulation conditions.

Vdd	16V
Simulation model	poly-Si TFT
Variation of V_{th}	±0.5V
Size of P0	120μm/6μm
The value of C0	1pF
Size of P1, P2	140μm/6μm
The value of C1, C2	Each 1pF
I_{bias} , I_{ref}	27μA
Time of T1	1μsec
Time of T2	5μsec
Time of T3	5μsec
Switch type	Transmission gate

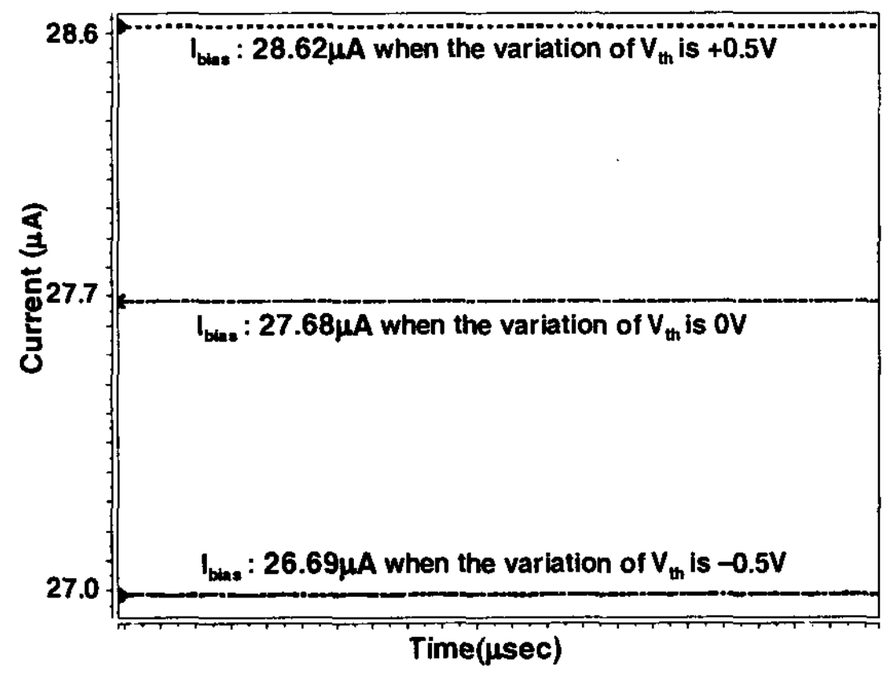

Figure 8. Simulated waveforms of proposed current source circuit.

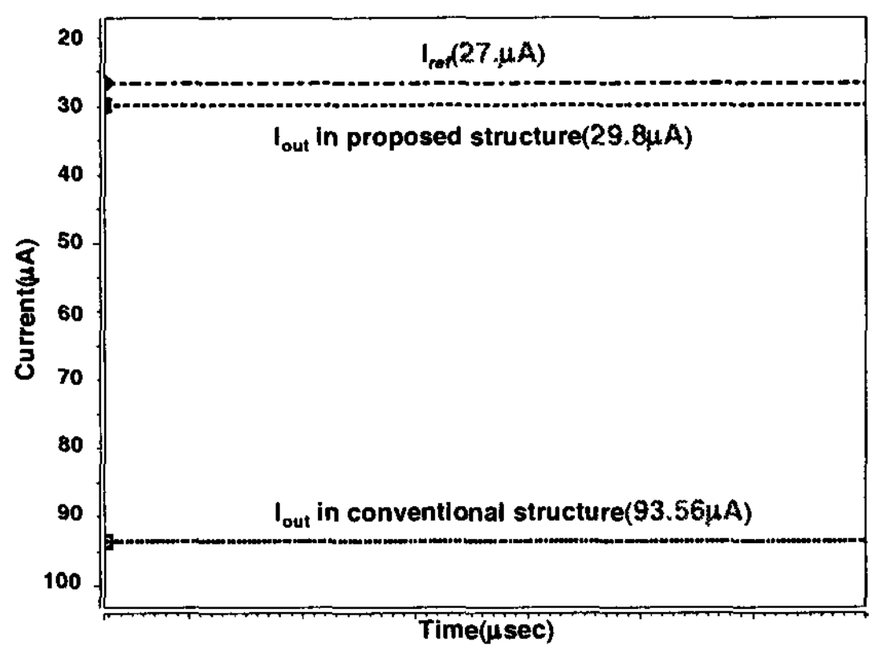

Figure 9. Simulated waveforms of proposed current mirror circuit.

Table 2. Output currents of the proposed current mirror circuits according to the value of the compensation capacitor.

The value of capacitor(pF)	Output current(μA)
0.1	36.8
0.2	35.2
0.3	34.1
0.4	33.1
0.5	32.5
0.6	31.9
0.7	31.5
0.8	31.2
0.9	30.8
1	29.8
2	29.1

4. Conclusions

We proposed new current source and current mirror circuits insensitive to V_{th} variation of poly-Si TFTs. The error currents of the proposed current source and current mirror circuits caused by V_{th} variation reduced less than 6.6% and 4.5% of that of conventional ones, respectively.

5. References

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