Effects of the Deposition Rate of Pentacene Film on the Electrical Characteristics of Organic Thin-film Transistors

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Abstract

Organic thin-film transistors were fabricated using pentacene as an active electronic material. Device characteristics are improved with increasing the deposition rate of pentacene. It is observed that the deposition rate influences on the interface properties between pentacene and polystyrene, and the molecular ordering of pentacene film. In this paper, we report the effects of the deposition rate of pentacene film on the device performance.

1. Introduction

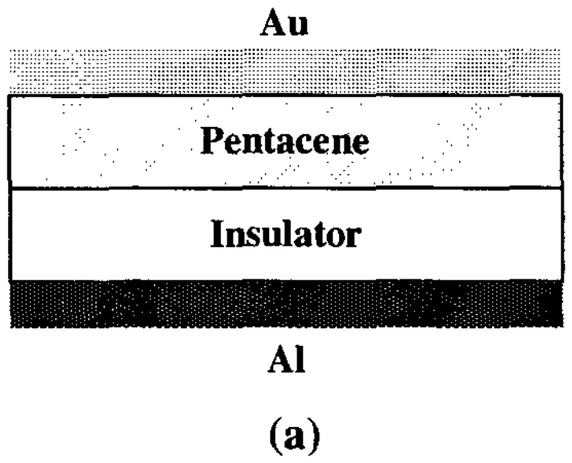
Organic thin-film transistors (OTFTs) are of increasing interest for low-cost display and logic elements. The performance of organic TFTs has been improved dramatically over the past ten years, and optimized organic TFTs show electrical characteristics similar to those obtained with amorphous silicon devices [1]. The main limitation to a larger exploitation of organic TFTs comes from their poor mobility, which at best reaches the level close to that of amorphous silicon TFTs. A further obstacle toward a larger development of organic TFTs comes for their increased complexity with respect to organic light emitting diodes, and in particular to the scarce knowledge of the microscopic charge transport mechanisms that affect the device characteristics [2].

It has been reported that pentacene shows the most pronounced properties for *p*-channel conduction, among many organic semiconductors [3], [4]. And the best performance for pentacene-based TFTs is usually obtained by employing high quality single crystalline pentacene films grown at low deposition rate. However, amorphous pentacene films grown at high deposition rate may exhibit yet unexplored transport properties [5]. Moreover, the effects of deposition rate of pentacene on the device performance are rarely studied. In this paper, we will report on the correlation between the deposition rate of pentacene and the device characteristics.

2. Experimental

In this paper, two kinds of devices were fabricated and are shown in Fig. 1. One is the metal-insulator-semiconductor (MIS) structure, Al/polystyrene (2500 Å)/pentacene (650 Å)/Au, and the other is the top contact TFT. The MIS devices were fabricated and the *C-V* characteristics were measured for different deposition rates of pentacene layer. As a gate electrode, 1500 Å-thick Al layer was thermally deposited on the glass substrate. The gate dielectric, 2500 Å-thick polystyrene (1 wt% in chloroform) layer was formed by spin-coating, and baked at 90 °C for 5 min. and consecutively at 95 °C for 1 hr in a vacuum dry oven. Pentacene film as an organic semiconductor layer was deposited at rates of 0.5, 1.0, and 2.5 Å/sec, and its thickness was about 650 Å. For the source and drain contacts, Au was thermally evaporated. All the deposition processes were carried out at a base pressure of about 1.6×10^{-6} Torr. The channel length and width are 150 μm and 5 mm, respectively. The MIS devices were also fabricated according to the above-mentioned TFT processes.

The current-voltage (*I-V*) characteristics were measured with Keithley 238 and 651 source-measurement units, and the *C-V* characteristics were performed using HP 4192A LF impedance analyzer. All the measurements were performed in the dark and shielded condition. The atomic force microscopy (Park Scientific Instrument) was used to investigate the morphological characteristics of pentacene films.



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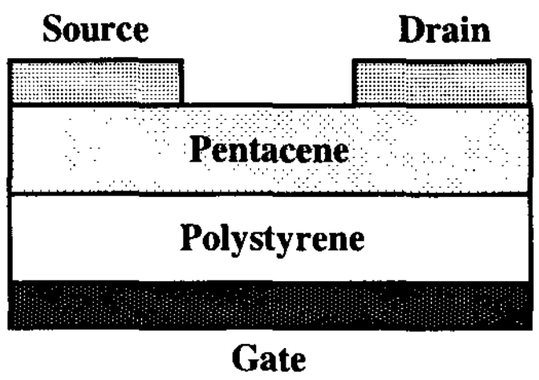

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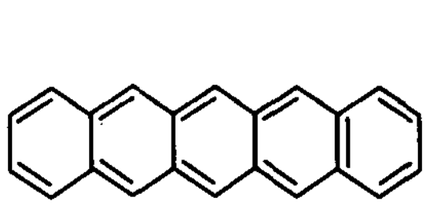

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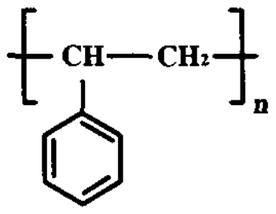


(d)

Figure 1 Schematics of (a) the MIS structure, (b) the fabricated organic TFT, (c) pentacene, and (d) polystyrene

3. Results and discussion

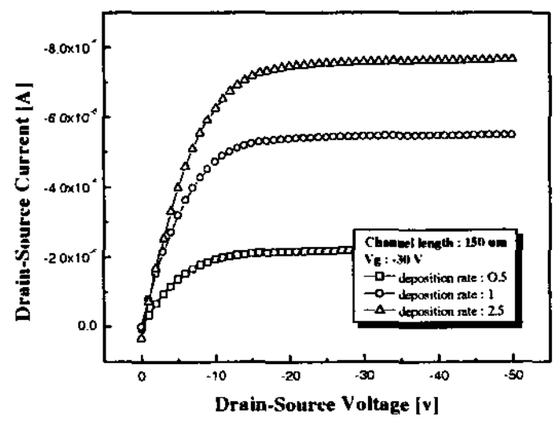
3.1 Current-Voltage Characteristics

The drain current density of the fabricated devices as a function of the drain voltage at the gate voltage of -30 V is shown in Fig. 2 (a). The drain current density of the fabricated devices as a function of the gate voltage at the drain voltage of -30 V is shown in Fig. 2 (b). The field-effect mobility is extracted from Fig. 2 (b) using the saturation drain current equation (1):

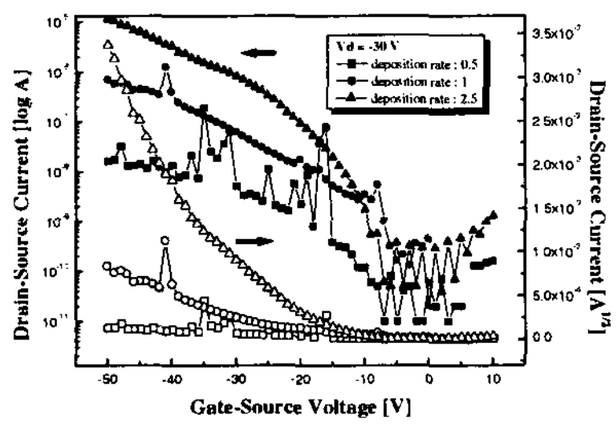
$$I_{D,sat} = \frac{W\mu_{eff}C_i}{2L}(V_G - V_T)^2 \quad (1)$$

where W is the channel width, μ_{eff} is the field-effect mobility, C_i is the capacitance of the insulating material per unit area, L is the channel length, V_G is the gate voltage, and V_T is the threshold voltage [6]. For different deposition rates of pentacene layer, μ_{eff} of the fabricated TFTs ranges from 2.0×10^{-5} to 0.16 cm^2/Vs and the device with the pentacene layer deposited at 2.5 Å/s shows the largest mobility value about 0.16 cm^2/Vs. The saturation current ($I_{D,sat}$) is increased with the deposition rate of pentacene and the device with the pentacene layer deposited at 2.5 Å/s shows the highest saturation current value, -7.6 μA. And the highest on/off current ratio about 10^5 was also obtained for the device with the pentacene deposited at 2.5 Å/s. Device characteristics are summarized in

Table I.



(a)



(b)

Figure 2 Measured (a) output and (b) transfer characteristics

Table I. Electrical properties of TFTs with different deposition rates

Deposition rate	μ_{eff} [cm^2/Vs]	on/off current ratio
0.5 Å/s	2.0×10^{-5}	10^3
1.0 Å/s	4.1×10^{-3}	10^4
2.5 Å/s	1.6×10^{-1}	10^5

3.2 Capacitance-Voltage Characteristics

The *C-V* characteristics of the pentacene MIS capacitors were measured to investigate the pentacene layer and interface properties. For the measurements, a small signal with 1 MHz frequency and 10 mV amplitude was superimposed to the DC bias. The measured *C-V* characteristics are described in Fig. 3. It is observed that the capacitances are decreased and saturate to certain values with the applied bias, which indicates that a depletion region exists at the pentacene and insulator interface, and becomes fully depleted under the biases above -1.4, -0.4, and 7.4 V for the devices with the pentacene deposited at 0.5, 1.0, and 2.5 Å/s, respectively. And the capacitances are decreased with the deposition rate of pentacene layer and the lowest value of about 0.375 nF is obtained for

the device with the pentacene layer deposited at 2.5 Å/s, which might be attributed to the influence of the polystyrene/ pentacene interface properties. The minimum capacitance is expressed by equation (2):

$$C_{\min} \cong \frac{\varepsilon_i}{d + (\varepsilon_i / \varepsilon_s) W_{\max}} \quad (2)$$

where ε_i is the permittivity of the insulator, ε_s is the permittivity of the semiconductor, d is the thickness of the insulator, and W_{max} is the maximum width of the depletion region [7], [8]. The lowest capacitance value of 0.375 nF corresponds to the maximum depletion region width of about 154 Å.

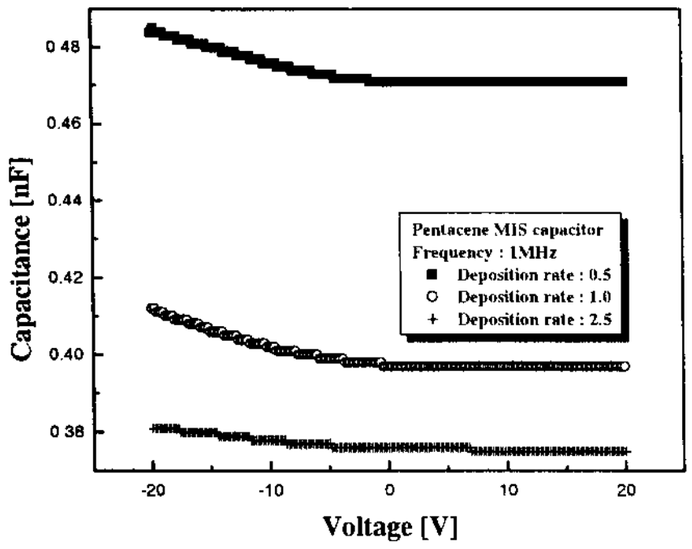


Figure 3 The *C-V* characteristics for pentacene MIS capacitor, according to the deposition rates

From the result of the *C-V* measurements, it can be stated that the deposition rate of pentacene layer has critical effects on the interface properties and the charge transport in pentacene layer. Increasing the ordering of the pentacene molecules has proved to be paramount to maximizing TFT efficiency [9]. However, it is reported that characteristic improvement was obtained for the devices with fast deposition conditions, even though crystalline quality of pentacene was deteriorated by increasing the deposition rate [5]. One possible explanation is the degree of purity of the deposited pentacene layers at different rates, because the deposition rate of pentacene was controlled by the applied temperature to unpurified pentacene powder. Therefore, further investigations are required for a clear understanding of the effects of the deposition rate on the device performance.

3.3 Morphological Characteristics

Atomic force microscopic images were obtained to investigate the effects of deposition rate on the morphological characteristics of the deposited pentacene films as shown in Fig. 4. Upon the investigations, the surface morphology of pentacene on polystyrene becomes smoother as the deposition rate is increased. Detailed roughnesses of the pentacene layer surface are summarized in Table II. And it is also observed that the grain size of pentacene film becomes a little bit smaller with increasing the deposition rate, which shows that pentacene molecules can be stacked with different ordering affected by the deposition rate. Further investigations on the ordering of pentacene films with varying the deposition rates are required.

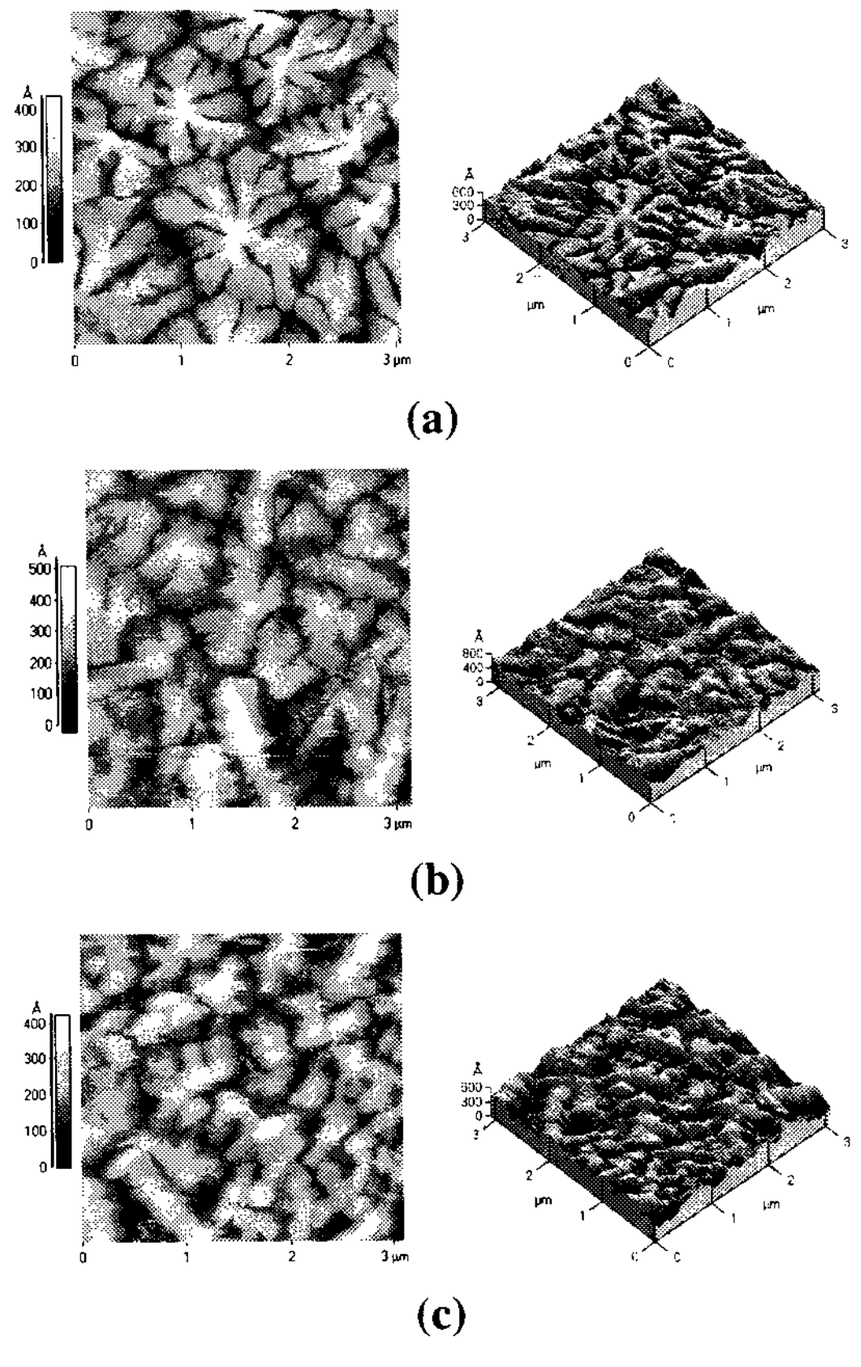


Figure 4 AFM images of pentacene deposited at (a) 0.5, (b) 1.0, and (c) 2.5 Å/s

Table II. Morphological characteristics

Deposition rate	Root-mean-square roughness	Average roughness
0.5 Å/s	59 Å	47 Å
1.0 Å/s	52 Å	42 Å
2.5 Å/s	43 Å	36 Å

4. Conclusion

Effects of the deposition rate of the pentacene layer on the TFT performance were studied. It is observed that the electrical characteristics of organic TFT were improved with increasing the deposition rate, which may be attributed to the different interfacial features between polystyrene and pentacene, because the characteristics of organic TFTs can be controlled by the interface properties. Using AFM images and capacitance-voltage characteristics, we can also confirm that the initial growth mode of pentacene can be modified by the deposition rate. For the further remarks, investigations for transport properties and trap distribution in pentacene are in progress, which will be related to the pentacene deposition conditions. And the molecular ordering of pentacene film with varying the deposition rate will be investigated.

5. Acknowledgements

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6. References

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