High Current Stress characteristics on Sequential Lateral Solidification (SLS) Poly-Si TFT

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Abstract

The reliability of TFT, crystallized by sequential lateral solidification (SLS) technology, has been studied High current damage is characterized by high gate bias (-20V) and drain bias (-10V). It is found that performance of SLS TFTs is enhanced by high current stress up to 300 sec of stress time for 20/8 (W/L) N-TFT. After that, TFT performance is degraded with the increase of the stress time. It is speculated from the experimental data that SLS TFTs initially contain a number of unstable defect states. Then, the defect states seem to be cured by high current stress.

1. Objectives and Background

SLS TFTs exhibit high mobility and driving current over Excimer Laser Annealing (ELA) TFTs. High current damage and hot carrier stress needs to be addressed to verify the reliability of high TFT performance. High current damages of SLS TFTs are only studied on this report.

2. Results

Fig.1 shows that mobility is increased as stress time is increased. Initial mobility is measured at 120 Vsec/cm2. However, mobility keeps increasing with stress time and is turned out to be 260 Vsec/cm2 after 30000 sec stress. The trap sites at the grain boundaries are stabilized by capturing mobile electrons, which, in other words, is called current curing effect. The slope of threshold voltage can be differentiated by two regions before and after 300 sec. The current curing effect occurs less than 300 sec as shown in Fig. 1. The threshold voltage increases rapidly after 300 sec. The high current damage takes over the current curing effect and dominates after 300 sec stress time.

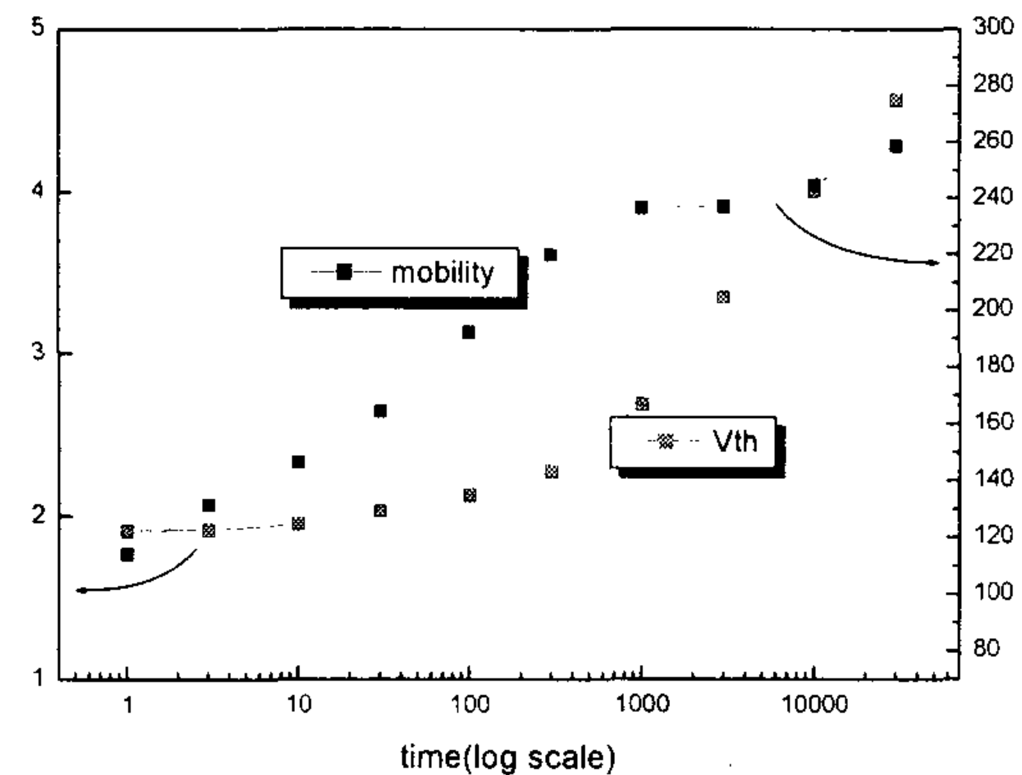

Fig.1 Mobility and threshold voltage under high current stress.

Fig.2 depicts current behavior under high current stress. Although the drain current of SLS TFTs varies with stress time, overall current driving ability shows superior to that of ELA TFTs. It is interestingly observed that SLS TFTs with the channels across grain growth direction and P-TFTs are not affected by high current stress.

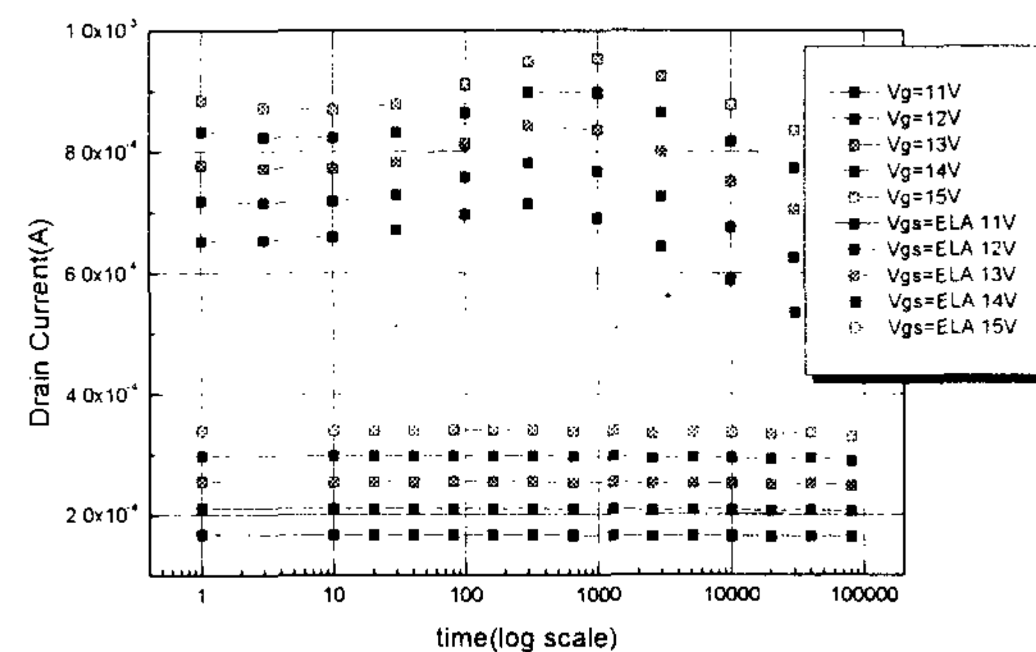

Fig.2 Current behavior under high current stress.

We will compare ELA and SLS TFT behavior and the detail observation and characteristics of high current stress will be discussed at the conference.