P2.18

Design of Low Power TFT-LCD Data Driver and Analog Buffer for Mobile Devices

Jong-Hoon Kim, Seong-Joong Kim, Hyun-Sook Shim, and Oh-Kyong Kwon
Division of Electrical and Computer Engineering, Hanyang University
17 Haengdang-dong, Seongdong-gu, Seoul, Korea
Phone : +82-2-2297-0139, E-mail : okwon7@chol.com

Abstract
This paper describes two kind of new concept for low power consumption for small area TFT-LCDs. First, the proposed analog buffer could reduce the static current by adopting new scheme. Second, new data driver structure reduced DC power consumption by reducing the number of operational amplifier (op-amp). As simulation results of Hspice, the quiescent current of proposed analog buffer is less than 0.8μA and the DC power consumption is reduced about 40~50% compared with conventional ones.

1. Introduction
Low power consumption is getting more and more important for data drivers of TFT-LCDs, since they are expanding the territory to a variety of mobile applications such as IMT-2000 terminals and PDAs. So, various methods to reduce the power consumption for TFT-LCDs have been proposed[1]. In addition, smaller driver are generally more desirable because of the low cost associated with chip size.

The data driver consumes mainly two kinds of powers; DC power by quiescent current of op-amps and ac power for charging/discharging data lines of the panel[2]. However, a TFT-LCD for a small area generally has a small number of pixels, so that the ac power is relatively low. Accordingly, the ratio of dc power to total power remains high in the data driver for small area a-Si TFT-LCDs.

Therefore, we have investigated the data driver structure and analog output buffer with low static current in small area a-Si TFT-LCDs for portable devices. The data driver structure could reduce DC power consumption by decreasing the number of op-amps, furthermore accomplished the low cost and highly uniform image quality. And we have designed a new low-quiescent-current buffer in the conventional data driver structure.

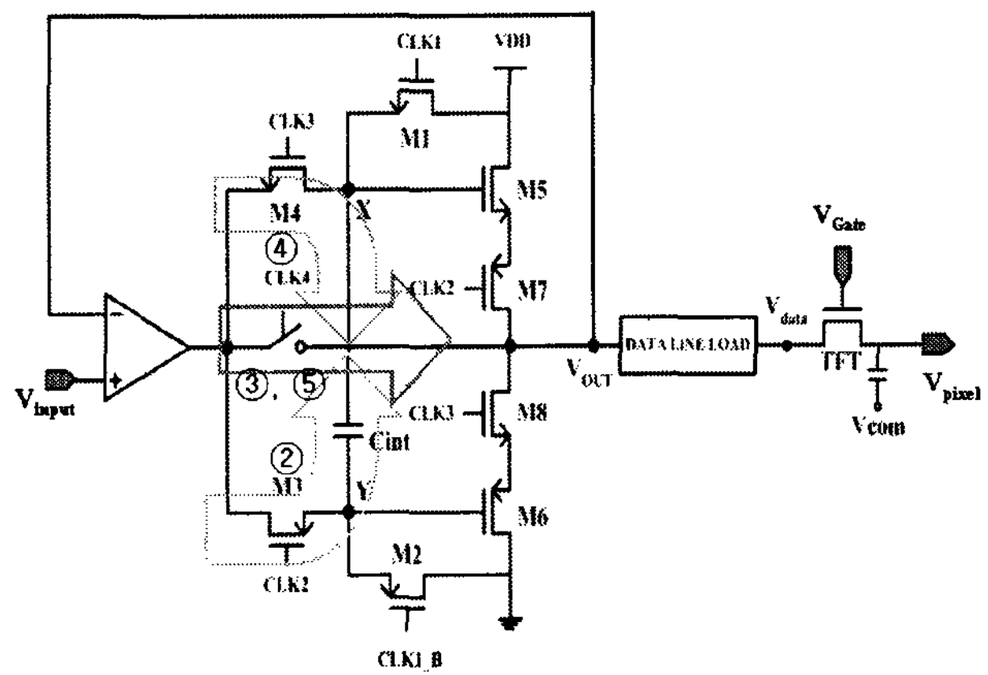

Figure 1. Circuit configuration of proposed analog buffer.

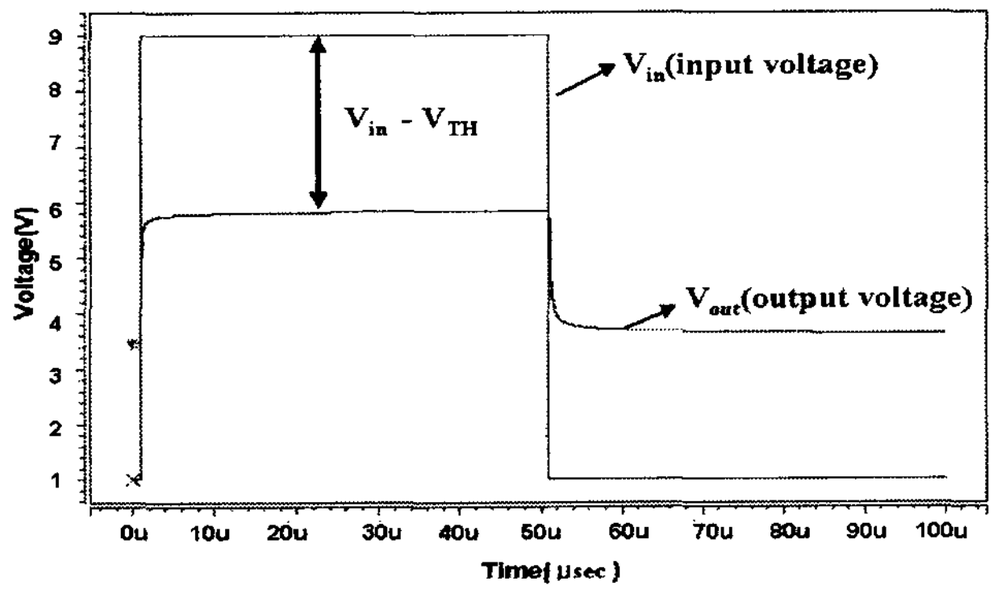

Figure 2. Output waveform of conventional source follower type buffer.

2. The proposed of analog buffer

2.1 The low power concept of new analog buffer
Figure 2 shows the schematic diagram of proposed analog buffer. The proposed analog buffer is composed of one stage op-amp and a modified class-B type circuits containing 1 capacitor and 8 transistors additionally.
The analog voltage relevant to the gray scale level at

the pixel of TFT-LCD is applied to the analog buffer. However, they consume a great deal of DC power because of the output buffers with high static current. The high static current is necessary for the op-amps to maintain high speed and stability. So, the conventional 2-stage op-amp isn't suitable for analog buffer of low power data driver for TFT-LCDs because of the large quiescent current of its output stage. And the conventional source follower type analog buffer has no static current, however, it is difficult to use for analog buffer of data driver because the output voltage of its is equal to $V_G - V_{TH}$, where V_G is the gate voltage of MOSFETs and V_{TH} is represented in equation (1). The output waveform of conventional source follower type analog buffer is shown Figure 1.

$$V_{TH} = V_{TH0} + \gamma(\sqrt{|-2\Phi_F + V_{SB}|} - \sqrt{|-2\Phi_F|}) \quad (1)$$

where V_{TH0} is the threshold voltage for V_{SB}=0, V_{SB} is the source to body voltage difference and γ is body effect coefficient.

In addition to, the source follower type configuration compensating the threshold voltage [3,4] is not proper because of body effect of MOSFET transistors.

The principles of proposed analog buffer is as following. The output load is pre-charged up to some voltage which is proportional to input video signal voltage by modified class-B type buffer having no static current. Therefore, the voltage of output load is fitted in video signal voltage by one-stage op-amp having very low static current because it is not output stage. Accordingly, this buffer can reduce the static current.

2.2 Operation and simulation results

Figure 3 shows the timing diagram of control signal to this buffer and output waveform. The proposed analog buffer requires 5-phase operation for charging and discharging data lines of panel. In other words, the data of positive polarity and the data of negative polarity are written in the panel during 5-phase operation. At the first phase(in ①), when clk1 is high, M1 and M2 are turned on and C_{int} is pre-charged for some voltage between supply voltage and ground. This phase doesn't need to repeat every two row line time, only it may be active once in one or two frame period. At second phase(in ②), either M3 or M4 is turned on according to the polarity of input signal. For positive polarity, M3 is turned on. In case of the input signal as figure 3(a), M3 and M7 are turned on and the voltage of X node(V_x) is pulled-up to $V_{Cint} + V_{in}$. The voltage of output load is charged to $V_x - V_{th}$ by M5. In third phase (in ③), both M7 and M8 are turned off and one-stage op-amp drives the output load up to input video signal accurately. At fourth phase (in ④), M4 is turned on and V_Y(the voltage of Y node) is pulled down. At last phase(in ⑤), the circuit operates as same as third phase.

In order to verify proposed analog buffer, we assume simply 2KΩ resistance and 20pF capacitance as data line load in case of the 2-inch QVGA [240×3(RGB)×320] resolution. For dot inversion, the positive polarity voltage ranges are from 6V to 9V and the negative ones are from 1V to 4V.

Figure 4 shows the Hspice simulation result of

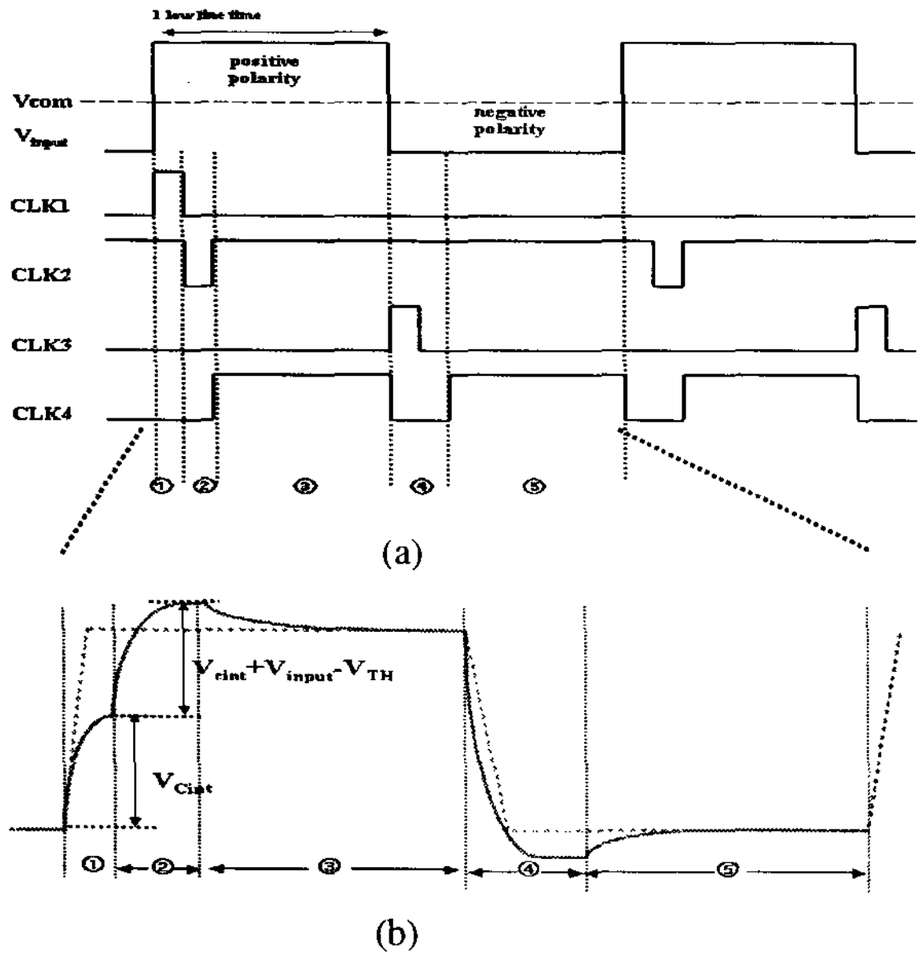

Figure 3.(a)Timing diagram of control signal and (b)output waveform.

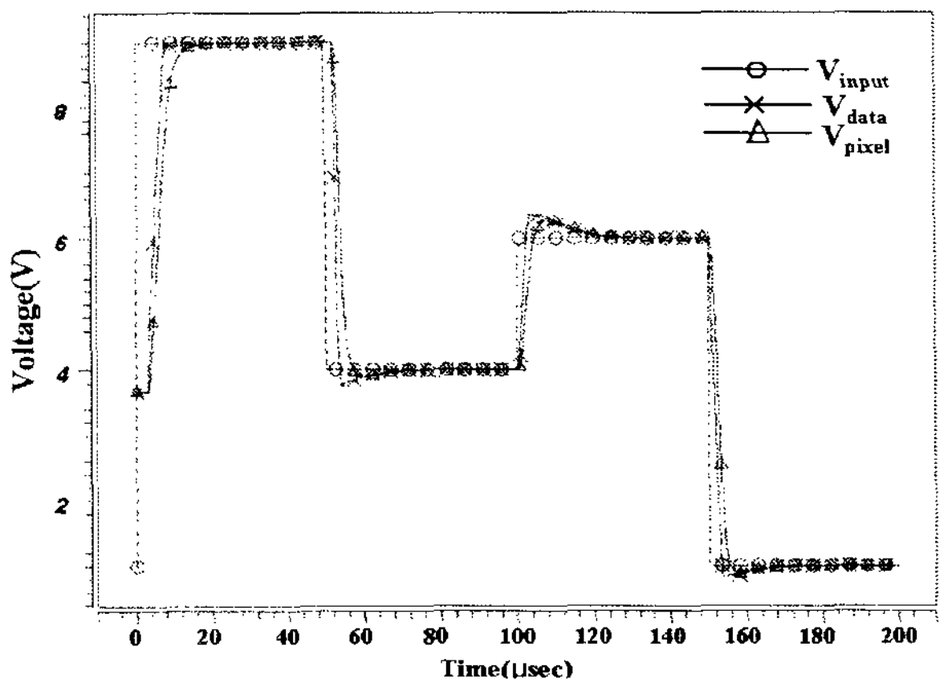

Figure 4. The simulation result of proposed analog buffer about the various transition voltage steps.

proposed analog buffer. The simulation results show that proposed analog buffer can drive the output load in the one-row line time of 50μsec.
The characteristics of the proposed analog buffer are summarized in table 1 and compared to conventional ones.

Table 1. Comparison of conventional Op-amp and proposed analog buffer.

Characteristic	Conventional 2-stage Op-amp	Proposed analog buffer
Supply voltage	10V (for dot inversion)	
Resolution	QVGA	QVGA
Quiescent current	1.5~2μA	<0.8μA
Error voltage	<5mV	<5mV
DC power consumption	10~14mW	<5.8mW (reduced 40~50%)

3. New data driver structure

Figure 5 shows the conventional 6bit data driver structure having 360-output channel. Generally, 2-driver ICs are required for QVGA [240×3(RGB)×320] resolution. The conventional structure contains one op-amp per each output channel, therefore it requires 360 op-amps. However, the proposed structure can reduce the number of op-amps by eliminating analog buffers block of each channel output, only contains 64 op-amps in R-sting DAC for Vcom modulation method and 124 op-amps for dot inversion method. The proposed structure for Vcom modulation method is shown in figure 6.

In case of conventional data driver structure, one op-amp drives one data line load(C_{DATA}=20pF), but in case of proposed structure, one op-amp can drive not only one data line but also 360-data lines during one-row line time. Accordingly, the op-amps of the proposed structure must have an excellent current driving ability that can charge the data line load capacitance from 20pF to 7.2nF; it is assumed that capacitance of one data line is 20pF, in the worst case, one op-amp have to drive approximately 7.2nF in one row line time of 50μsec. So the transistor size of op-amp's output stage must be larger than that of typical op-amp used in small size TFT-LCDs. The schematic diagram and its simulation results for worst case are shown in figure 7 and figure 8 respectively. The characteristics of proposed structure is summarized in table 1.

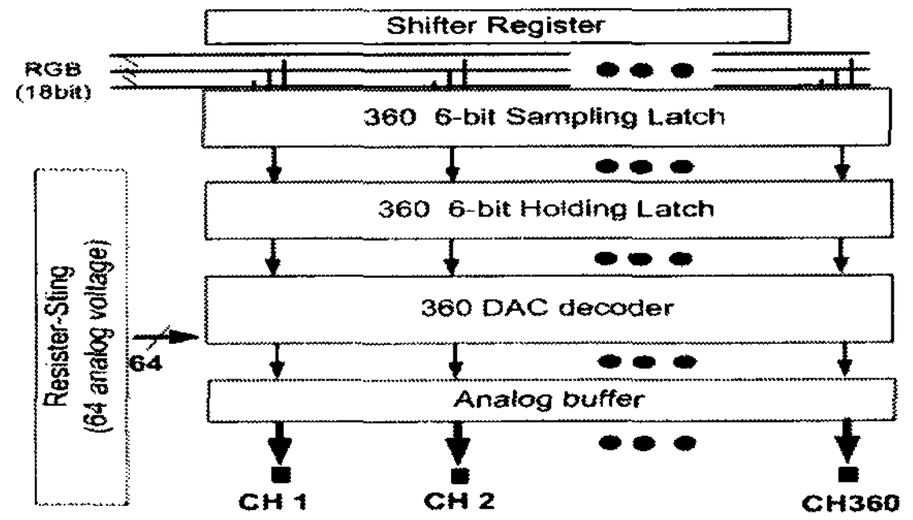

Figure 5. Conventional data driver architecture of 360 output channel.

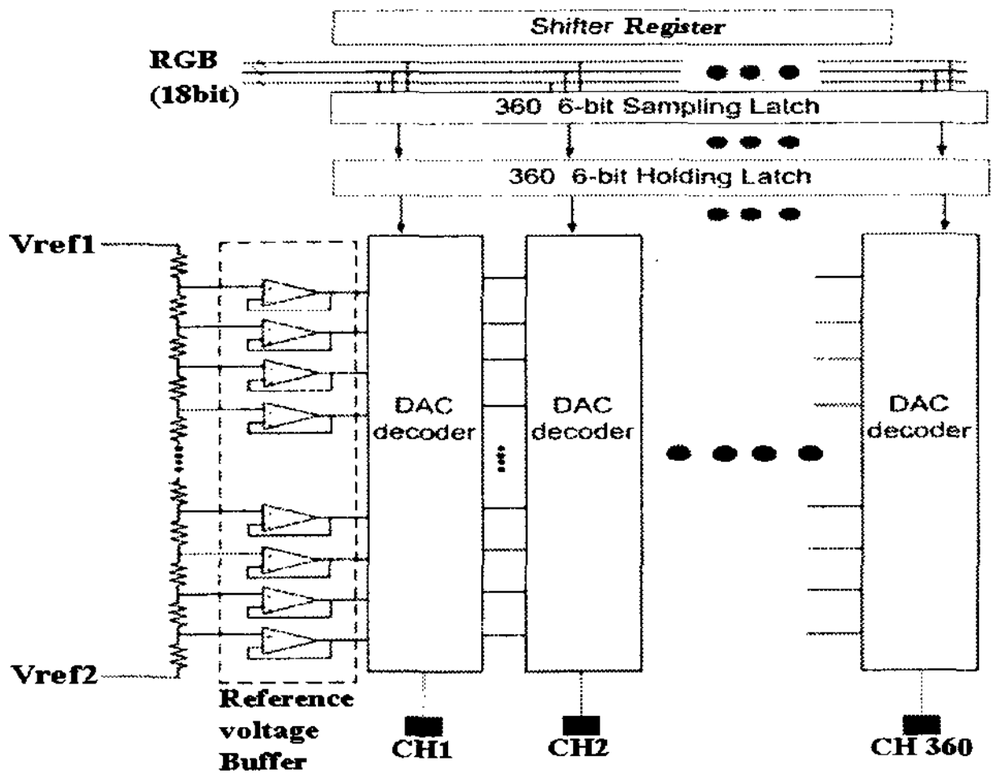

Figure 6. Proposed data driver architecture without analog buffer block.

3.1 Power Consumption

The DC power consumption by the quiescent current of op-amp is reduced when compared with conventional one. In case supply voltage is 5V for Vcom modulation method, the DC power of typical structure is 5V×360×2(2-driver ICs)× I_Q, where I_Q is the quiescent current(1.6uA~2.0uA), and one of the proposed structure is 5V×64×2× I_Q' , where I_Q' is 7.6μA. As shown in table 2, DC power is reduced about 25%. But in case supply voltage is 10V for dot inversion, DC power increases as compared with conventional one. Therefore, this structure is more proper for TFT-LCDs that applied the Vcom modulation driving method than the dot inversion method.

3.2 Estimation of area

Figure 9 shows the area comparison of the data driver having 360 output channel.

Because this structure contains only 64 op-amps, chip areas can be decreased. One channel size of typical 6 bit data driver structure is approximately 1000 ㎛×40 ㎛ and the total area of driver with 360 output is 1000 ㎛×14400 ㎛. But The total area of the proposed structure is approximately 800 ㎛×14800 ㎛, and this indicates that about 18% of area can be saved as compared with that of conventional data driver.

3.3 Uniformity

Generally, channel to channel voltage variation exists because of offset of analog buffer. When the same gray level such as all white or black pattern image is displayed, the displayed image have poor uniformity at typical ones. However, this structure, that one op-amp drives the same-gray level channel, can eliminate channel to channel voltage variation. Therefore this structure accomplish highly uniform image.

Table 2. Summary of the characteristics of conventional method and proposed method.

	Conventional method		Proposed Method	
Supply Voltage	5V	10V	5V	10V
Power(mW)	6~7	10~14	4.7~5	19~20
Area (only Op-amp areas)	14.4mm^2 (2.3mm^2)		11.84mm^2 (0.32mm^2)	
Image Uniformity	Moderate		Excellent	

4. Conclusion

We investigated the data driver structure that could reduce DC power consumption, furthermore accomplish the low cost and highly uniform image quality. Moreover, we designed a new analog buffer reducing static current. As simulation results of Hspice, the quiescent current is less than 0.8μA and the dc power consumption is reduced about 40~50% compared with conventional ones.

5. References

[1] Oh-Kyong Kwon .," An Ultra-Low-Power Driving Method for AM-LCD," in IDW'01, pp. 1595-1598.

[2] K. Meinstein *et al.*,"A Low Power High-Voltage Column/Dot Inversion Drive System," in SID Digest 1995, pp. 391-394.

[3] J. Jeon *et al.*,"A New Digital Driving Scheme for Poly-Si TFT-LCD Panels," in AISA DISPLAY 1998, pp. 425-428.

[4] S. W. Lee *et al.*," A Novel Integrated Serial Digital Data Driver for Poly-Si TFT-LCDs,", in IDRC 99, pp. 465-468.

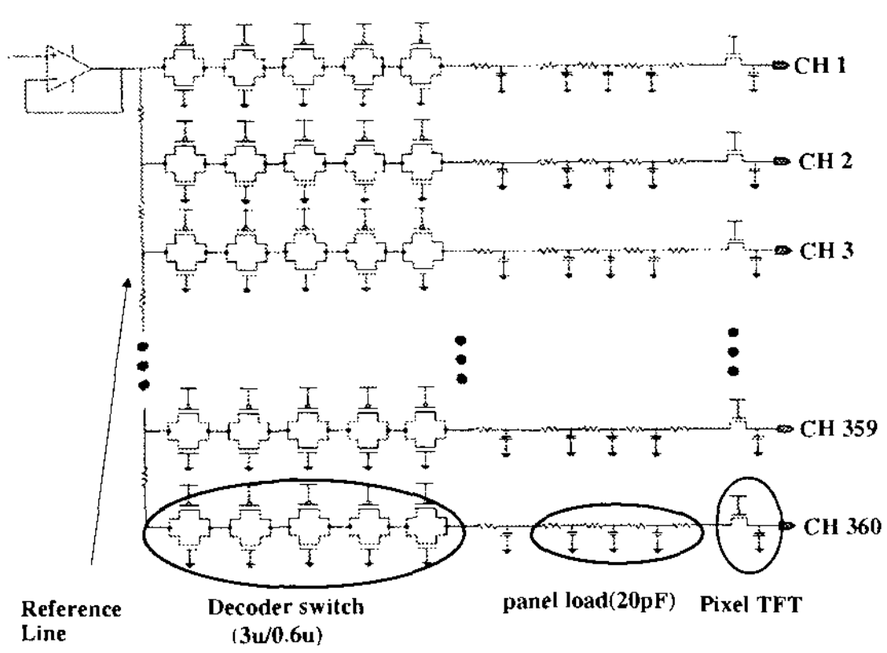

Figure 7. Schematic diagram for worst case simulation.

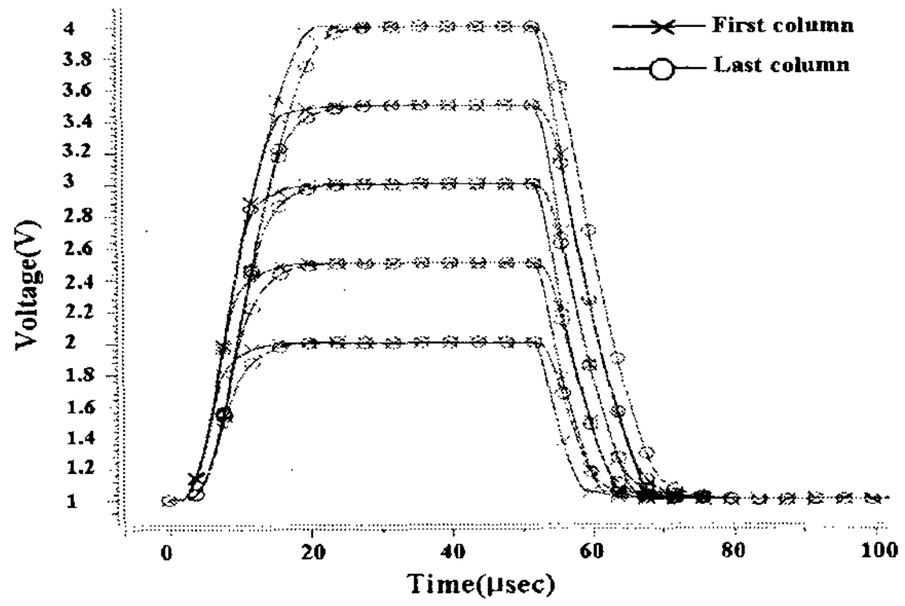

Figure 8. Simulation result of the circuit shown in figure 7.

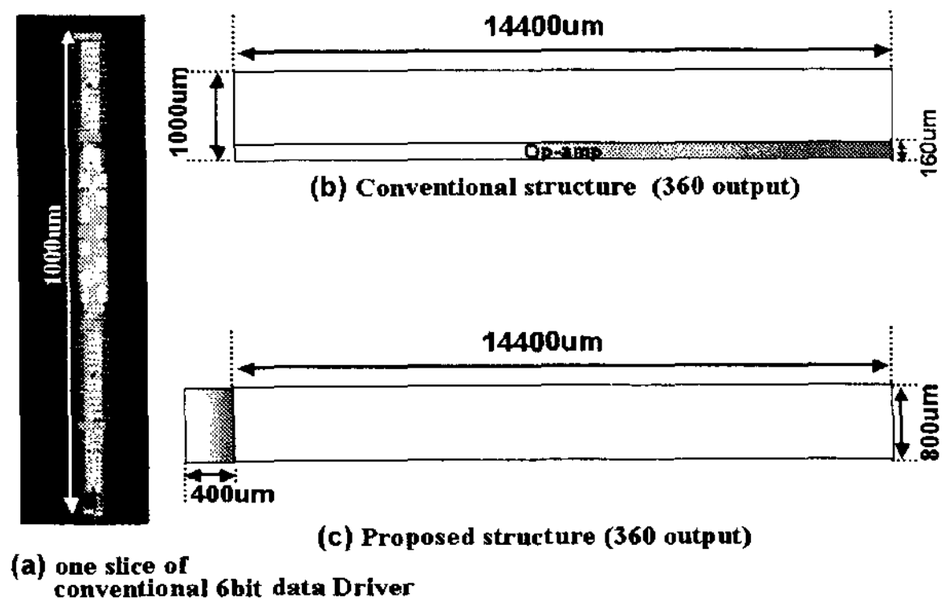

Figure 9. Estimation of the driver-IC area with the output pitch of 40 ㎛.