

High voltage MOSFET fabricated by using a standard CMOS logic process to drive the top emission OLEDs in silicon-based OLEDs

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Abstract

Using the conventional standard CMOS logic process, the high voltage MOSFET to drive top emission OLEDs was fabricated for the silicon-based organic electroluminescent display. The drift region of the conventional high voltage MOSFET was implemented by the n-well of the logic process. The measurement result shows a good saturation characteristic up to 50 V without breakdown phenomena.

1. Introduction

The silicon-based organic electroluminescent display (OLED) is comprised of the top emission organic light emitting devices (OLEDs) on the CMOS logic circuit. Although the OLED has a merit of comparatively low operating voltage, it is not easy to drive OLEDs directly with the conventional CMOS logic because the operation voltage of OLEDs is usually higher than the supply voltage of the CMOS logic, for example 5V.

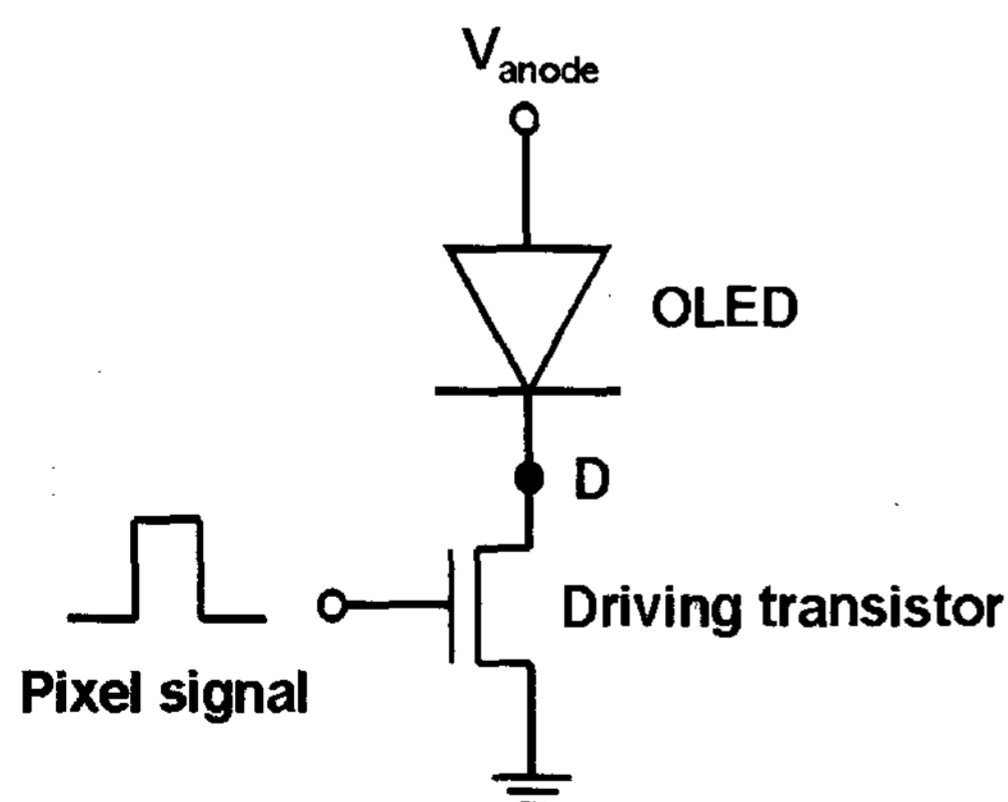


Figure 1 The pixel structure of the OLED.

Therefore, as a driving transistor of the pixel circuit shown in Fig.1, a high voltage MOSFET is necessary to drive an OLED safely [1].

In this work, a high voltage MOSFET that can be implemented using the 5V conventional 1.5 μ m CMOS logic process is proposed and confirmed, to drive top emission OLEDs for the silicon-based OLED.

2. The top emission organic EL device

A simple top emission organic EL device shown in Fig. 2 was fabricated in order to examine the operating voltage range. Aluminum cathode was used to be compatible with the standard CMOS process when OLEDs are integrated on the driving circuit. Also, the thin nickel anode to transmit the light was evaporated because the conventional ITO sputtering may cause damage to the emitting layer.

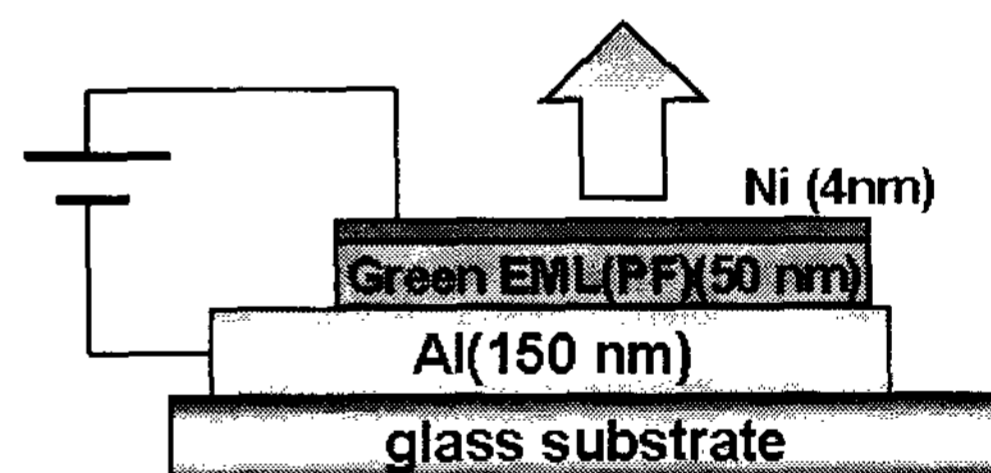


Figure 2 The structure of the fabricated top emission OLED.

Fig. 3 shows the measured I-V characteristic. This device operates on the 25~40V range, and it is comparatively high. It is mainly due to the high work function cathode and a single emitting layer. The high voltage operation characteristic of the top emission OLEDs can be found in other studies [2].

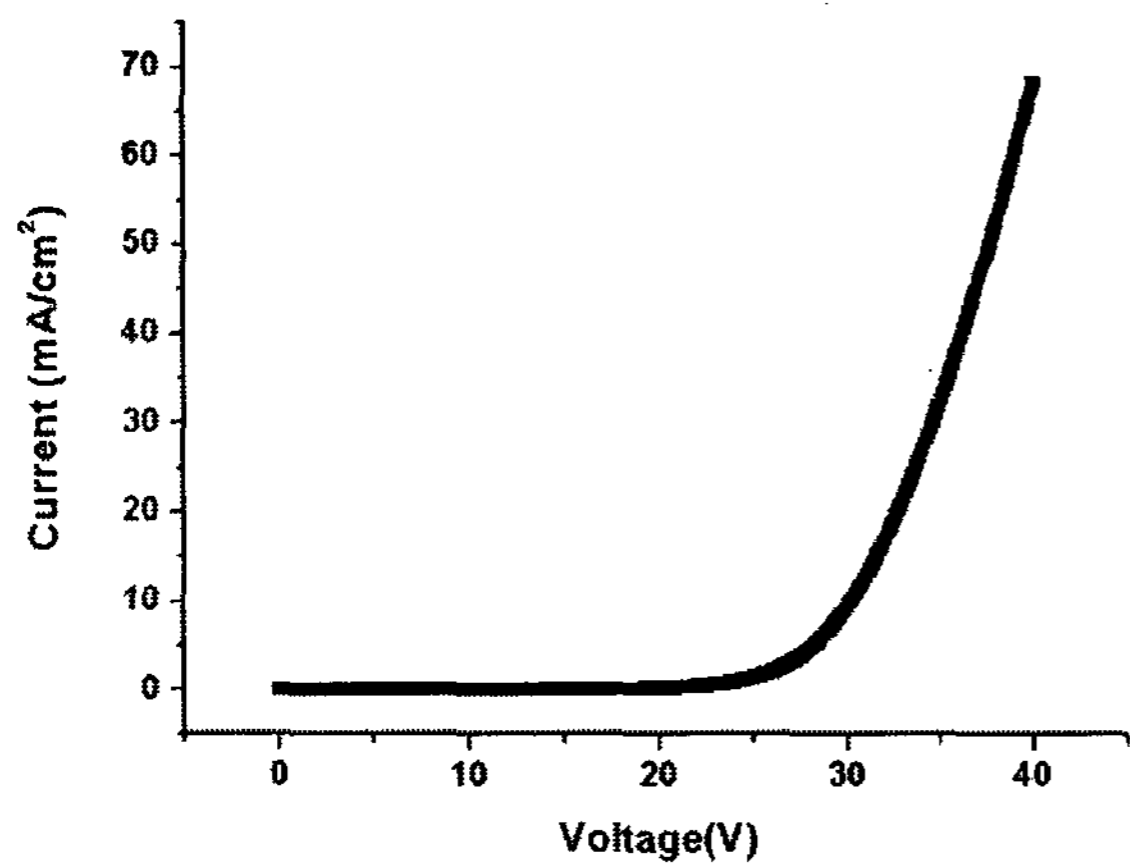


Figure 3 The measured I-V characteristic of the fabricated top emission OLED.

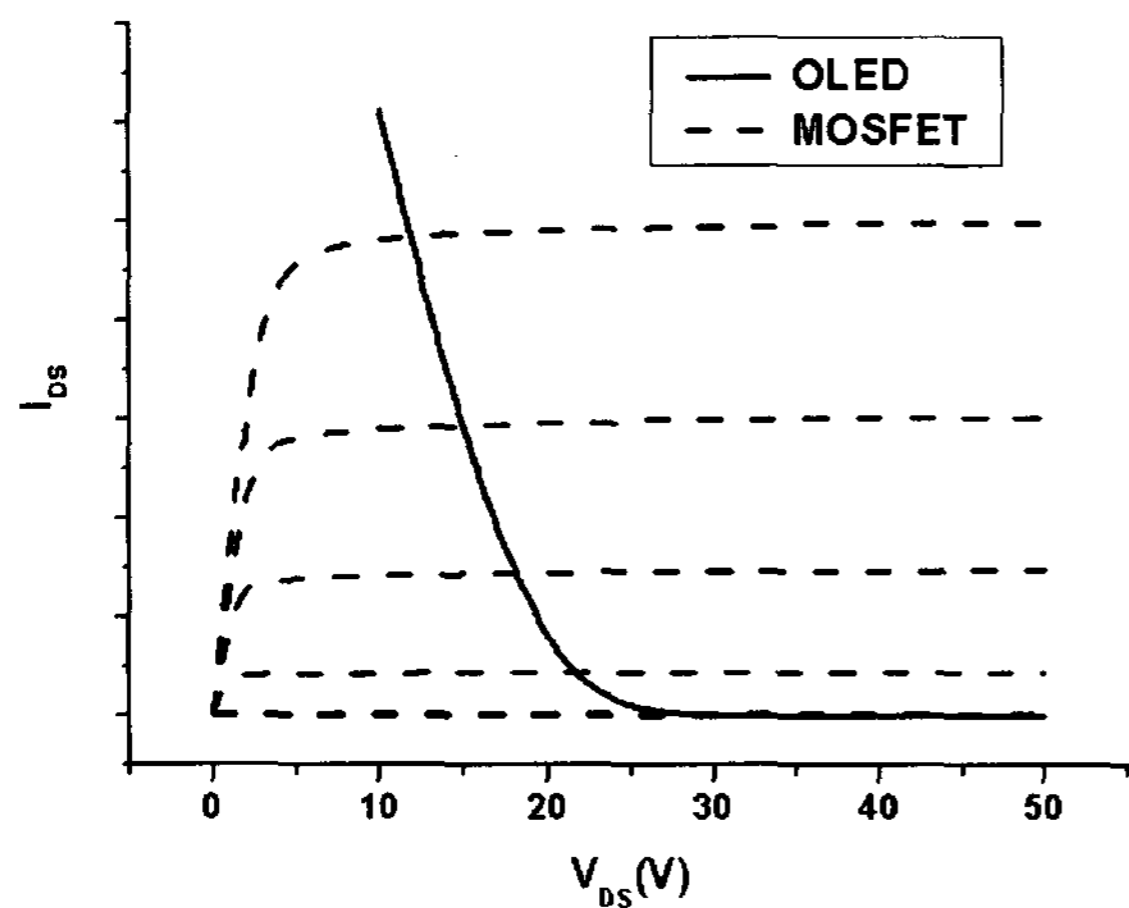


Figure 4 The example of the load line for the pixel circuit.

Fig. 4 shows an example of the load line for the pixel circuit shown in Fig. 1. From the figure, it is obvious that, to operate in the saturation region, the supply voltage V_{DD} of the driving transistor should satisfy the criteria:

$$V_{DD} \geq V_{EL_max} + V_{d,sat} = V_{EL_max} + \sqrt{2 \frac{I_{d,sat}}{\mu_{FET} C_{OX} \frac{W}{L}}}$$

where V_{EL_max} is the maximum operating voltage of the OLEDs [3]. The criteria specify that the driving transistor should operate up to about 50 V considering the electrical characteristic of the fabricated top emission OLED. Although a little lower voltage operation is expected when some other techniques, e.g. employment of multi layer or a low work function

cathode, and so on, are applied, it is not easy to operate below 5 V, which is the supply voltage of the conventional 1.5 μm CMOS logic driving circuit. Hence, a high voltage MOSFET is necessary.

3. The high voltage MOSFET implemented with the conventional standard process

The conventional high voltage MOSFET has the drift region to disperse the strong electric field. Compared with the standard logic process, the high voltage process requires additional mask steps to form the drift region, which causes higher process cost.

However, the high voltage MOSFET can be implemented by the simple layout technique even in the conventional logic process [4-6]. Fig. 5 shows the layout and the cross section of the high voltage MOSFET according to the standard 1.5 μm process design rule. If we replace the drift region of the high voltage process by n-well of the standard logic process, the low-doped n-well region disperses the strong electric field of the drain, in place of the drift region. This technique has the advantage that a high voltage MOSFET can be fabricated without any process modification.

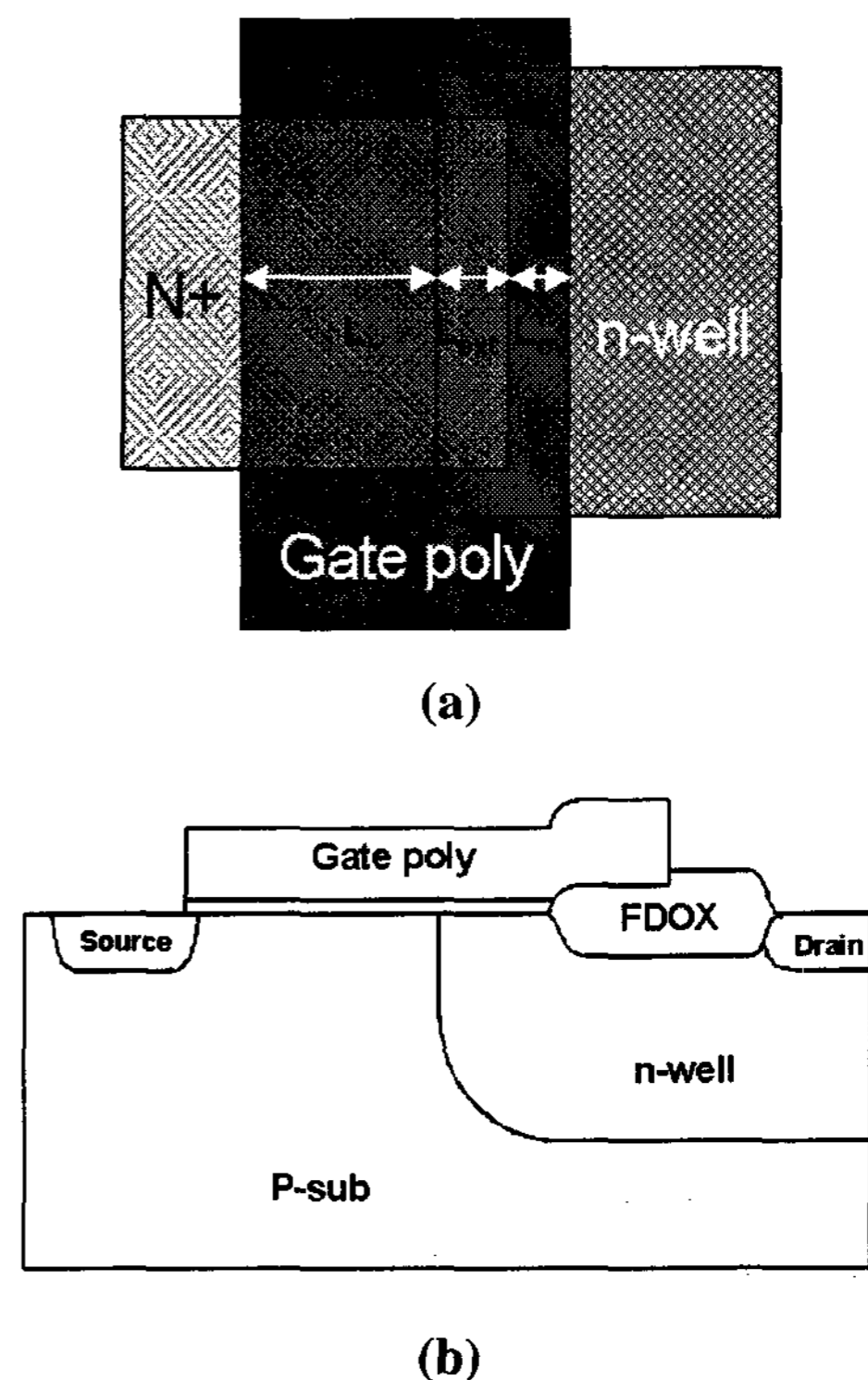


Figure 5 (a) The layout and (b) cross section of the fabricated high voltage MOSFET whose drift region is replaced by the n-well.

The high voltage MOSFET was fabricated using the standard 1.5 μm logic process. Fig. 6 shows key process flow.

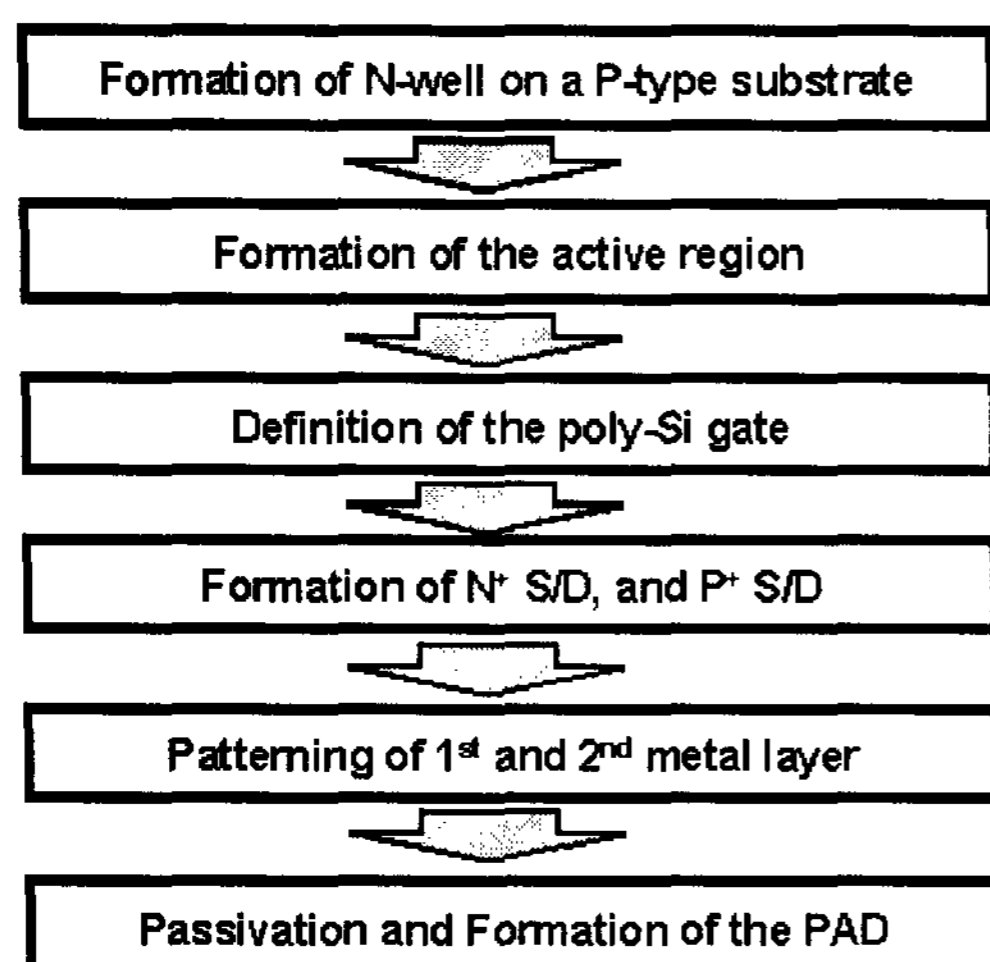


Figure 6 The key process flow of the standard CMOS logic process.

Fig. 7 shows the transfer characteristic of the fabricated high voltage MOSFET. It shows the good characteristic which is similar to that of the low voltage logic NMOS. Fig. 8 shows the output characteristic of the high voltage MOSFET. It shows excellent saturation characteristics up to 50 V without breakdown phenomena, which is high enough to drive top emission OLEDs.

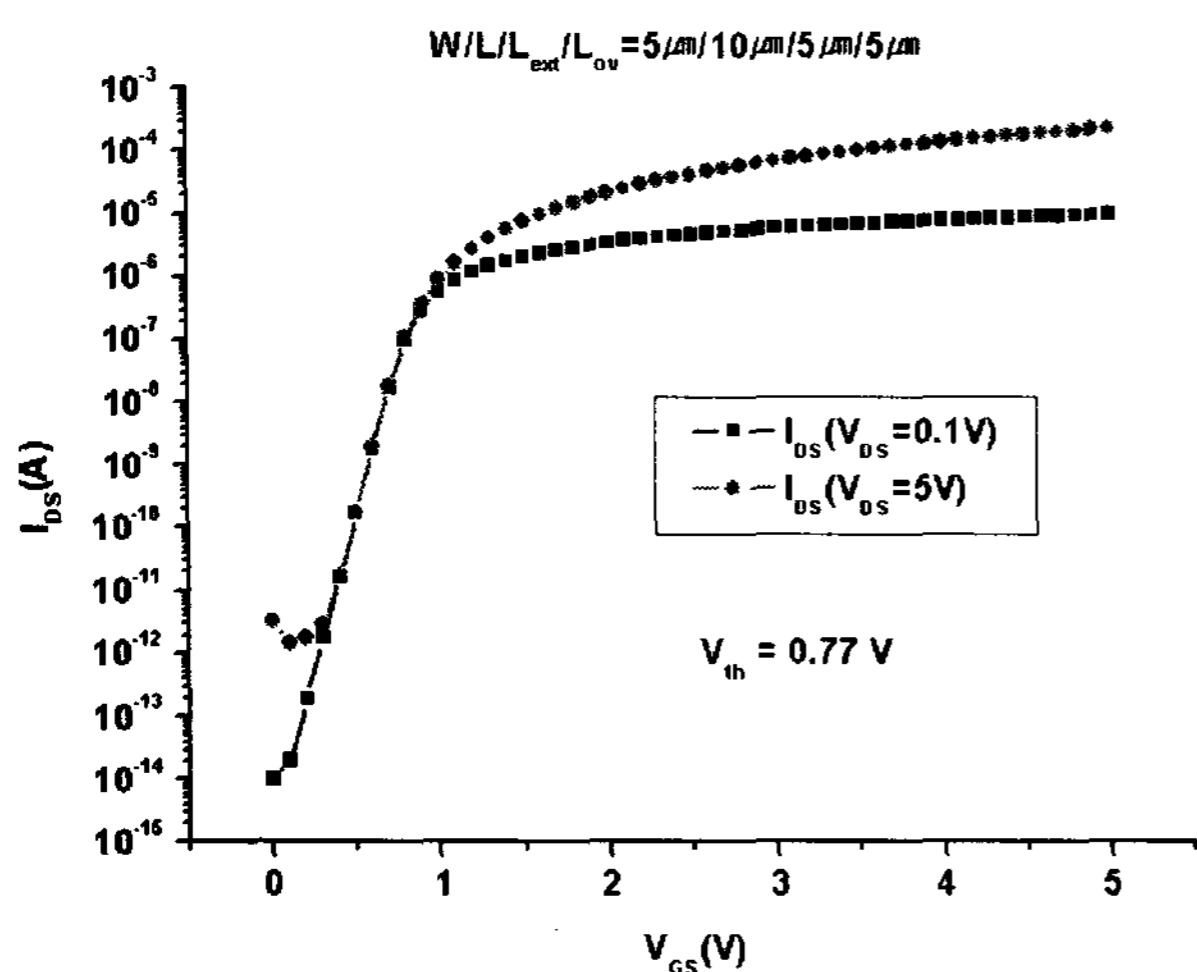


Figure 7 The transfer characteristic of the fabricated high voltage MOSFET.

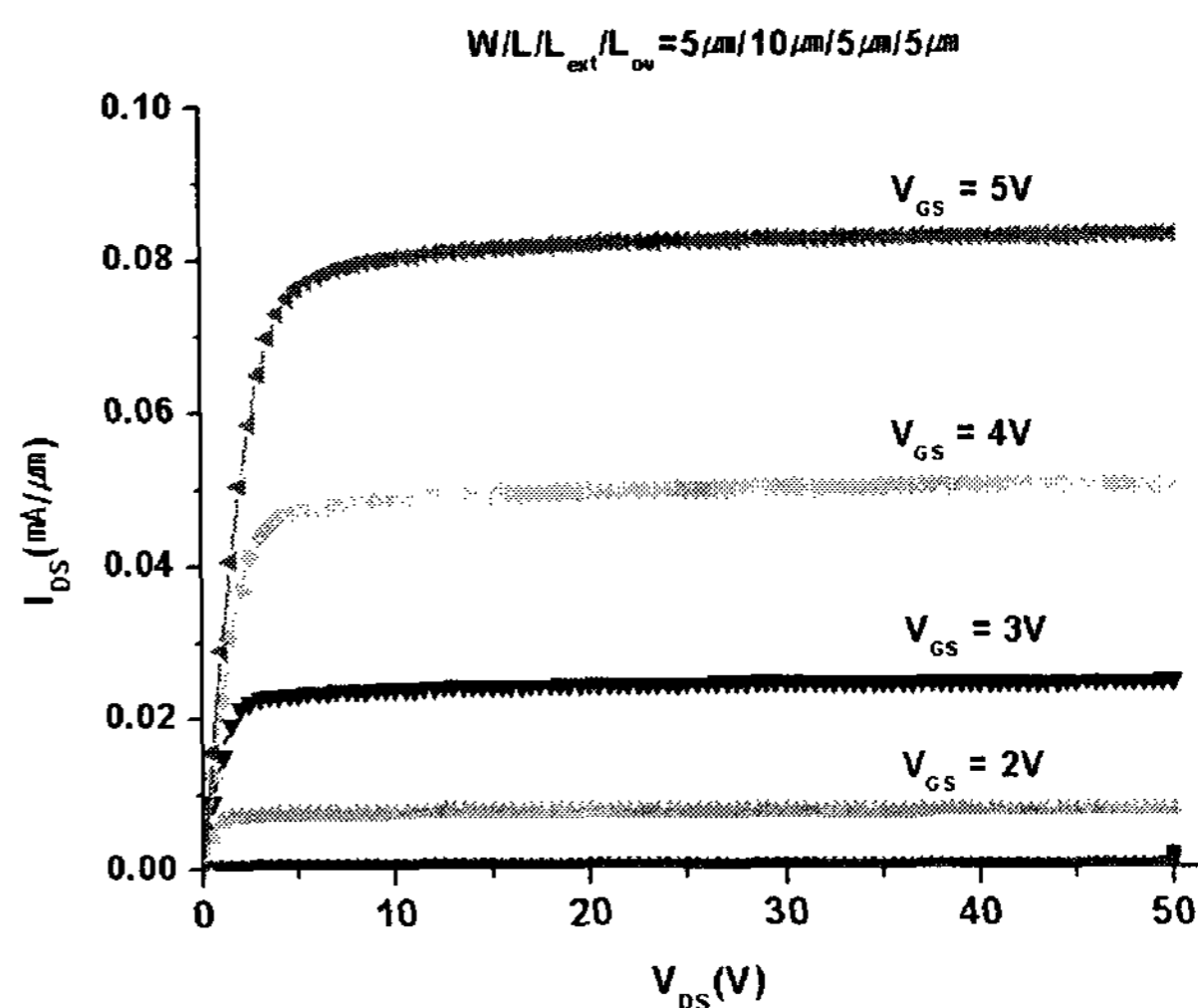


Figure 8 The output characteristic of the fabricated high voltage MOSFET.

4. Conclusion

By a simple layout change, a high voltage MOSFET which is able to drive top emission OLEDs was fabricated using the standard CMOS logic process for the silicon based OLED. The electrical measurement shows that it is able to drive top emission OLEDs up to about 50 V.

5. References

- [1] S.C. Tan, and X.W. Sun, SID02 DIGEST, 980(2002).
- [2] Samil Kho, Daeyong Cho, and Donggeun Jung, IMID'02, 714(2002).
- [3] TaeHyung Zyung, Display engineering 1, Section 3-2, 824(2000).
- [4] Jong Duk Lee, Jung Hyun Nam, Hyuck In Kwon, and Byung-Gook Park, JKPS 40, 592(2002).
- [5] Jozef C. Mitros, Chin-yu Tsai, Hisashi Shichijo, Keith Kunz, Alec Morton, Doug Goodpaster, Dan Mosher, Taylor R. Efland, IEEE TED, 48, 1751(2001).
- [6] Hyuck In Kwon, Jung Hyun Nam, Byung Gook Park, Jong Duk Lee, 8th KCS, 533(2001).