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A Study on the Relationships between Addressing Time and Cell Structure in AC PDP

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Abstract

One of the most important problems in ADS method is that the method has too long addressing period, The addressing time can be defined as the sum of the discharge time lag and the duration of discharge current. If the addressing time increases, the sustaining period for display image should be decreased. As a result, the luminance of the PDP decreases. Therefore, the discharge time lag and duration of discharge current should be decreased in order to reduce the addressing time.

In this paper, in order to improve addressing time, relationships between addressing time and cell structure in AC PDP was studied

1. Introduction

One of the most important problems in address-display separated (ADS) scheme [1,2] in ac plasma display panels(PDP) is that they have too long addressing period. One line scanning time is about 3㎲, so that the time for 480 lines in VGA resolution is about 1.4㎳. A frame consists of 8 sub-field for 256 gray level. Therefore, the total addressing time is 11.52㎳, which is about 70% of one frame. As the addressing time increases, the sustaining period for display image should be decreased. As a result, the luminance of the PDP decreases.

The dual scan method has adopted to solve this problem in a large ac PDP. In this case the scanning period can be half reduced compared with single scan. However, the driving circuit cost increase is inevitable. In case of the high definition TV(HDTV) whose scan line is more than VGA resolution, the addressing speed has been big issue[3]. The addressing time depends strongly on the cell geometry and on the thickness of the dielectric layers on the display and address electrodes[4].

In this study, we investigated the relationships between the discharge cell structure and addressing time in ac PDP.

2. Basic concept of ac PDP

Figure 1 shows the principal structure of a discharge cell in ac PDP. On the front panel, a paired paralleled display electrode Z and scan electrode Y are fabricated. Each electrode is composed of narrow and transparent bus electrodes to emit the luminance effectively. A dielectric layer covers these electrodes, and the MgO protecting layer is performed on the dielectric layer by E-Beam evaporation method[5-7].

On the rear panel, striped address electrodes are arranged. Striped barrier ribs are on both sides of the address electrodes to divide the adjacent discharge cells and to eliminate the optical cross-talk between them. Three primary colors of

phosphor material for red, blue, green colors are deposited in the neighboring channels made by the ribs and the dielectric layer[8].

The structure has realized good performances such as a high luminance, a high luminous efficiency and a wide viewing angle. The panels are assembled each other with about 130㎛ gap. A Ne-He-Xe gas mixture is introduced between gaps. The panel structure is the simplest one of conventionally developed color PDPs and the fabrication process is simple enough to mass-produce, easy to manufacture large area panels and high-resolution panels[9-11].

As a driving method of ac PDP, address display separation(ADS), scheme has been widely used. In ADS method, a picture of one frame is divided into eight sub-fields. Each sub-field has reset, address and sustain period as shown in Figure 2. The process of the reset period is to erase the wall charge accumulated on the dielectric surface in the previous sub-field, which make the same surface condition before next addressing. The process of address period is to make new wall charge on the dielectrics of each discharge cell by applying the addressing pulses between scan and scan and address electrodes. The process of sustain period is to make an image on the panel by applying the ac sustaining pulses to all display electrodes[12, 13]. In this case, only the selected discharge cells, which have been addressed in the address period, are turned on. The number of sustaining pulses is decided corresponding to the weight of luminance for each sub-field[14].

3. Experimental

Table 1 shows the specifications of 4-inch test model ac PDP used in our experiment.

Figure 2 shows the driving waveforms of ADS method used in this experiment. ADS waveform of ramp method is used. The total period is 1.63ms, In the reset period, the ramp rising time is 100㎲ and the ramp falling time is 150㎲. The address period is designed as about 1ms in order to make the same condition as the conventional 40-inch PDP. The pulse width of one address is about 3㎲.

Figure 3 shows the schematic diagram of experimental setup. The total driving circuit, which is applied each electrode, consists of analog part and digital part. In the digital part used the personal computer, the variation of pulse is easily done by using the signal generator (Time 98) which is able to control with real time. The Digital driving circuit part consists of signal generation, power supply and analog switching part.

Table 1. Specification of 4-inch ac PDP

Front panel		Rear panel	
Dielectric thickness	20㎛	Address electrode width	100㎛
ITO width	310㎛	White back thickness	15㎛
ITO gap	60㎛	Rib height	120㎛
Bus width	100㎛	Rib pitch	250㎛
MgO thickness	5000Å	Rib width	50㎛
He+Ne(30%)+Xe(4%) 300Torr		Phosphor thickness	20㎛

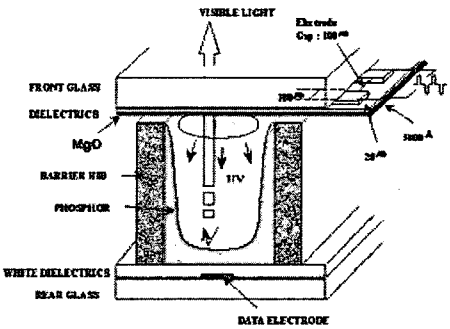

Figure 1. Principal structure of a discharge cell in ac PDP

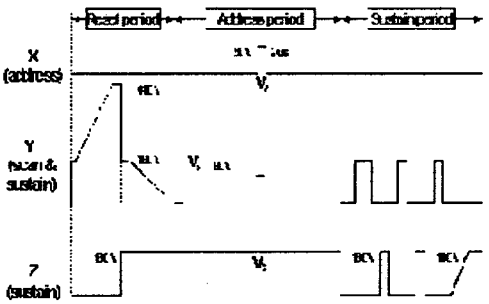

Figure 2. Driving waveform of ADS method

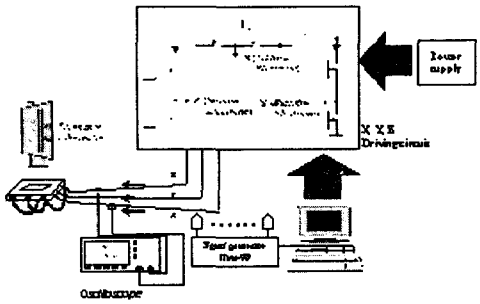

Figure 3. Schematic diagram of experimental setup

Figure 4 shows the voltage pulse waveform and the current waveform. Because PDP cells are capacitive load, charge current or displacement current first flows in applying to voltage. If the voltage of cell inside is formed by the current component, then the discharge current by the discharge flows.

However, after the pulse voltage rises up, the discharge current is represented by the current waveform, with time delay to some extent. This time delay is called discharge time lag[15].

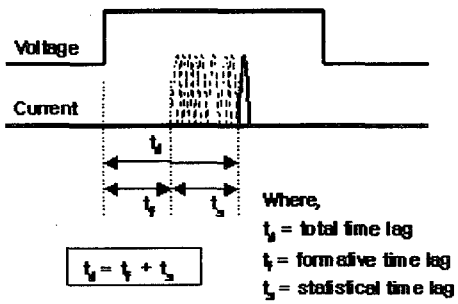

Figure 4. Discharge time lag

The discharge current can be measured with the oscilloscope, using the current probe.

Td is calculated by the time, which is from 10% point of peak of the applied voltage waveform to 10% point of rising peak of the discharge current in the oscilloscope. Currently, the address pulse width is allotted about 3μs by this discharge time lag, when 1 line scans in ADS driving of 40-inch VGA class. Accordingly, scanning 480 lines in total takes about 1.44ms, and scanning 8 sub-fields takes about 11.52ms. This takes approximately 69% of 1 sub-frame in 16.67ms. It is hard to obtain sufficient luminance because the sustain period to be able to display is shortened much.

The addressing time probably needs to be a minimum because these can bring about more serious problems in high-resolution spec.

4. Results and Discussion

Figure 5 shows the typical addressing discharge current waveforms when the gap of ITO electrode on the front panel decreases. When the gap of ITO decreases from 60μm to 40μm, the discharge lag and the addressing time decrease from 1.3μm to 1.1μm as 4% proportion per 10μm.

Figure 6 shows the thickness of transparent dielectric layer on the front panel. When the thickness of transparent dielectric layer decreases from 40μm to 20μm, the discharge lag and the addressing time decrease from 1.5μm to 1.2μm as 4% proportion per 5μm.

Figure 7 shows typical addressing discharge current waveforms when the height of barrier rib on the rear panel decreases.

Such as above results, when the height of barrier rib decreases from 150μm to 100μm, the discharge lag and the addressing time decrease from 1.3μm to 1.2μm as 4% proportion per 10μm.

Figure 8 shows the thickness of white dielectric layer on the rear glass decrease. Such as above results, when the thickness of white dielectric layer decreases from 25μm to 15μm, the discharge lag and addressing time decreases from 1.66μm to 1.3μm as 4% proportion per 2μm.

However, In the case of no white dielectric, the discharge time lag and the addressing time increase up to 2.2μm reversely.

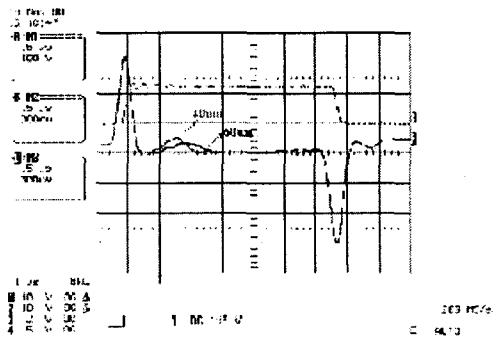

Figure 5. The current addressing discharge waveforms as a parameter of ITO gap

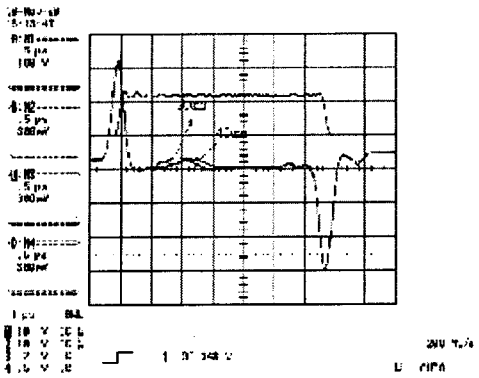

Figure 6. The current waveforms as a parameter of transparent dielectric thickness

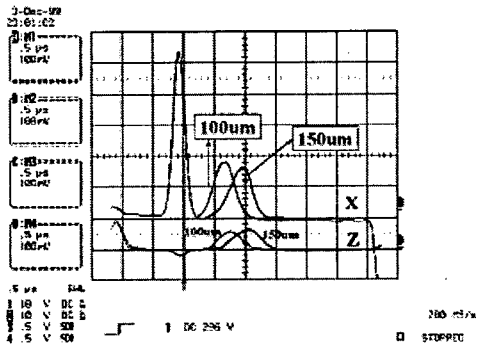

Figure 7. The current waveforms as a parameter of barrier rib height

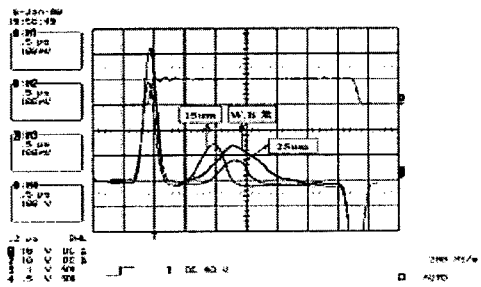

Figure 8. The current waveforms as a parameter of white dielectric thickness

5. Conclusion

In this paper, the relationships between discharge cell structure and addressing characteristics are investigated.

It is found out that the addressing time was decreased with decreasing gap of ITO electrode and thickness of transparence dielectric layer on the front glass. The decrease rates were 4% per 10 ㎛ and 4% per 5㎛, respectively. Also in cases of decreasing height of barrier rip and thickness of white dielectric layer on the rear glass, addressing times were at the rate of 4% per 10㎛ and 4% per 2㎛, respectively.

The most improvement conditions of the Addressing time are as following. That's, dielectric layer width in front panel, ITO gap, white back width and Rib height decrease 10, 10, 2, 10㎛, respectively. Consequently each improvement rate of addressing time is obtained 4%.

6. References

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