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종이위에 구현한 유기박막트랜지스터의 특성

성재용, *김영훈, *문대규, *한정인, 곽성관, 정관수

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Polymer Thin Film Transistors Fabricated on Photo Paper

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Abstract

In this paper, we demonstrate polymer thin-film transistors (TFTs) on a paper-based flexible substrate. As a substrate, commercially available photo-paper is used with parylene coating. The parylene layer enables conventionally used wet chemical process and vacuum deposition processes for electrodes and gate insulator. As an active channel layer, we used poly-3-hexylthiophene (P3HT) which is solution process. Field effect mobility up to (0.06 ± 0.02) cm^2/V s and on/off ratio of $10^3 \sim 10^4$ are achieved on a photo-paper.

I. Introduction

During the last decade, there has been an increasing interest in electronic devices based on conjugating polymer materials, such as light-emitting diode [1], field-effect transistors [2], solar cells [3] and photo-detectors [4]. Also, recently, electronic devices on flexible substrates are gaining much attention due to their advantages in light-weight, robustness and mechanical flexibility. However, commonly used flexible substrates are still very expensive, since various coatings (hard coating, non-glare coating, barrier coating) are required for high-performance applications.

The focus of this paper is to development of OTFT arrays on a cheap photo paper. However, compared to other flexible substrates, such as polymers and metal sheets, paper sheet suffers from wet process and heat treatment. The paper easily soaks up the water and tears apart into pieces within a minute. In order to protect the paper sheet from the water, a barrier layer must be coated on the entire substrate. As a barrier layer, Parylene was coated on each side of the paper by vacuum deposition process. Parylene coating method is used in wide applications such as barrier coating for oxygen, moisture, chemicals and solvents. In addition, Parylene is hydrophobic material with thermal mechanical stability up to 150 •. We report on the characteristics of OTFT array fabricated a Parylene coated paper substrate for the first time.

II. Experimental

2.1 Parylene coating on a paper

The paper sheet used in this experiment is commercially available photo paper. Due to the water absorption, the paper sheet easily soaks up water during the wet chemical process. Thus, a protection layer or a barrier layer should be coated on the entire sheet in order to carry out the process. Commonly used thin film deposition methods, such as sputtering, evaporation and spin coating provide films with reasonable quality. However, several deposition steps are required to

deposit films on both sides of the substrate and the process is rather complicated. Fig. 1 shows the Parylene deposition process on a photo paper. Parylene coating process, compared to other deposition process, is very effective and simple process for coating the entire substrate in a single step. Parylene source material, which is in a dimer form, is first converted to dimeric gas under vacuum and heat. Then the gas passes through the pyrolisis where the dimer is cleaved and finally deposited around the substrate as a clear polymer film. The coating process is done at ambient temperature and the thickness can be controlled up to 70 •. In our case, the thickness of the layer was varied from 5 •. Parylene is also a hydrophobic and also provides conformal, pinhole-free coating suitable as a barrier layer.

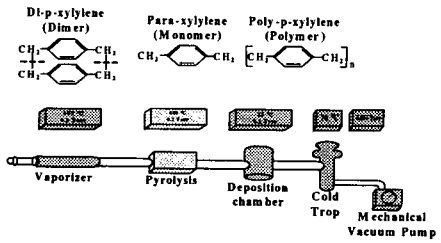

Fig. 1 Parylene deposition process

2.2 Fabrication of Polymer TFT on a paper substrate

The deposition of gate electrode was carried out by RF-magnetron sputtering process. Nickel (Ni) is preferred for its high CTE value (25 x 10^{-6} / K) and ductile properties. Ni thin film was first deposited at room temperature with thickness of 150 nm. For gate dielectric, polyimide (PI) / SiO_2 dual-layer structure was used to improve the electrical properties of TFT devices. The details of PI / SiO_2 dual-layer structure properties and the electrical properties of TFT devices using such structure are described in elsewhere [5]. As source and drain electrodes, thermally evaporated gold (Au) with thickness of 50 nm. The OTFT structure was bottom contact type and the gate width and length were 500 • and 25 •, respectively. Fig. 2 shows the polymer TFT devices fabricated on a flexible photo paper.

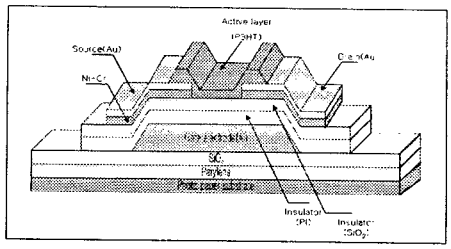

Fig. 2 Structure of Polymer TFT on a paper

Poly-3-hexylthiophene (P3HT) was purchased from Aldrich with more than 98% in head-to-tail (HT) regio-regularity. P3HT was dissolved in $CHCl_3$ solvent for 2 days with concentration varied from 0.2 wt% and printed by contact printing or spin coating method. First, an elastomer stamp was created by pouring liquid poly (dimethylsiloxane) (PDMS) into a master structure and curing at 60 • for 24 hours. The mixing ratio of base and the curing agent was 10 : 1 by weight. The elastomer stamp fabricated by following this procedure exhibited 1 nm in surface roughness and Young's modulus of 3 MPa. The stamp was then inked by P3HT solution. The P3HT solution was removed after several seconds under a stream of nitrogen, leaving a thin layer of P3HT on the stamp. Then the stamp was contacted with the substrate and the P3HT layer was transferred to the substrate. The thickness of the printed P3HT layer can be controlled by the concentration of solution and the duration time. The samples were then annealed in N_2 and vacuum atmosphere continuously.

Electrical characteristics of metal films and the OTFT devices made on a paper sheets were measured using HP4145B semiconductor parameter analyzer. The transfer and output characteristics were measured under vacuum and dark conditions to avoid any effects by moisture, oxygen and illumination.

III. Results & Discussion

The photo-papers used in this work have very rough surface properties. Fig. 3(a) shows atomic force microscopy (AFM) image of bare surface of photo-paper. The RMS roughness was over 27 nm which is extremely high compare to polymer substrate such as polycarbonate (PC) and polyethersulfone (PES) (RMS roughness about 1~2 nm). Rough surface should be controlled in order to achieve high performance devices. Using parylene layer, the RMS roughness of the paper was reduced to 7 nm (Fig. 3(b)). For more reliable device, over-coating layers may be applied to reduce the surface roughness. Fig.4 shows the reflectance of photo-paper substrates with Al and Ni coating. The reflectivity is relatively low which results from their low flatness.

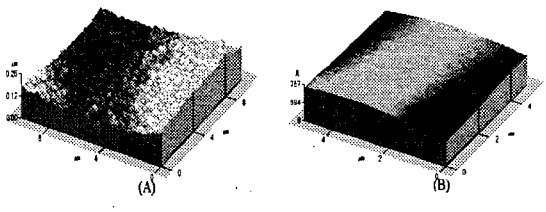

Fig. 3 AFM images photo-paper surfaces; (a) bare, (b) parylene coated

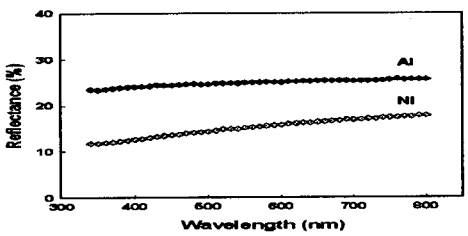

Fig. 4 Optical reflectance of metal coated photo-paper substrates.

In this experiment, P3HT was used after further purification process to increase the HT regio-regularity. Transistor properties, such as field effect mobility and on/off ratio are greatly affected by the micro structure of the thin layer. According to Sirringhaus et al., P3HT layer with edge-on orientation showed enhanced field effect mobility up to 1×10^{-1} $cm^2/V \cdot s$. In contrast, P3HT layer with face-on orientation the mobility was nearly 2 orders lower. This phenomenon is believed to be due to the difference in π - π * stacking orientation. When the side chain is attached to the oxide surface, the layer is edge-on oriented, which results in π - π * stacking orientation parallel to substrate surface, also the direction which the current flows in the device. However, when the side of thienyl ring is attached to the oxide surface, the layer is face-on oriented, which results in π - π * stacking orientation normal to substrate surface and direction the current flows. Also, since the side chains are electrically insulators, they will affect the charge transport in the polymer layer. The orientation of the layer is very much dependent on the HT regio-regularity, the formation method of the layer and surface energy of the substrate.

The electrical characteristics of polymer FETs on a photo-paper substrate with a channel length of 25 μm and width of 500 μm are shown in figure 5 (a) and (b). Well saturated behavior is observed in figure 5 (b) and field effect mobility was calculated in saturation region. Field effect mobility was up to (0.06 ± 0.02) $cm^2/V \cdot s$ and on/off ratio was about 10^3 ~ 10^4, which are relatively high values even compared to OTFT fabricated on polymer or glass substrates. However, the off-state current of the device is very high, resulting in relatively low on/off ratio of the device. However, with proper passivation layer, such as SiO_x, the off-state current can be lowered.

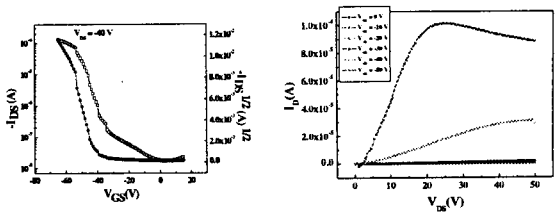

Fig. 5 Electrical characteristics of polymer FETs fabricated on a parylene coated photo-paper (L=25 μm, W=500 μm).

IV. Conclusion

We demonstrated polymer FET arrays fabricated on a parylene coated paper substrate with reasonable characteristics. For improved device characteristic and wet chemical process, parylene layer was coated on the substrate. With purified P3HT, field effect mobility up to 0.06 cm^2/V s and on/off ratio about $10^3 \sim 10^4$ were achieved. Parylene coating is a very effective way to control the rough surface of a photo paper and also enables the wet chemical process. Using these fabrication techniques, even lower cost displays could be demonstrated such as electronic papers and wearable displays.

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