100nm 이하 Device에서의 CMP 기술의 문제점 및 향후 도전과제

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Issues in CMP Technology and Future Challenges for Sub-100nm Devices

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Abstract

CMP process requirements become tighter especially in sub-100nm technology. Especially, high planarity and low defectivity appear as leading issues in CMP technology. Also, the introduction of new materials and advanced lithography technique increases CMP applications. Here are listed some major issues and challenges in CMP technology, which can be categorized following four items. These have practical significance and should be considered more concretely for future generation.

Key Words : Edge over erosion(EOE), Depth of Focus(DoF), Cu/Low-k, Noble metal, Defectivity

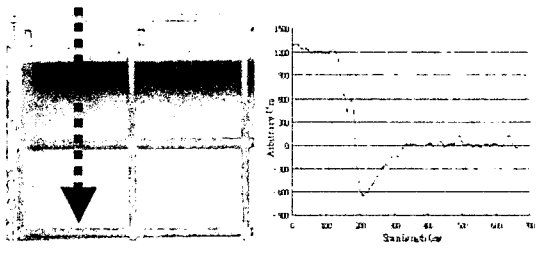
1. Edge over erosion in highly selective CMP

Usually, discolor-like-overpolishing phenomena were found after W plug CMP process as can be seen in Fig.1 (a). This is the effect of edge over erosion (EOE) which is attributed to the local stress concentration between patterned and non-patterned region. Fig.1 (b) shows the step-height profile of Fig.1(a) and the significant step-height difference near the edge of a cell array can be observed. This EOE behavior is distinct in highly selective CMP process such as W and poly-Si including 1st step Cu CMP.

Also, the EOE is distinguished in low pattern density compared with high pattern density region. In general, higher pattern density drives the significant erosion, however, the EOE shows the opposite result. Fig. 2 displays the erosion and EOE as a function of W pattern density. As expected from Fig. 2, the EOE is critical to planarity of low pattern density regime such as contact plug or via CMP. Therefore, the CMP of damascene pattern of Cu or W having high pattern density does not make such significant EOE compared with erosion.

This type of over-polishing results in poor planarity in a chip, and it gives detrimental influences on the subsequent patterning processes. The insufficient or improper plug patterning and the residual particulate defects are typical examples as shown in Fig. 3(a) and (b). To do so, to meet the planarity requirements for subsequent patterning process, it is inevitable to minimize the EOE or to eliminate the effect of poor planarity. To solve the last problem, it is simple and clear, if the additional planarization process is inserted prior to photolithography process. However, this approach is time-consuming and cost-ineffective.

In the previous research, Park *et al* [1] suggested some solutions such as hard pad, mild selectivity slurry, precise EPD control, and high pressure-low



(a) (b)

Fig. 1. Discoloration at the edge of a cell array (a)Top-down view image and (b) Step height profile from a periphery to a cell array in y-axis direction.

speed process parameters. Also, they proposed the best method to conduct the EOE including the erosion would be dummy pattern generation for minimizing pattern density difference or CMP-friendly layout design for high planarity.

2. Effect of new light source for photolitho-graphy

As design node technology enters into sub-100nm generation, the new light source of ArF is introduced in photolithography technology. Compared with KrF technology, ArF technology needs more advanced planarity due to low depth of focus (DoF) margin and poor photoresist (PR) characteristics. The step height induced from CMP planarity causes coating thickness variation of PR and anti-reflective coating (ARC) layer.

These undesirable effects lead to a partial patterning and a wide size variation. Table 1 exhibited after development inspection (ADI) critical dimension (CD) variation of deep hole patterning process for DRAM, where such variation is not so critical in KrF photolithography technology.

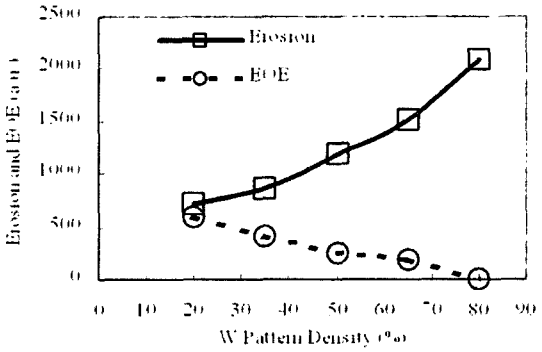


Fig. 2. Erosion and EOE amounts as a function of W pattern density during W CMP process.

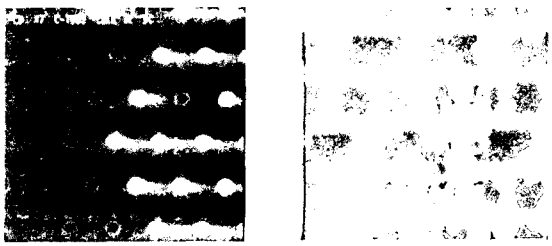


Fig. 3. Typical issues originated from EOE (a) Inadequate plug definition, (b) Residual particle .

Table 1. ADI-CD variation under various process condition in deep hole pattering process for DRAM.

Condition	Normal	Bare-Si	CMP	SOG
Variation(a.u.)	> 30	17	19	18

Due to the step height variation, the normal process results in above 30 in ADI-CD variation. However, the ideal case defined on bare-Si having no step height variation has only 17 in variation. It is noticeable that a planarized surface with CMP or SOG coating delivers a superior performance in minimizing CD variation. This explains that the local step height variation can cause the patterning failure and this is critical to these days having ArF photolithography technology.

For more advanced pattern definition, ArF with immersion technology and EUV lithography will be introduced in mass production line. Unfortunately, the new photolithography technologies require tighter and lower DoF specification. For this reason, the high planarity performance including good uniformity characteristics is inevitable for future technology.

3. Introduction of new material CMP

As patterning technology improves, a great deal of materials has been introduced to meet the device requirements. Among them, some materials are treated using CMP technology. As new materials, Cu/low-k dielectrics for advanced interconnection and noble metal for capacitance are typical examples.

For multi-level interconnection of sub-100nm devices, the materials having low dielectric constant specifically below 2.5 are crucial for minimizing circuit speed delay. On the other hand, most of low-k materials have weak stress resistance and represent intrinsically hydrophobic properties. Due to these characteristics, there are a lot of defects such as delamination, crack, scratch, water mark, and so on. As mentioned Endo *et al.*[2], low pressure controllability is very important technology for minimizing defects of low-k CMP. And a precise post CMP cleaning technology is requested to prevent Cu corrosion and water driven defect due to hydrophobic surface properties.

Noble metals such as Ru, Ir, and IrO2 are expected for their high capacitance characteristics. Especially, Ru is one of the excellent candidates for

capacitor electrode for DRAM. As expected, Ru has the strong resistance to gases and chemicals, and thus, a poor etching rate and selectivity during dry etching or CMP process is observed. As seen in Fig. 4, Ru CMP method is more desirable than dry etching, however, low Ru removal rate and poor Ru to oxide selectivity are still remained as unsolved issues

Fig. 4. SEM photographs of separated Ru capacitor electrode. (a): by dry etching, (b): by CMP.

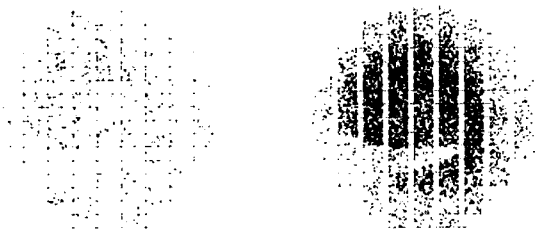


Fig. 5. Observed defect counts on the same wafer. (a) with old tool, (b) with new inspection tool.

4. Defectivity issues in CMP process

Defects generated from CMP process give rise to critical failure in device activity and reliability. Major defects are listed as scratches and particles. Although a improved cleaning methods are adopted to remove defects, the high resolution defect inspection tool catches a lot of scratches and particles. In some cases, it is impossible to inspect meaningful defects such as pattern missing, mask defect or damage owing to tremendous defect counts originated from CMP defects. As seen in Fig. 5, total defect counts measured with old tool is 510, however, new inspection tool of high resolution reads 7400 counts in spite of the same tested wafer. Most of difference between two tools can be attributed to contribution of small-scale scratches and particles. Even though the effect of these small size defects is not clear, these small defects can sometimes prevent from detecting true and critical defects due to computation capability.

Another defect issue would be the organic particles which are attributed to a pad or a brush material. Although most of organic defects can be removed with the aid of plasma ashing, the additional step is inevitable and sometimes they are not eliminated due to a formation of organic-inorganic hybrid material so called sludgy defect . Especially, there are many limitation in process temperature and cleaning chemicals for adopting new materials such as metal gate or advanced dielectric materials.

Reference

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