The Latest Poly-Si TFT Circuit Technologies for System-On-Glass LCD

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Abstract

System-on-glass technology made with low temperature poly-Si TFT has been rapidly advancing in recent years. We have developed a low-power, narrow edged frame, 1.9inch system-on-glass LCD which fully integrates a 16-bit RGB interface driver and all power circuits required for driving the LCD. In this paper, the latest poly-Si TFT circuit technologies used in the newly developed LCD are discussed. The development trends are also reviewed.

1. Introduction

Low temperature poly-Si (LTPS) TFT LCD has been widely used in mobile products, such as digital video cameras, digital still cameras, personal digital assistants (PDAs) and mobile phones. The main reason is because LTPS TFT LCD can realize a high-resolution, high-luminance, compact and highly reliable display, based on its system integration property. In addition, there is the possibility of further advanced integration of systems, such as memories, sensors and signal processors, which will supply new, additional value to users. In this paper, the development trends of system-on-glass technology using LTPS TFT are introduced. The latest poly-Si TFT circuit technologies used in a newly developed 1.9-inch system-on-glass LCD with a fully integrated 16-bit (5+6+5-bit) RGB interface driver and power circuitry, are also discussed.

2. Development Trend

Table 1 shows the system integration roadmap of LTPS TFT LCDs. In 1996, an analog interface driver including a vertical driver and analog sample-and-hold circuits were first introduced for the digital video camera application. Then the technology was extended to a digital interface driver including 4-bit digital-to-analog converters (DACs) for the PDA application in 2000. [1] After that, some functional circuits, such as a low-current DC-to-DC converter, were developed for the PDA and mobile phone applications in 2002. [2] In these 1st and 2nd generations, the TFT carrier mobility was around 50cm^2/V-sec, the threshold voltage was around 2V and the design rule was 3.5μm.

Table 1 System Integration Roadmap of LTPS TFT LCD

Time	Before 2000	2000-2002	2002-2004	After 2005
Generation	1st	2nd	3rd	4th
System Integration	V Driver & Analog Sample Hold	4bit DAC 6bit Selector Low Current DCDC Converter	Completely Integrated RGB Interface High Current Power Circuit leading to Single Power Supply	Multi-bit Frame Memory High Speed Interface Sensor Signal Processors
Interface	Analog (Special Format)	Digital (Special Format)	Digital (Standard 18bit RGB Parallel)	Digital (CPU or RGB Serial)
Application	Digital Video Camera Digital Still Camera	PDA Mobile Phone	PDA Mobile Phone	Advanced Mobile Terminal
Mobility	50 cm2/Vsec	50 cm2/Vsec	100 cm2/Vsec	200 cm2/Vsec
Vth	2V	2V	1V	0.5V
Design Rule	3.5um	3.5um	2.0-3.0um	1.0um

By the end of 2002, we developed a completely integrated, 18-bit (6+6+6-bit) RGB digital interface driver, including a timing controller and 6-bit DACs, for the PDA application using an advanced TFT process technology. [3] In 2003, we also developed a single power supply, 18-bit (6+6+6bit) RGB digital interface driver for the mobile phone application. [4] As described in the table 1, the system integration technology greatly advanced in these years. The development process has already reached the 3rd generation and is now entering the next (4th) generation. The next target of this technology is to create a new, value-added display with advanced integration of various systems, such as frame memories, sensors, signal processors and so on. [5][6] These advanced technologies will be reported by many in the near future. In this paper, I will focus on our latest system-on-glass LCD and poly-Si TFT circuit technologies.

3. Development of a 1.9inch, low-power system-on-glass LCD with 128 x 160 pixels

3.1 Overview

LTPS TFT LCD has an advantage of having ability to integrate the driver circuits with the display on the same glass substrate, while it has disadvantages of higher supply voltage and larger circuit area compared to a conventional Si LSI. This is due to a lower TFT device performance and a relatively larger design rule. It is important to suppress these disadvantages and solve the consequent problems when the technology is applied for mobile phones, because it is critical to have low power consumption and a narrow edged frame. We have developed some unique circuit technologies to achieve these requirements on a 1.9-inch system-on-glass LCD, with fully integrated 16-bit RGB interface driver and power circuits, for the mobile phone application. In the following section, the newly developed circuit technologies are discussed.

3.2 System Block

Figure 1 shows the system block diagram. This panel has a signal interface circuit, two horizontal drivers (H Drivers), a vertical driver (V Driver), a timing generator (TG), two reference drivers, a VCOM driver and three DC-DC converters. The interface circuit receives signals from outside the system and delivers them to the TG. The TG generates the signals which control the H Drivers and the V Driver. Reference Drivers generate reference signals for DACs in the H Drivers. The VCOM Driver supplies a common electrode voltage of the liquid crystal. Three DC-DC converters adjust 2.75V input supply voltage to 5.5V, -2.75V, -4.3V. These voltages are all required for the LCD driver. The integration of these DC-DC converters results in single power supply operation.

The signal flow is as follows. The input RGB signals with 2.75V of amplitude are sampled and latched in sampling latches in the H Driver. Then the signals are converted to analog signals in DACs and output to source lines to be supplied to pixel electrodes according to the output of the Vertical Driver. Finally, the signal is held in the pixel electrodes during one frame cycle. A gray scale corresponding to the analog voltage is displayed.

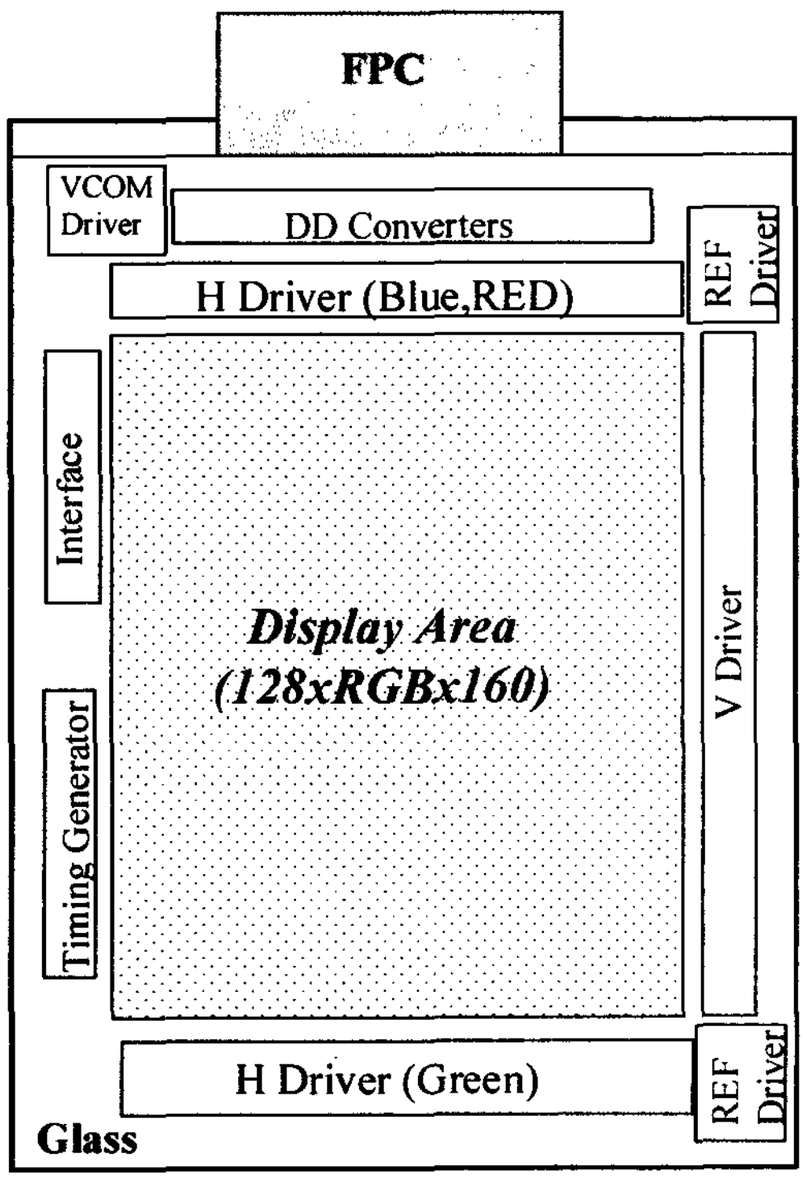

Fig. 1 System Block Diagram

3.3 Horizontal Driver (H Driver)

Figure 2 shows the system block diagram of the H Driver. In this panel, a 5-bit driver for Red and Blue is integrated on the upper side of the panel, while a 6-bit driver for Green is integrated on the lower side. The Red and Blue driver consists of a horizontal shift register, 128 x 5 x 2-bits of sampling latches, 128 x 5 x 2-bits of 2^{nd} level of latches, 128 x 2 blocks of 5-bit DACs and 128 x 2 of CS pre-charging circuits. The Green driver consists of a horizontal shift register, 128 x 6bits of sampling latches, 128 x 6bits of 2^{nd}

latches, 128 blocks of 6-bit DACs and 128 of CS pre-charging circuits.

The operation is as follows. RGB data signals with 2.75V of amplitude are sampled and latched in sampling latches according to an output of the horizontal shift registers. These signals are transferred to a 2nd set of latches, and converted to analog signals in the DACs to be supplied to the source lines. The DAC is a voltage-scaling DAC, which outputs one voltage from some set of reference voltages based on the digital signals in the 2nd level latches. The reference driver is a resistor-strings circuit between 2.75V and ground (GND). The resistor value is set to be a sufficiently small value for charging source lines during one horizontal period. The CS pre-charging circuit charges source lines to the CS signal, which is equal to a black-level signal, just before the DACs supply analog image signals to source lines. Because this operation corresponds to "pre-charging", it helps the drivability of the reference drivers, resulting in an increased resistor value, and thus, decreased power consumption.

In this panel, a 5-bit Red and Blue driver and a 6-bit Green driver are located separately, resulting in an optimized circuit layout of DACs needed for 65k-color display. This is because the reference voltage lines can be shared among DACs of the same bit-resolution, but are hard to share between DACs of differing bit-resolution.

The Red and Blue driver has 10 bits of latches and 2 blocks of DACs for every 3 source lines. Because the pixel pitch of this panel is 240μm, the width of a latch is 24μm and the DAC width is 120μm, there is sufficient room to integrate these circuits using the current LTPS TFT design rule.

On the other hand, the Green driver has 6 bits of latches and 1 DAC block for every 3 source lines. The width of a latch is 40μm and that of a DAC is 240μm, which are larger compared to the Blue and Red driver. Therefore, the DAC circuit is instead designed with a folded layout as shown in figure 3. As a result, the frame edge width in the vertical direction is also greatly decreased. This kind of custom driver design is very suitable for LTPS TFT LCD. This leads to realizing a compact LCD with a narrow edged frame.

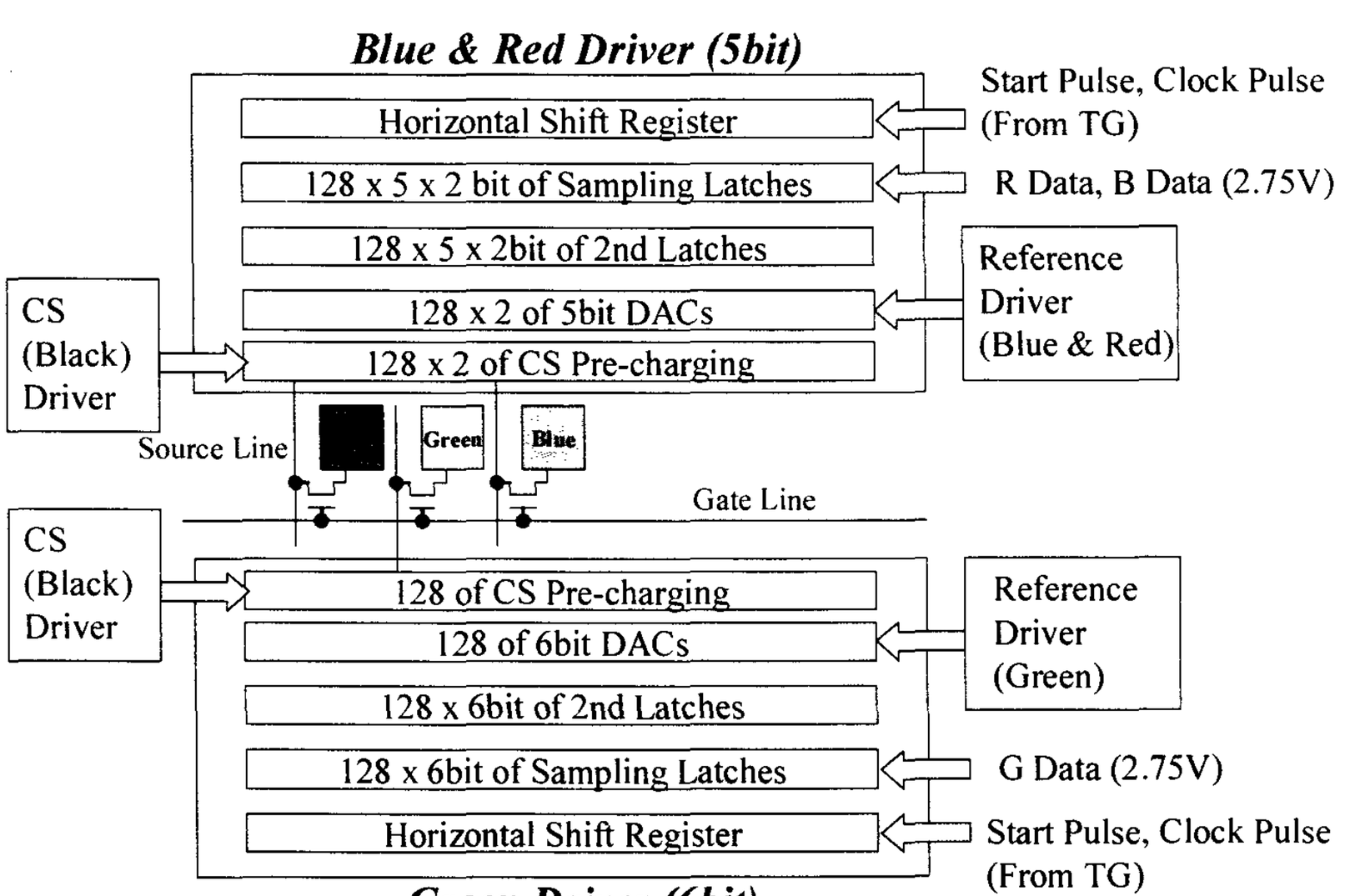

Fig. 2 Horizontal Driver Architecture

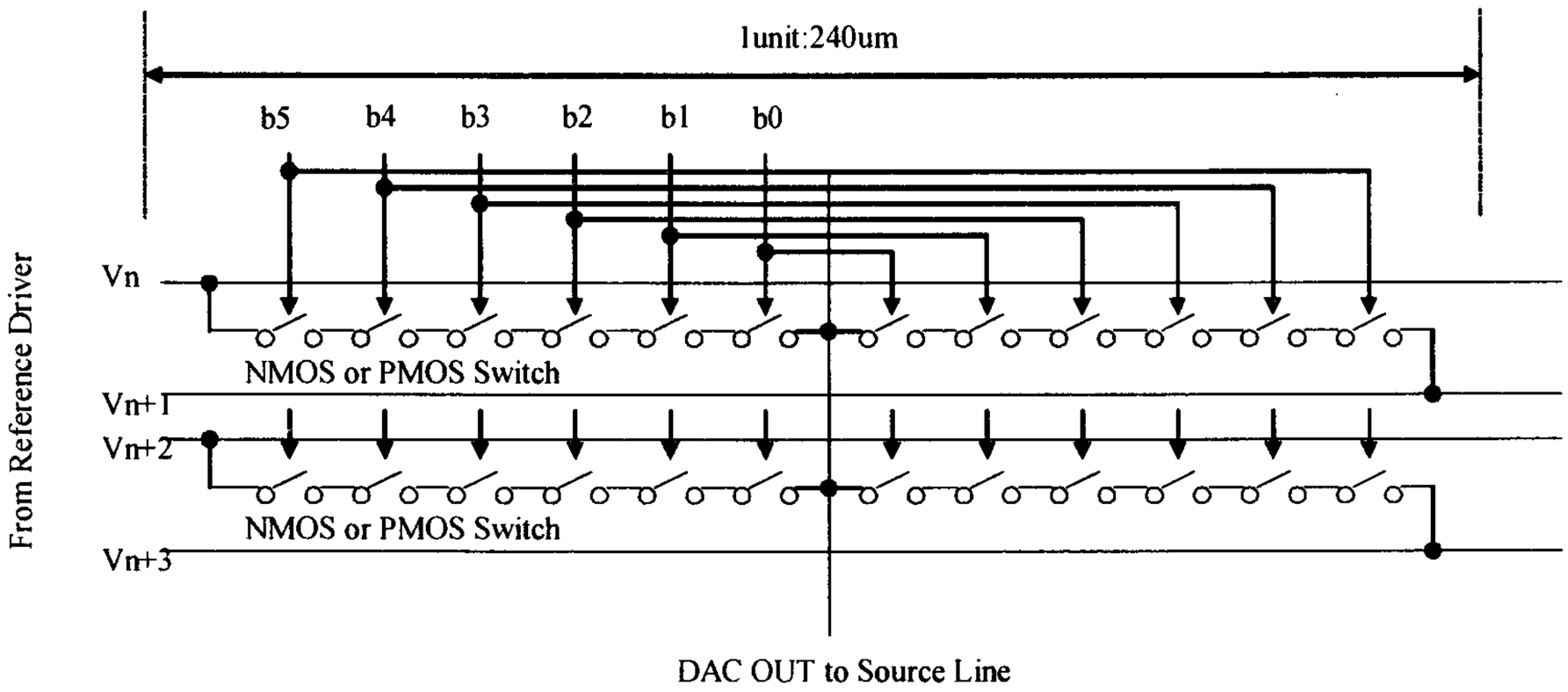

Fig. 3 New DAC Layout for Green

3.4 Timing Generator (TG)

Figure 4 shows the block diagram of the TG. This TG is designed with very narrow layout on the left side of the panel. It consists of two blocks. One is Horizontal Timing Generator (HTG), another is the Vertical Timing Generator (VTG). The HTG has a fine Horizontal Counter (H Counter) which controls the pulse for horizontal shift registers and a coarse H Counter which generates latch pulses and parts of vertical control pulses. The fine H Counter is needed mainly for generating a start signal for the horizontal shift register. It doesn't require a large number of flip-flops, resulting in a small circuit area. The coarse H Counter counts a slow clock during horizontal period to generate some slow signals. Therefore, it also needs only a small number of flip-flops and small circuit area. Consequently, the circuit size of TG is greatly decreased, which leads to a narrow-edged frame in the horizontal direction.

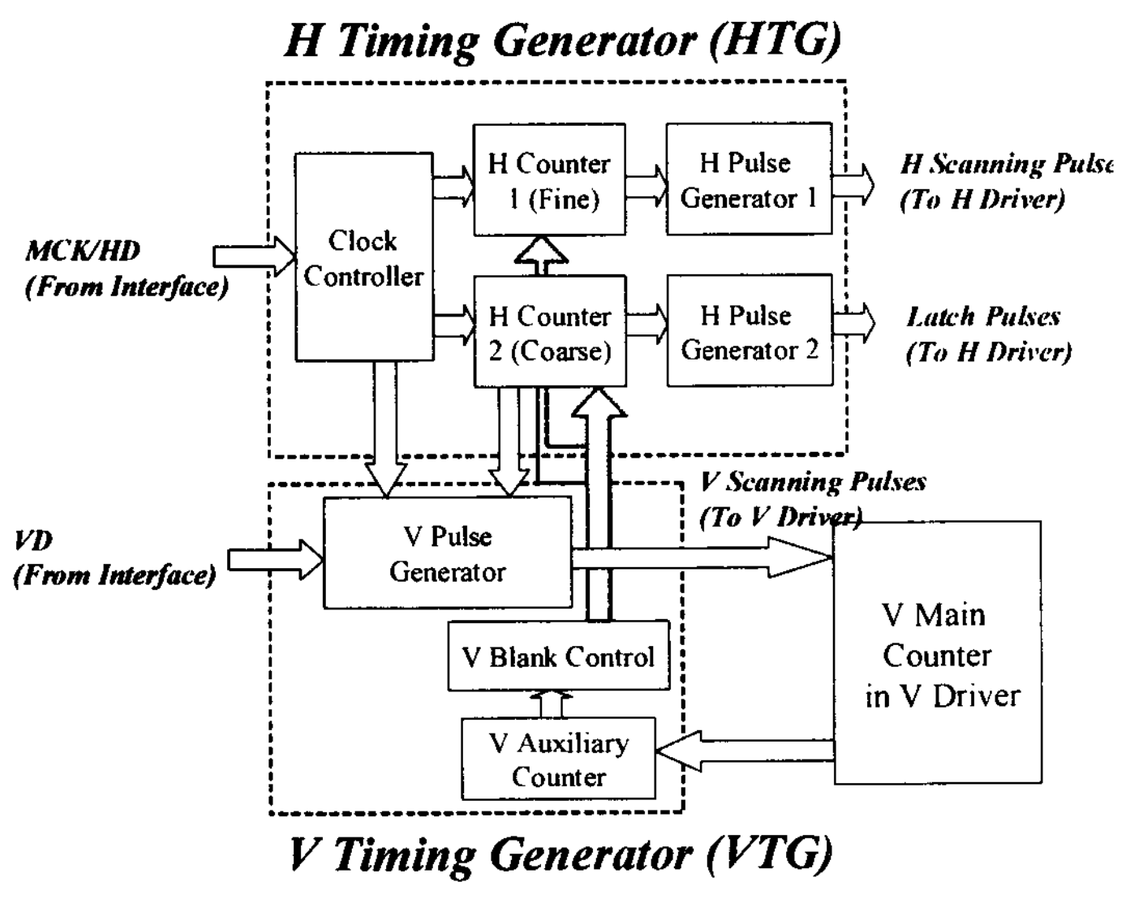

Fig. 4 Timing Generator

The VTG generates pulses for a V Driver and controls the operation of H Drivers in a vertical blanking period. This block doesn't have a large main counter. That function is given to the Vertical Shift Register in the V Driver. This architecture also contributes to decreasing the circuit area and frame edge width in the horizontal direction

3.5 Results

Figure 5 shows the measured power consumption of this panel. The average value is about 4.3mW, which is sufficiently small number for the mobile phone application. Figure 6 shows the measured minimum operating voltage. The average is 1.6V, which is much smaller than the minimum supply voltage (2.6V) of the panel. This means the panel has an enough operating margin needed for mass production. Figure 7 shows the display photograph and table 2 describes the specifications. This panel achieves a narrow edged frame, with 7.3mm for the upper, 3.2mm for the lower, 2.1mm for the right and the left frame edges. This panel fully integrates a 16-bit RGB interface driver and power circuitry required for the LCD, which results in 65k color display with a 2.75V single power supply operation.

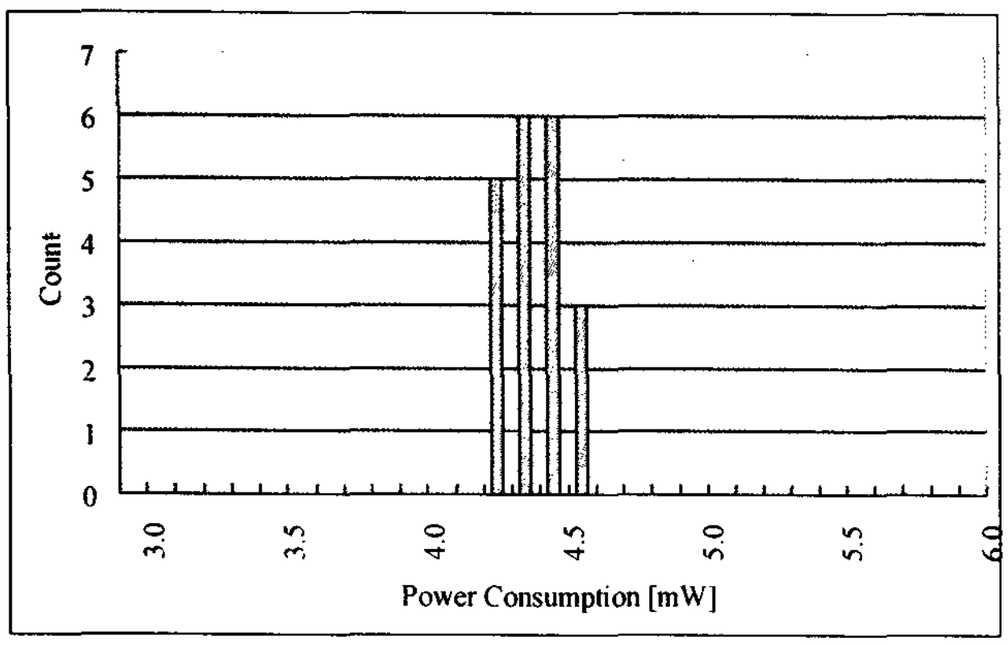

Fig. 5 Measured Power Consumption

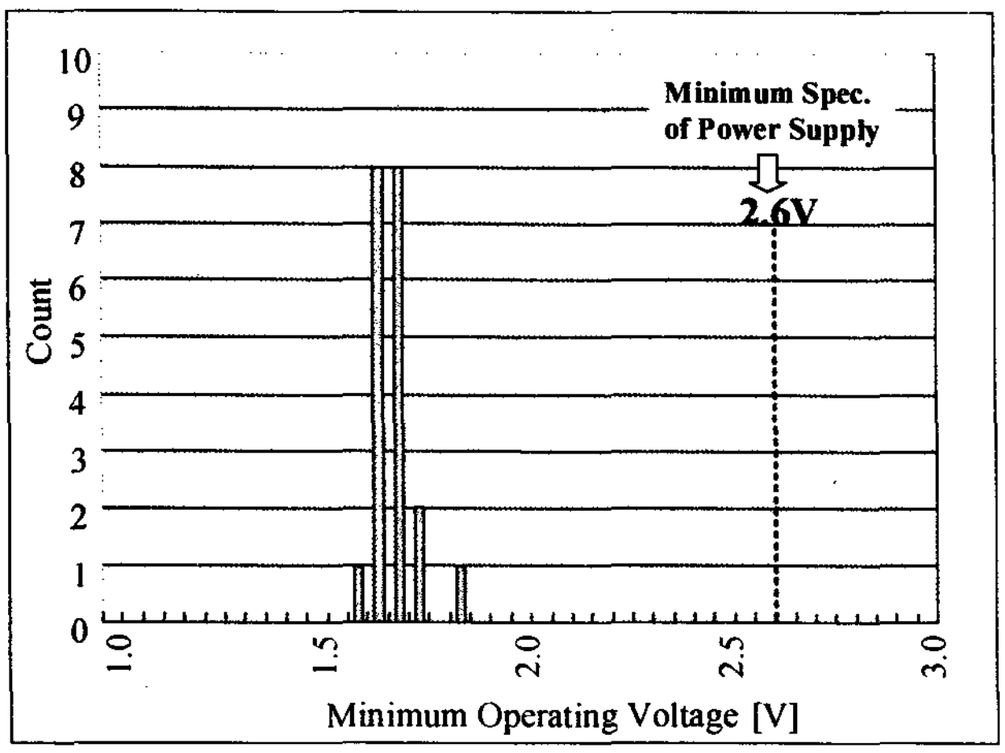

Fig. 6 Measured Minimum Operation Voltage

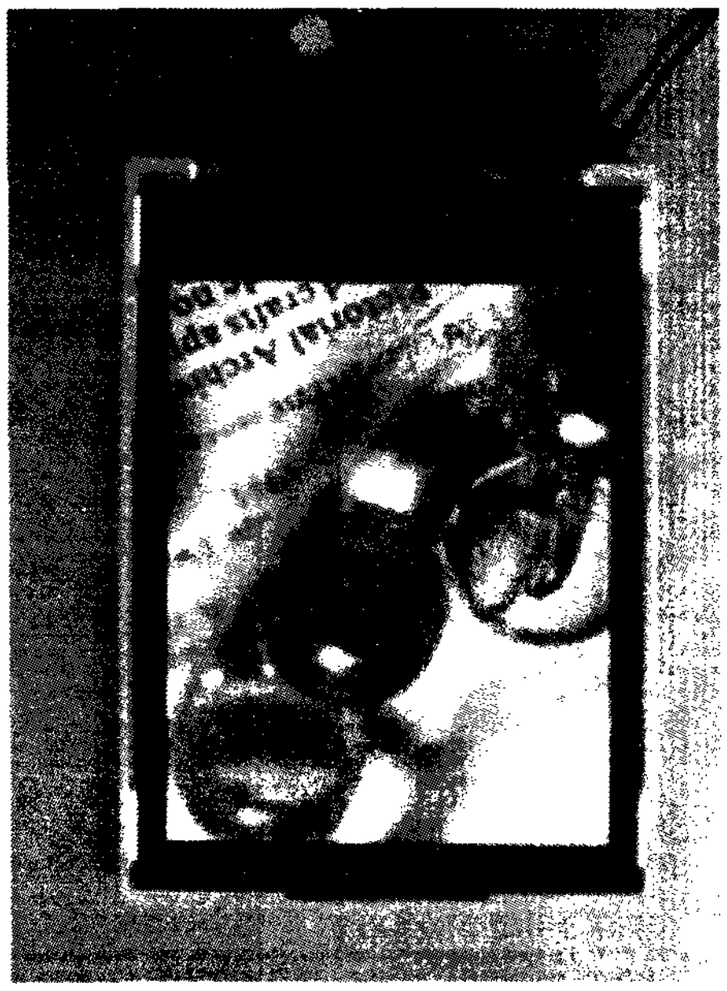

Fig. 7 Display Photograph

Table 2 Specifications

Item		Specifications
Number of Pixels		128 x RGB x 160
Display Size		1.94 inch diagonal
Pixel Pitch		240um x 240um
Liquid Crystal Mode		Transflective
Interface		16bit RGB parallel
Number of Colors		65536
Dot Frequency		1.55MHz
Power Supply Voltage		2.75V
Functions		Completely Integrated RGB Interface Scan Inversion Partial Mode 8-color Mode Fully Integrated DCDC Converter
Frame Width	Upper Lower Left Right	7.3mm (including PADs) 3.2 mm 2.1mm 2.1mm

4. Summary

System-on-glass display technology with LTPS TFT is steadily advancing. We have recently developed a 1.9-inch system-on-glass LCD which fully integrates a 16-bit RGB interface driver as well as power circuits. The LCD can display 65k colors image with a single power supply voltage, consuming only 4.3mW of power. This development will surely lead to far more value-added system-on-glass displays in the near future.

5. References

[1] Y.Nakajima, et al., ISSCC Digest, p188, 2000.

[2] N.Toyozawa, et al., SID 02 Digest, p686,2002.

[3] Y.Kida et al.. Late News Papers of Euro Display 2002.

[4] Y.Nakajima et al., SID 04 Digest, p864, 2004.

[5] T.Ikeda et al., SID 04 Digest, p860, 2004.

[6] T.Nishibe et al, IDW 03 Digest, p362, 2003.