8.2: Invited Paper:*LTPS Technology in ERSO*

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Abstract

A Poly-Si and a ITO films with surface roughness 1.8 nm and 0.5 nm of root mean square (R_{rms} vakue) values were developed, respectively. A 3 inch UXGA LTPS TFT-LCD with 667 ppi resolution and a 10 inch VGA LTPS OLED have been developed and demonstrated using PMOS technology.

1. Introduction

Low temperature poly-silicon thin-film transistors (LTPS-TFTs) technology has become the most promising candidate for AMLCD and AMOLED applications due to its high performance [1-2]. This technology is not only able to realize the integration of LCD driver circuit but also system circuit on the glass. Although LTPS-TFT LCD and LTPS-TFT OLED can be developed by using PMOS or CMOS technology, the fabricated process can be simplified and the cost can be improved by using PMOS technology[3-4]. Conventionally, the resolutions for TFT LCD are widely used from 100 to 200 ppi. However, these are not sufficient to display higher quality of image required subject such as digital camera and high-end projectors [5-6]. In this paper, a 3 inch LTPS-TFT LCD with resolution of 667 pixel-per-inch(ppi) has been successfully developed and demonstrated using PMOS technology.

As to AMOLED application, LTPS-TFT is not only able to integrate circuit to the glass but also provide a stable characteristics compared with amorphous Si TFT. Since OLEDs are current-driving devices, LTPS-TFTs are required to supply a enough current to drive each OLED pixel. The gray-scale scheme of AMOLED displays is achieved by modulating the different current level to each pixel. However, the gray-scale control has become an important issue due to the non-uniformity feature of LTPS-TFTs caused by the fact that the grain boundaries and sizes of poly-Si. Traditionally, the uniformity is difficult to control during the laser crystallization process of poly silicon formation. In this paper, we proposed a new pixel circuit [7]and smooth poly-Si thin film surface[8] to improve the LTPS-TFTs non-uniformity issue. In addition, we developed a ultra smooth surface of ITO film to improve the image quality and the panel life time[9-10].

2. Experiment

A top gate structure was adapted to fabricate P-type self-align (SA) TFTs on NEG OA10 annealing glass. At the first step of process, 300nm silicon oxide and 50 nm a-Si thin films were deposited as buffer layer and active layer, respectively. A 50 nm a-Si layer was crystallized to become poly-Si thin film by XeCl excimer laser crystallization and 98% laser overlap ratio in N_2 atmosphere at room temperature. TFTs active area was patterned and defined by dry etching. Subsequently, a 100 nm gate insulator was deposited by PECVD TEOS-based oxide, followed by a 450 ℃ annealing. The gate electrode(MI) was followed to deposit and then define by dry etching. The p+ was self-aligned doped by through the gate electrode. The 400 nm inter-layer was formed and then contact opened by etching process. The source and drain electrodes (MII) were deposited and then defined by the dry etching process. The p+ doping activation was performed by furnace annealing. The cross section of our p-channel poly-Si TFTs is shown in Figure 1. The channel length is 5um and the channel width is 10 um. The design rule is 2 um in this process.

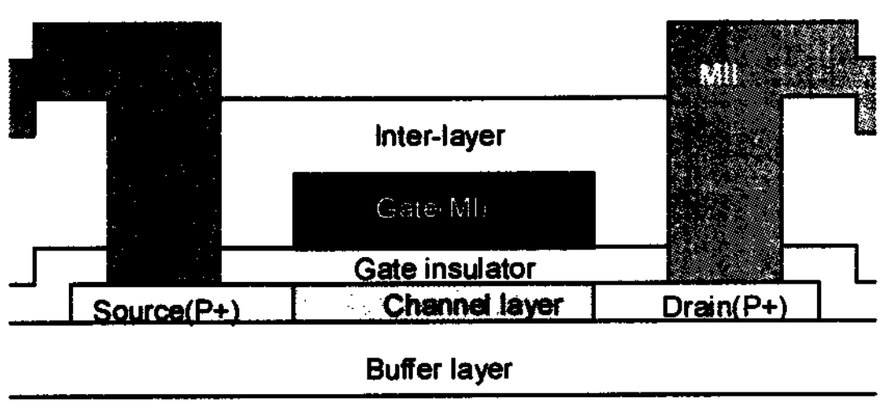

Figure 1. A cross section of p-channel TFT.

3. Results and Discussions

3.1 LTPS on LCD

The relation between the laser energy density and grain size of the crystallized poly-Si film is shown in Figure 2. From this figure, it is found that the grain size of poly-Si is strongly related to the excimer laser energy density. As the laser energy density is small (<320 mJ/cm^2), a smaller grain size of poly-Si is observed. As the laser energy density increases to a suitable value (330 mJ/cm^2), a larger and uniform grain is obtained. As the energy increases over 330 mJ/cm^2, a localized fine-grain of poly-Si is observed.

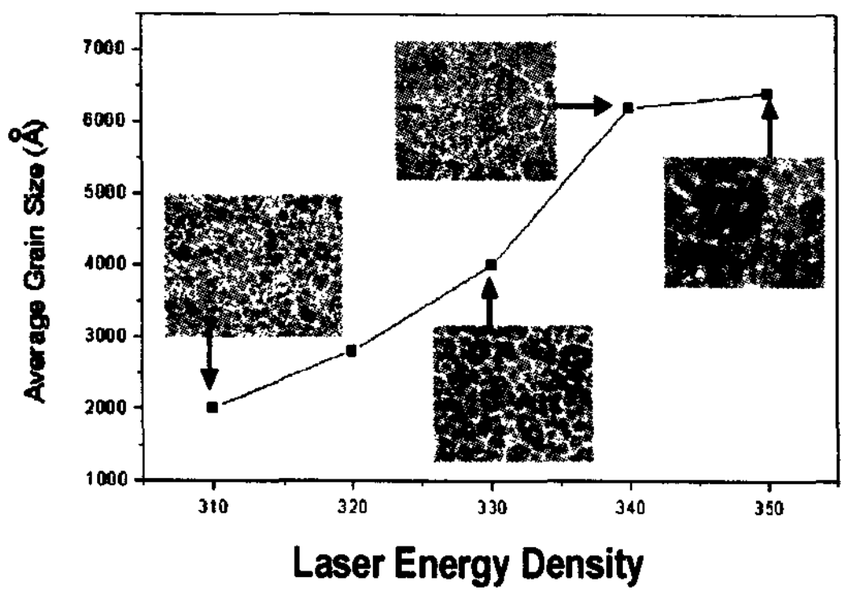

Figure 2. The relation between the average grain size (Å)and the laser energy density(mJ/cm2).

3.1.1 Surface Smooth Technology for Poly-Si

In the conventional process, surface roughness was about 12 nm(R_{rms}). However, surface roughness can be reduced to 1.8 nm(R_{rms}) using a additional proper processes. In these processes, native oxide, weak bonded silicon and unwanted impurities were removed. It is reported that oxygen ambiance and native oxide on surface prevents the relaxation of surface stress, and contributes to have less surface roughness [11]. These processes are started from etching process followed by additional ELA process. The additional laser annealing process allows partial melting of poly-Si and causes the melted silicon to reflow from ridges and vertices. Afterward the liquid silicon solidifies from under un-melted poly-Si. Since solidification occurs from bottom to top, there is less lateral driving force to form protrusions. Therefore, surface could be flattened to an extreme level less than 2 nm(R_{rms}). AFM stereographs of poly-Si fabricated by conventional and smooth processes were shown in figure 3.

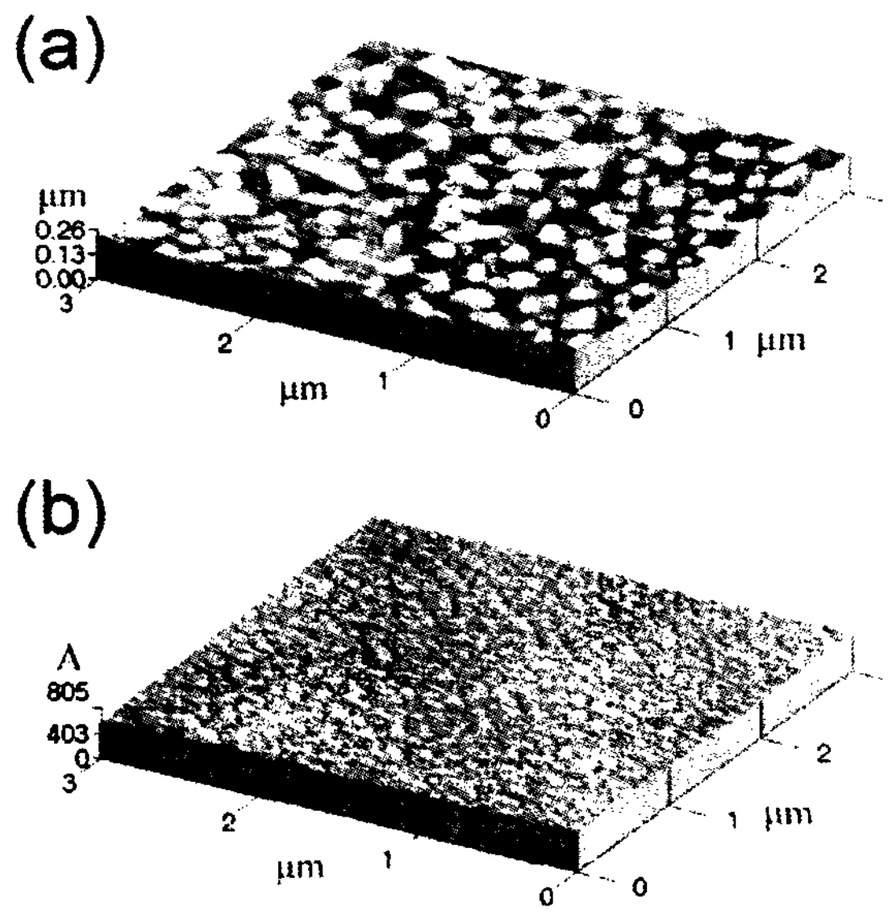

Figure 3. AFM stereographs of (a) conventional process poly-Si with roughness of R_{rms}~12 nm and (b) smooth process poly-Si with roughness of R_{rms} ~1.8 nm.

3.1.2 Less Thickness Variation of Gate Insulator

In addition, the study of the roughness effect on the gate insulator thickness was performed. As shown in Figure 4, rough poly-Si surface formed by conventional ELC would cause the local thickness lost of gate insulator film. In figure 4(a), an estimated 100 nm thickness of gate insulator film was deposited on rough poly-Si, and we found thickness lost was about 10 to 15% in the grain boundary ridges and vertices. As gate insulator thickness was reduced to 25 nm, the maximum lost could attain 30% as showed in Figure 4(b). The controllability of gate will be affected significantly and TFTs performance will be degraded. This issue becomes serious for thinner gate insulator. Figure 4(c) shows thin gate insulator deposited on smooth poly-Si, no obvious thickness lost was found. The roughness due to conventional ELC process may be an issue for thin gate insulator of TFTs device reliability and performance. As a consequence, this poly-Si smooth process can be an effective way to improve this issue.

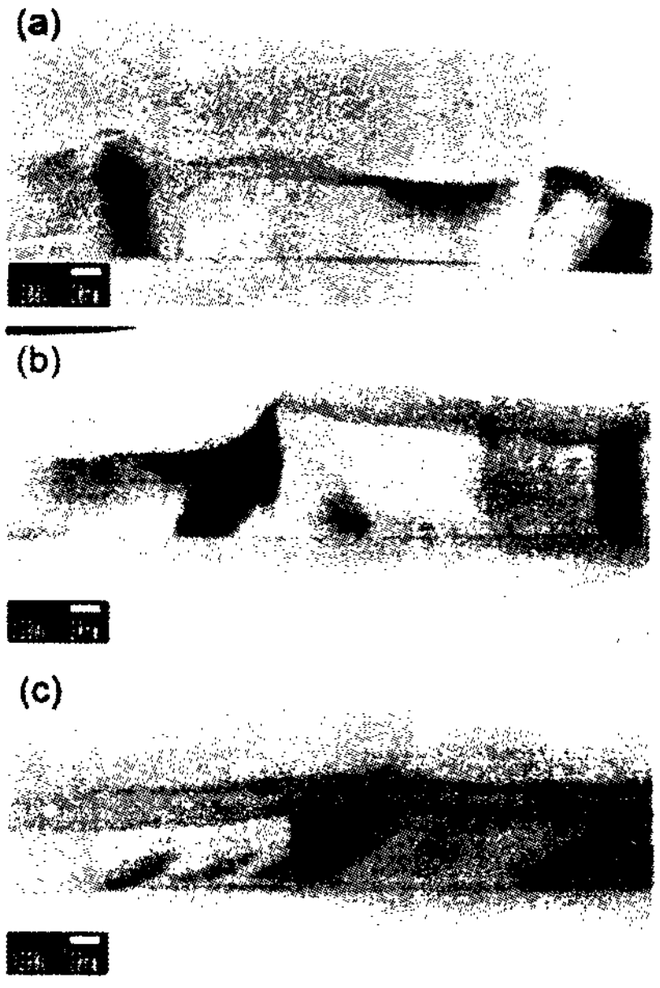

Figure 4. TEM photograph of poly-Si with (a) gate oxide thickness of 100 nm on rough poly-Si, (b) thin gate oxide thickness of 25 nm on rough poly-Si and (c) thin gate oxide thickness of 25 nm on smooth poly-Si thin film.

3.1.3 Highest Resolution TFT-LCD Panel

Based on the previous technique, we have successfully developed 3-inch diagonal sizes with XGA (427ppi) and UXGA(667ppi) resolutions LCD by LTPS TFTs technology, respectively. The image of 3-inch LTPS TFT-LCD panel with UXGA resolution and 6-bits gray scale was shown in Figure 5. The small pixel pitch of 13x39 μm and high aperture ratio of 26% was realized.

Figure 5. Image of 3-inch UXGA LTPS TFT-LCD.

3.2 LTPS on OLED

3.2.1 Less Surface Roughness of ITO Thin Film

A smooth surface of ITO layers which is served as an anode electrode of OLEDs can improve the image quality and panel lifetime[10]. We have successfully developed a highly smooth surface morphology of ITO and apply to active-matrix OLED displays. The AFM was used to investigate it. Figure 6 shows the AFM photograph of ITO which is processed at 140 °C.. The thickness of ITO thin film is 100 nm and the corresponding resistivity is about 200 μΩ-cm .From the Figure 6, the R_{rms} value was observed about ~0.5nm.

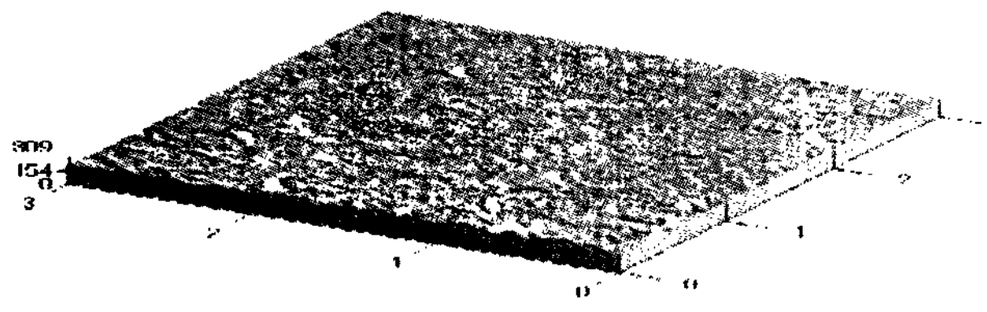

Figure 6. AFM photograph of ITO which is processed at 140 °C.

3.2.2 New Pixel Driving Circuit for OLED

A novel pixel structure with five transistors and one capacitor (5T1C) of AMOLED was developed. The schematic is shown in Figure 7.

T1 was used as switch to sample the data from the data lines. T2 was a driving TFT which supply a constant current passing through the OLED. T3 and T4 were the TFTs to compensate the threshold variation of the T2. The function of T5 was used to eliminate the IR drop of power line of VDD. Therefore, it was possible to control OLED current independent of the threshold voltage of driving TFTs.

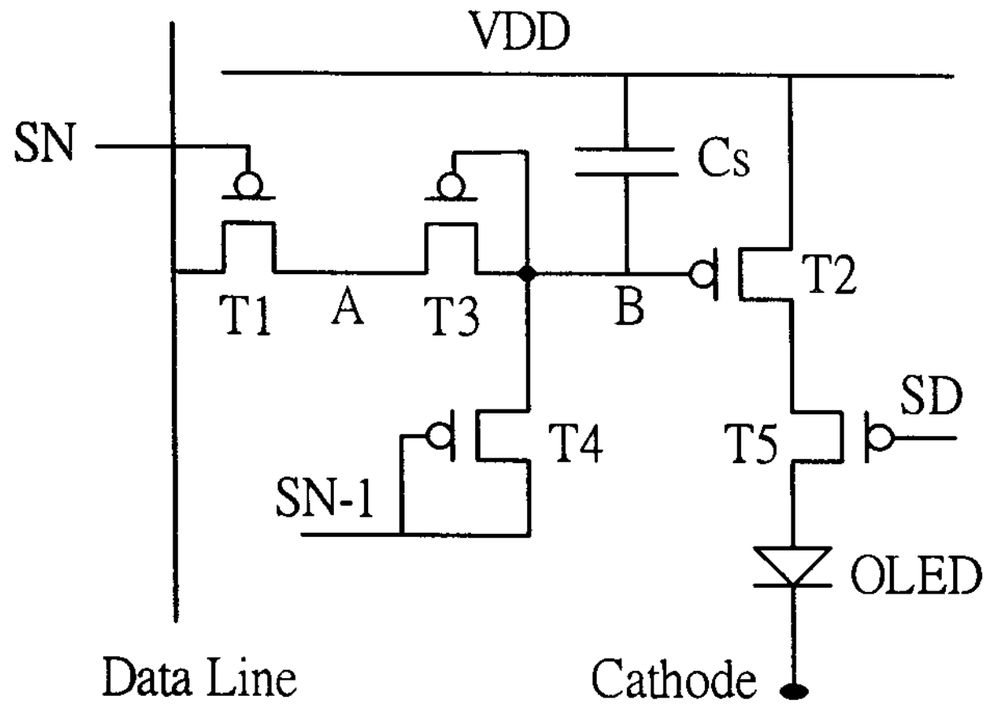

Figure 7. The schematic of proposed novel pixel structure of AMOLED.

Compared the conventional pixel structure which was two transistors and one capacitor(2T1C), the output current variation with two different current levels under the condition of the threshold voltage variation,ΔVth=4±1V, the uniformity of output current for our proposed pixel structure was improved more than 50% comparing to the conventional 2T1C pixel structure under the same TFT threshold voltage variation. The simulation results were listed at Table 1.

Table 1. The simulation results of proposed schematic(5T1C) and 2T1C.

Vt	Proposed (uA)	ERROR	2T1C (uA)	ERROR
3V	3.506	6.6%	5.659	72.5%
4V	3.288	0	3.281	0
5V	2.962	9.9%	1.246	62%
Vt	New (uA)	ERROR	2T1C(uA)	ERROR
3V	1.763	1.0%	3.961	122.7%
4V	1.744	0	1.778	0

3.2.3 Large Size of LTPS AMOLED Panel

Based on the previous technique, we have successfully developed 3.8-inch diagonal sizes with QVGA resolutions OLED by LTPS TFTs technology. For the large size of panel requirement, we have also used a 5T1C pixel structures and successfully developed 10-inch diagonal sizes with VGA resolutions LTPS AMOLED display. The image of 10-inch LTPS AMOLED was shown in Figure 8. The corresponding panel specifications were listed at Table 2.

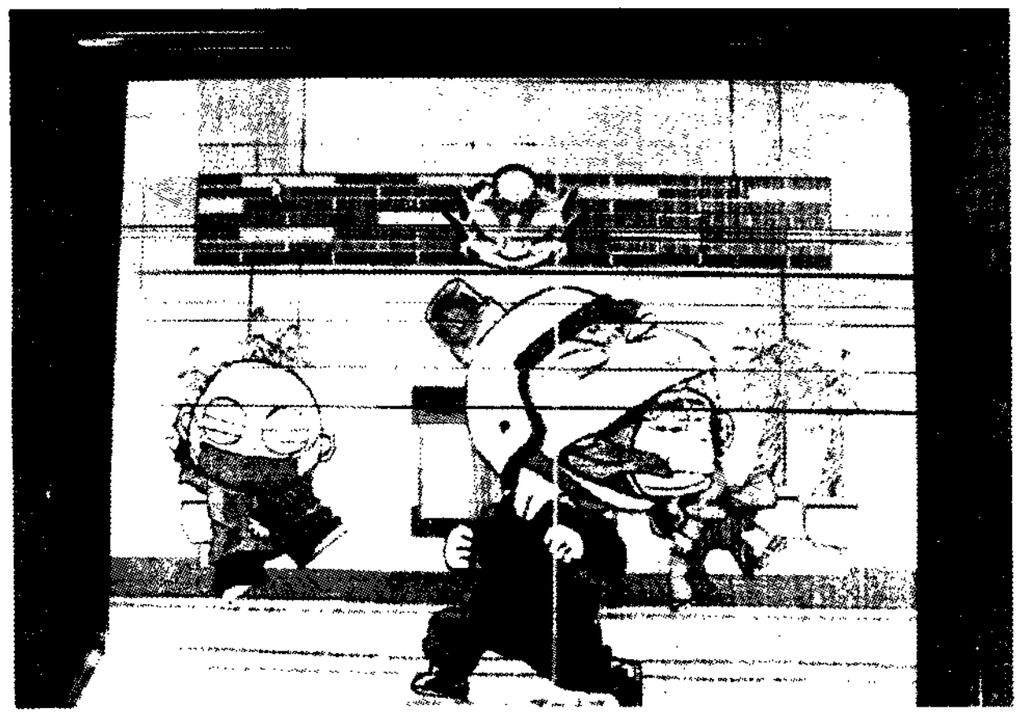

Figure 8. Image of 10-inch LTPS AMOLED.

Table 2. The specifications of 10-inch LTPS AMOLED.

Display size	10-inch diagonal
Resolution	640 × 3 ×480
Gray scale	4 bits
Brightness	300 nits(cd/cm2)
Pixel pitch	(90 μm×3) × 360 μm
Aperture ratio	30%
Pixel Structure	5T1C
OLED structure	Bottom emission
Scan driver	Integrated scan driver

4. Conclusion

A Poly-Si and a ITO films with smooth surface roughness are developed. A 3 inch UXGA LTPS TFT-LCD with 667 ppi resolution and a 10 inch VGA LTPS OLED have been developed and demonstrated using PMOS technology.

5. Acknowledgements

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