Device Physics of Low Temperature Poly-Si and Single Grain TFTs

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ABSTRACT
Static and transient behaviour of Low Temperature Poly-Si TFTs (LTPS-TFTs) and Single Grain TFTs (SG-TFTs) are compared. 3-D simulation is applied here for the first time to TFTs to account for the structure and twin boundaries in SG-TFTs.

1. INTRODUCTION

Low Temperature Poly-Si (LTPS) TFTs and Single Grain (SG) TFTs have much in common with SOI MOSFETs, but the presence of gap states in considerable concentration results in their unique static and dynamic behaviour. For LTPS, the relationship between gap states distribution and TFT figures of merit, e.g. threshold voltage and mobility, has been analysed in many papers. It has also been shown that a detailed knowledge of the generation-recombination (g-r) mechanisms and their dependence on electric fields is necessary in order to account for the leakage current in these devices.[1] More recently, the transient behaviour of LTPS TFTs has been studied and found strongly influenced by both the gap Density of States (DOS) and the energy dependence of the carrier capture cross sections[2]. In the present paper we compare and contrast the static and dynamic behaviour of LTPS and SG TFTs. The LTPS TFTs studied here were fabricated by laser re-crystallization according to the process previously reported.[3] The SG-TFTs were fabricated by the Micro-Czochralski (μ-CZ) method[4]. This technique, developed at Delft Technical University, is capable of producing TFTs with mobilities exceeding 500 $cm^2 V^{-1} cm^{-2}$. For LTPS devices 2-D simulation, with the assumption of a spatially continuous DOS, is adequate. This is not true for SG-TFTs, due to the device structure with a central "neck". Furthermore twin boundaries have been identified in SG-TFTs and correlated with the device performance[5]. To gain detailed information on the effect of these defects on the device characteristics we employ 3-D simulation with the ISE software. The hydrodynamic model is used to account for hot carrier effects. Fig.1a and Fig.1b shows the SG-TFT structure used in the simulation. The thickness of gate oxide is 100nm, and the gate size is 2μm/2μm. We model the twin boundary as a planar defect with a density of gap states given in Fig.2.

2. STATIC CHARACTERISTICS

The SG-TFT transfer characteristics are simulated for a twin boundary centred midway between source and drain. The angle α between the boundary and the source-drain direction is varied, $\alpha=0°$ indicating a boundary parallel to the channel. The results are presented in Fig.3. For $\alpha > 45°$ the boundary completely obstructs the current path. The simulation shows that under these conditions the current is limited by thermionic emission above the barrier and is therefore proportional to the twin boundary area, which increases for decreasing α. For $\alpha < 45°$ only part of the channel is obstructed so both drift and thermionic emission play a role. The I-V characteristics of LTPS TFTs show little asymmetry for source-drain reversal. Asymmetric behaviour is instead observed for Single Grain TFTs. The effect of a twin boundary on the off current is simulated in Fig.4. If the boundary is in contact with the

[1] O K B Lui et al., Solid-State Electron., **41**, 575, (1997).
[2] N G Bavidge et al., Appl. Phys.Lett.,**77**, 3836,(2000).
[3] S Inoue et al., Proc of Asia Display'95, p.339.
[4] R Ishihara et al. Proc. SPIE, **4295**, 14.(2001)
[5] R Ishihara et al. Proc. SPIE, **5004**, 10, (2003)

source, it has little effect whereas when in contact with the drain it produces a tenfold off-current increase. This is due to the higher generation rate associated with the twin boundary defects. Fig.5 shows the experimental output characteristic of a single grain TFT. The kink effect (Fig.5a) disappears when source and drain are exchanged (Fig.5b). This effect can be reproduced in simulation (Fig.6). We find that the position of the twin boundary is very important for the kink effect. A large kink effect can be observed when the boundary is close to the drain whereas no kink is observed when it is close to the source. Hence the asymmetry for source-drain swapping. According to the simulation results, the effect is due to the enhancement of the electric field and the associated impact ionization at the twin boundary. Such enhancement is strongly dependent on the density of traps at the boundary.

3. GATE SWITCH-ON TRANSIENTS

Fig.7 shows the transient for two LTPS TFTs with different DOS. The shorter and smaller overshoot is that of the better TFT. A similar overshoot has been observed in SOI-MOSFETs.[6] The effect can be explained in the following way. When a positive voltage step is applied to the gate of a n-channel device, the body floats positive with respect to the source, forward biasing the source-to-body junction. The steady-state is achieved through electron injection from the source into the body. Some of these electrons are driven towards the interface to form the conductive channel (charge per unit surface Q_n), the rest recombine with the background holes, giving rise to the depletion region (charge per unit surface Q_B). The latter process requires a finite time, as the current through the source/drain body junctions is limited. Since $Q_n+Q_B \approx C_{ox}V_{GS}$, if $Q_B(t) < Q_B(\infty)$ then $Q_n(t) > Q_n(\infty)$ and an excess drain current is observed. As the source-body recombination current is inversely dependent upon the carrier lifetime τ, and the number of holes to be recombined is proportional to the acceptor concentration N_A, the transient time increases with τ and N_A. If the SOI-MOSFET is fully depleted, the transient becomes extremely short. In poly-Si the carrier lifetime is of the order of nanoseconds and the active layer is intrinsic. Therefore, one expects very fast transients. By contrast, we observe transients lasting several milliseconds. The different behaviour of poly-Si TFTs compared to single-crystal SOI is due to the fact that poly-Si is undoped (Fermi level near the mid-gap), so the formation of the depletion region proceeds through capture of electrons into initially empty states, rather than through recombination of free holes. Under these conditions, the transient consists, for n-channel devices, of contributions from all acceptor-like traps in the upper half of the bandgap: the tail states, with a larger capture cross section, are responsible for the fast transient portion (not shown) whereas the deep states, with smaller cross sections, give rise to the long transient shown in Fig.7. One expect that the overshoot is higher in magnitude for increasing concentration of gap states. Simulations are reported in Fig.8, which explain the differences between the two samples of Fig.7. As can be seen from Fig.9, the overshoot is dependent on the off time between pulses t_{off}.[7] The influence of the t_{off} can be explained as follows. The traps below the final Fermi level fill with electrons during the on pulse. After switch off, when the equilibrium conditions are reached, the Fermi level moves back towards the centre of the energy gap. All of the trapped electrons above the equilibrium Fermi level must be emitted into the conduction band. As explained before, the overshoot appears when the trapped electron concentration after gate switch-on is lower than that at steady state, the difference being made up by free electrons. Hence, if t_{off} is so short that the trapped electrons have no time to be emitted, no overshoot is present. The overshoot is much reduced, but still present, in SG-TFTs (Fig.9), although in principle

[6] H.C. Shin et al., IEEE Trans. Electron Devices., **43**, 318,(1996).

[7] P Migliorato et al., Proc. of IDW'03,p.327

these devices should be fully depleted. We speculate that in SG-TFT a different mechanism may contribute to, or dominate the overshoot, namely the time dependence of potential barriers associated with twin boundaries. One expects that the grain boundary barrier height increases with the amount of charge trapped in it and, therefore, that the effective mobility decreases with time. Figs.10 and 11 show the results of a 2-D simulation by using the hydrodynamic model in the ISE software. At the moment no attempt has been made to reproduce in simulation the dynamic behaviour of a SG-TFT, since the computing power needed for 3-D transient simulation is not yet available to us. The present results support however the argument that the modulation of twin boundary barriers can be an important contribution to the transient behaviour of SG-TFTs.

4. CONCLUSIONS

Static and dynamic characteristics of LTPTS and Single Grain TFTs have been compared. Both static and dynamic behaviour of LTPS TFTs is satisfactorily accounted for by assuming a spatially continuous distribution of gap states and 2-D device modelling is adequate in most cases. By contrast, in SG-TFTs defects can be localized at one or more twin boundaries so that 3-D modelling is necessary. Simulation shows that the location and orientation of the twin boundaries affects mobility, off-current and kink effect. The time dependence of the barrier height, associated with twin boundaries, can be important for the dynamic behaviour of SG-TFTs.

AKNOWLEDGEMENTS

This work was supported by the Seiko Epson Corporation.

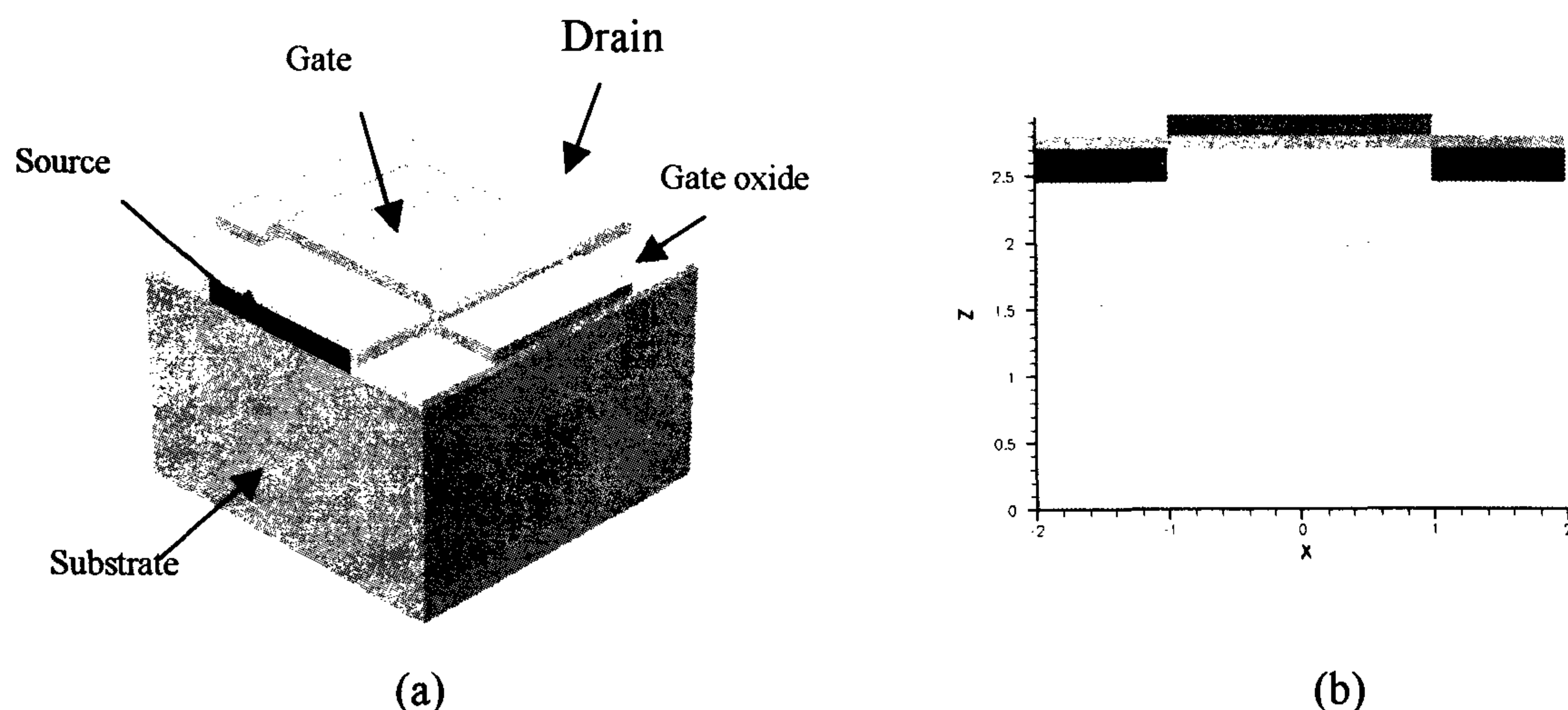


Fig.1, (a) Three-dimensional view of the SG-TFT device for simulation. (b) Cross-sectional view of the device, showing the central filter characteristic of the . Micro-Czochralski technique

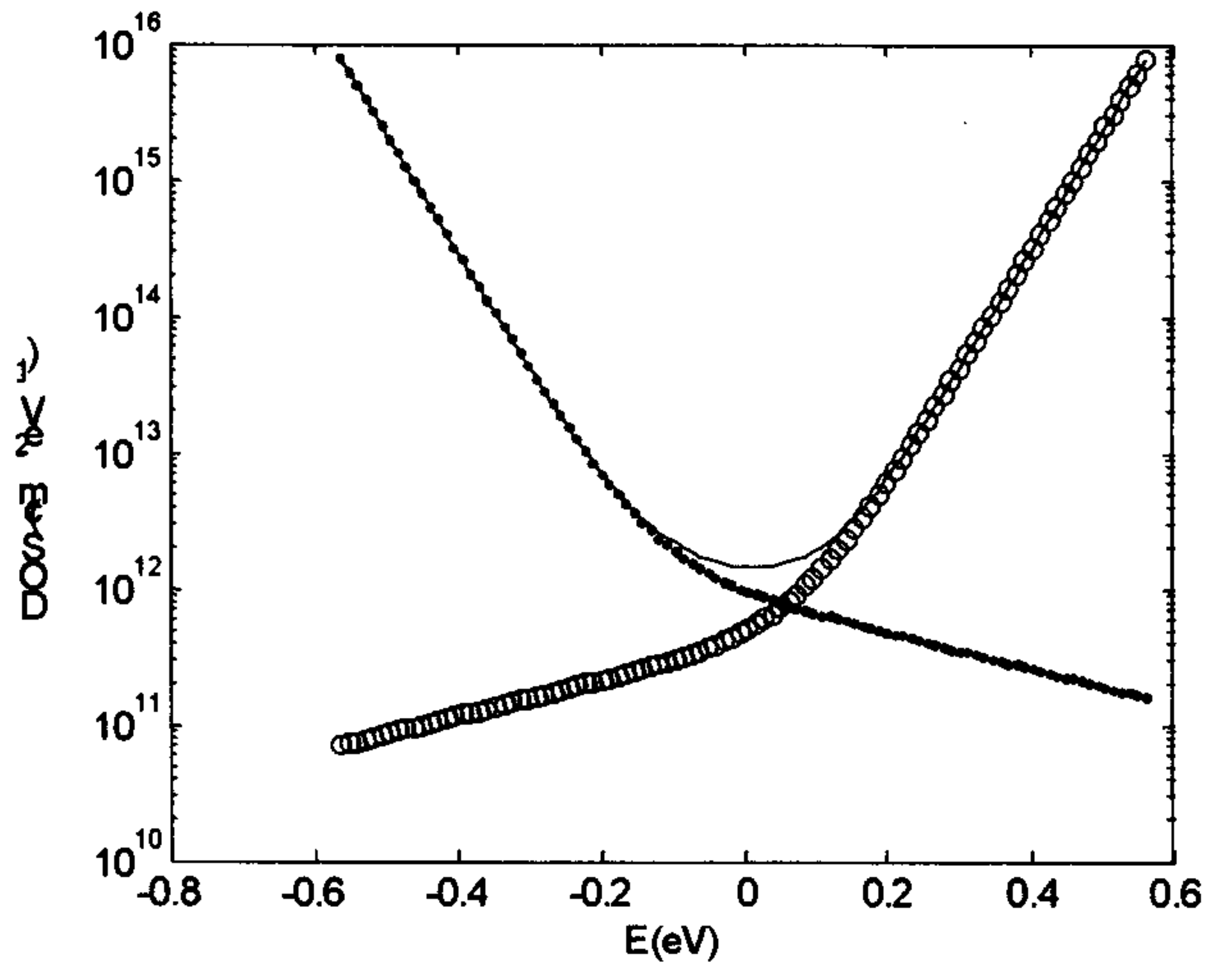


Fig.2 The density of trap states (DOS) in the twin boundary used in the simulation

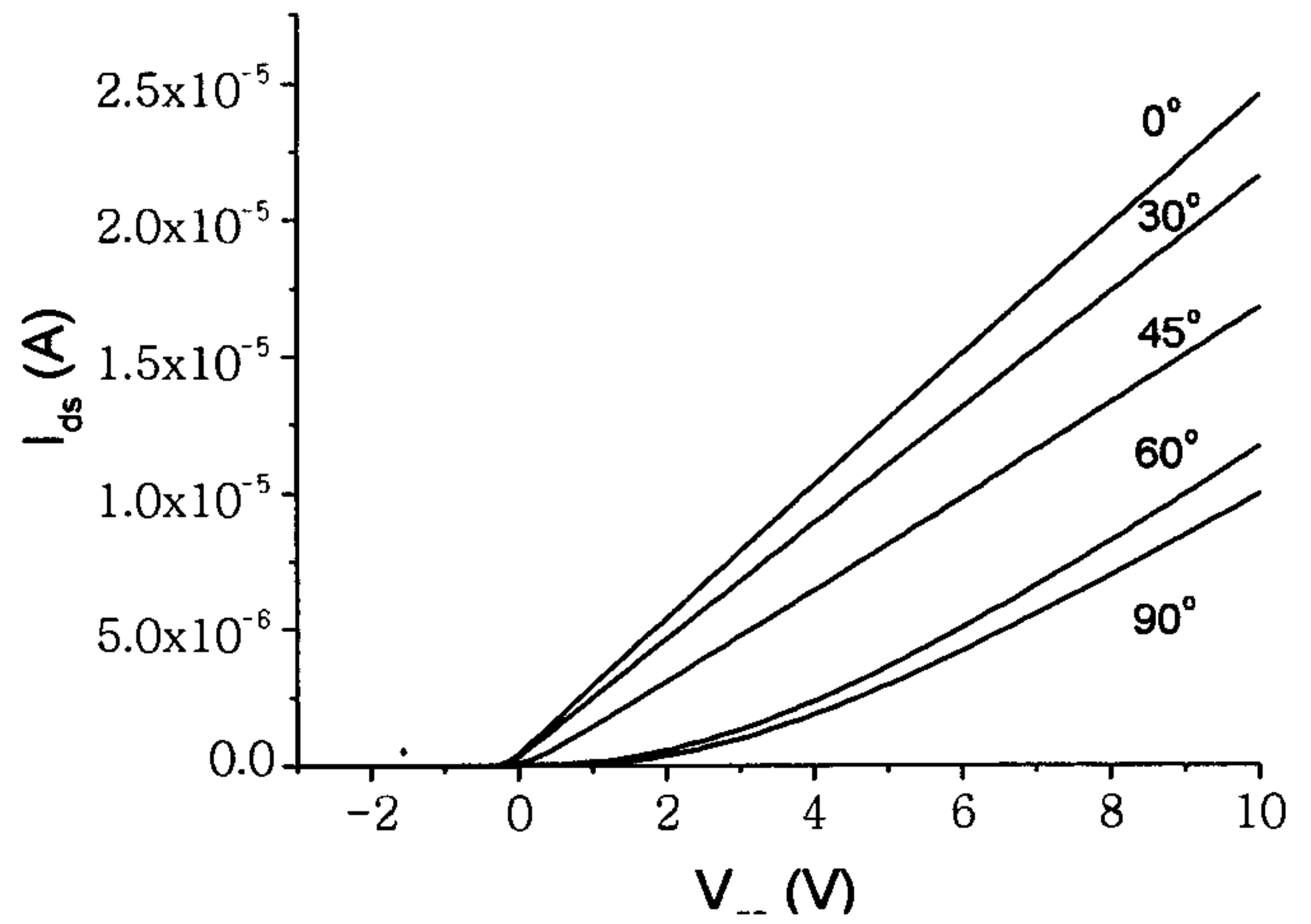


Fig.3 Simulated transfer characteristics for a SG-TFTs with one twin boundary centred in the middle of the channel. V_{ds}=0.1V. The angle between the twin boundary and the direction from source to drain varies from 0 to 90 degrees.

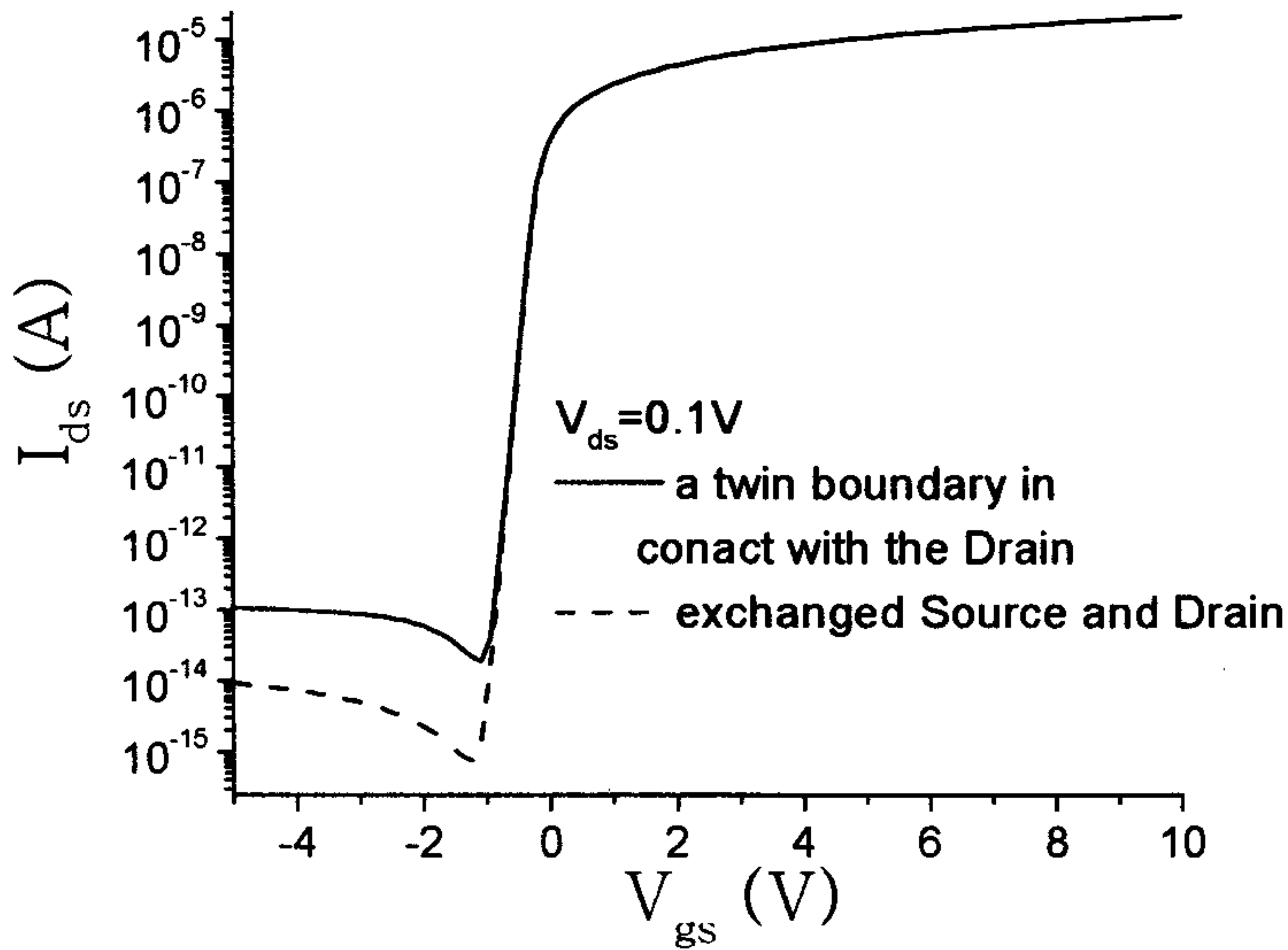
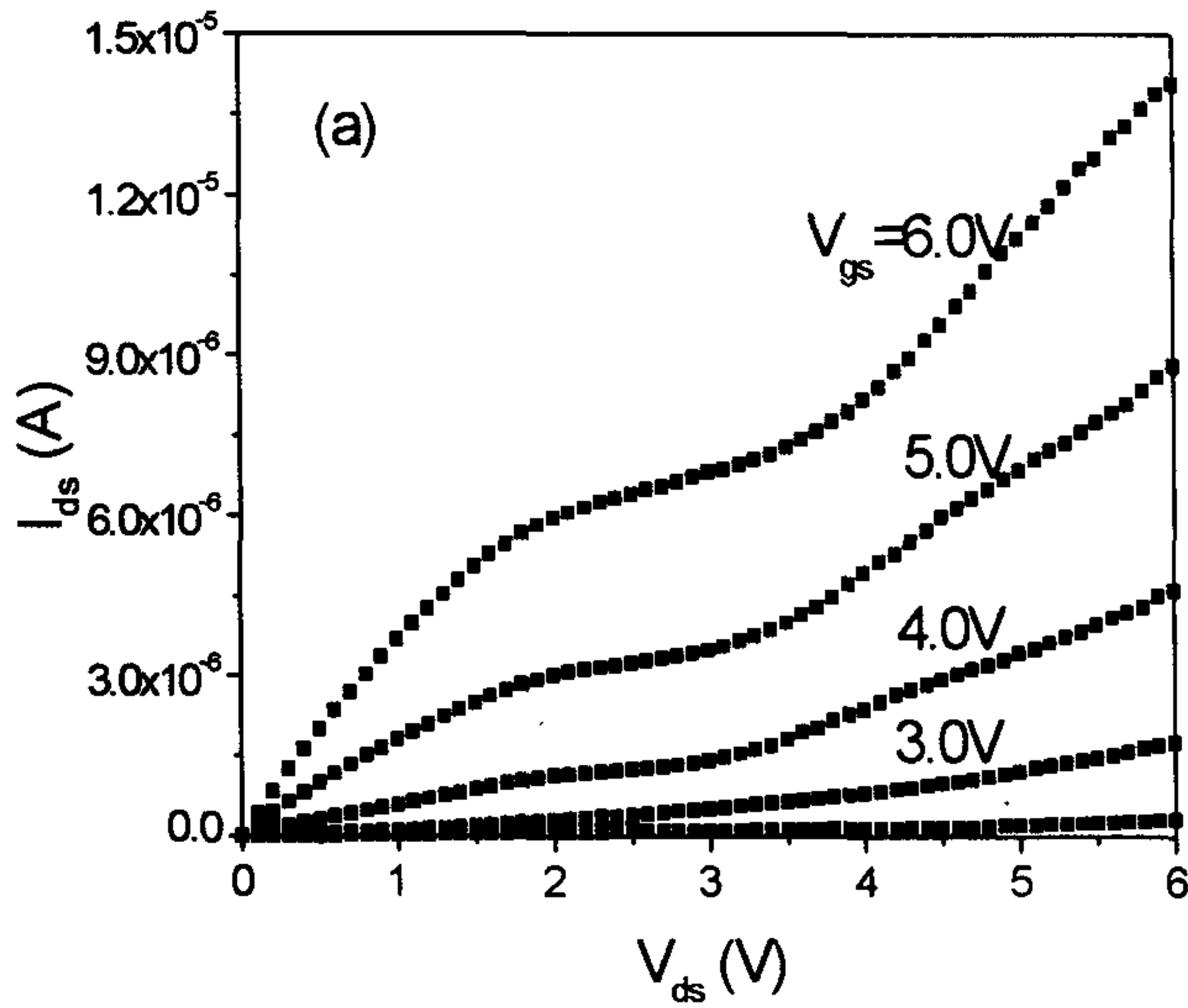


Fig.4 Simulated transfer characteristics for a SG-TFT with a twin boundary in contact with the drain (solid line) or the source (dashed line). V_{ds}=0.1V.



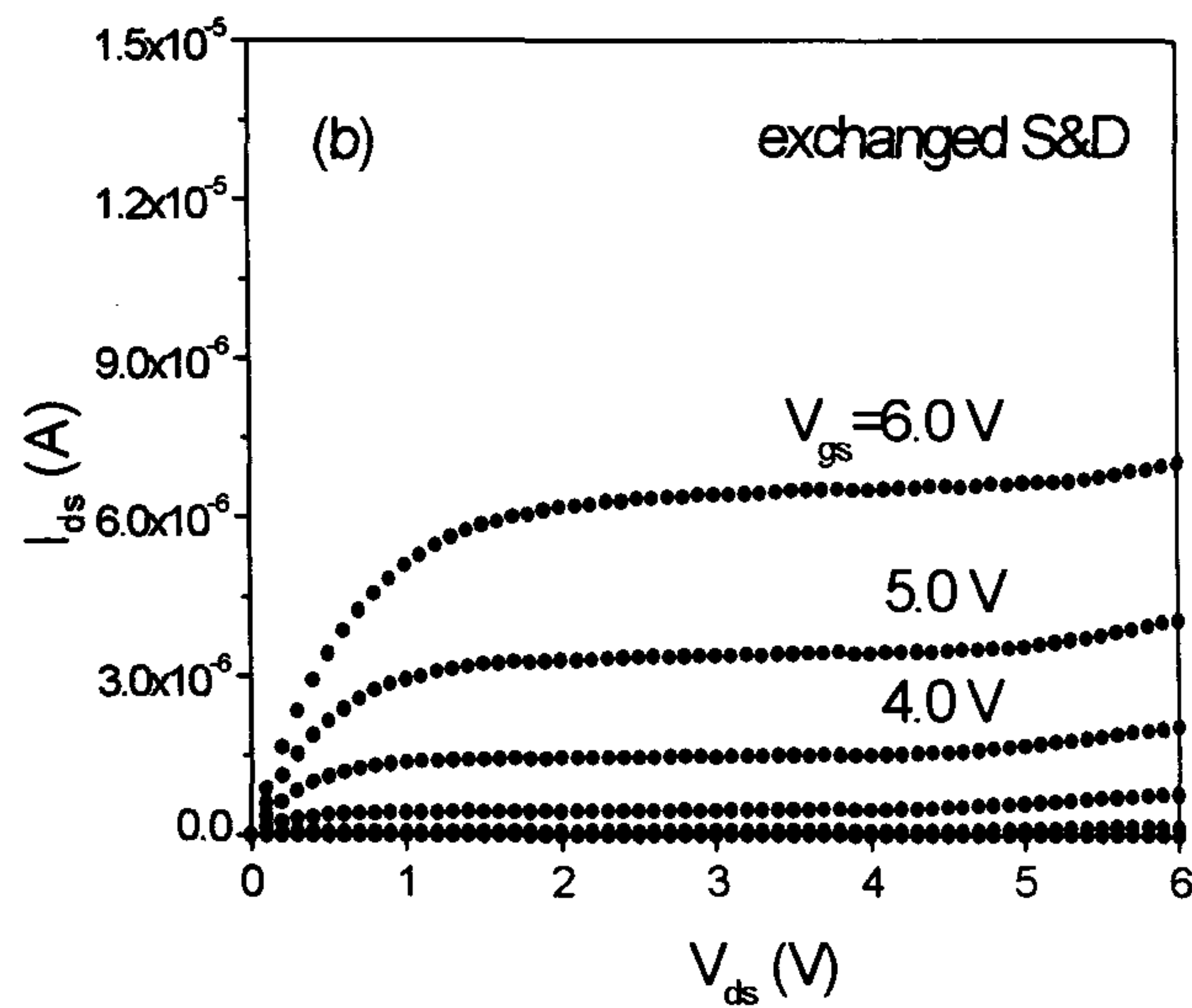


Fig.5 (a) Experimental output characteristics of a SG-TFT (W/L=3.2μm/2.9μm) showing the kink effect. (b) Output characteristics of the same device with source and drain interchanged: no kink effect is present.

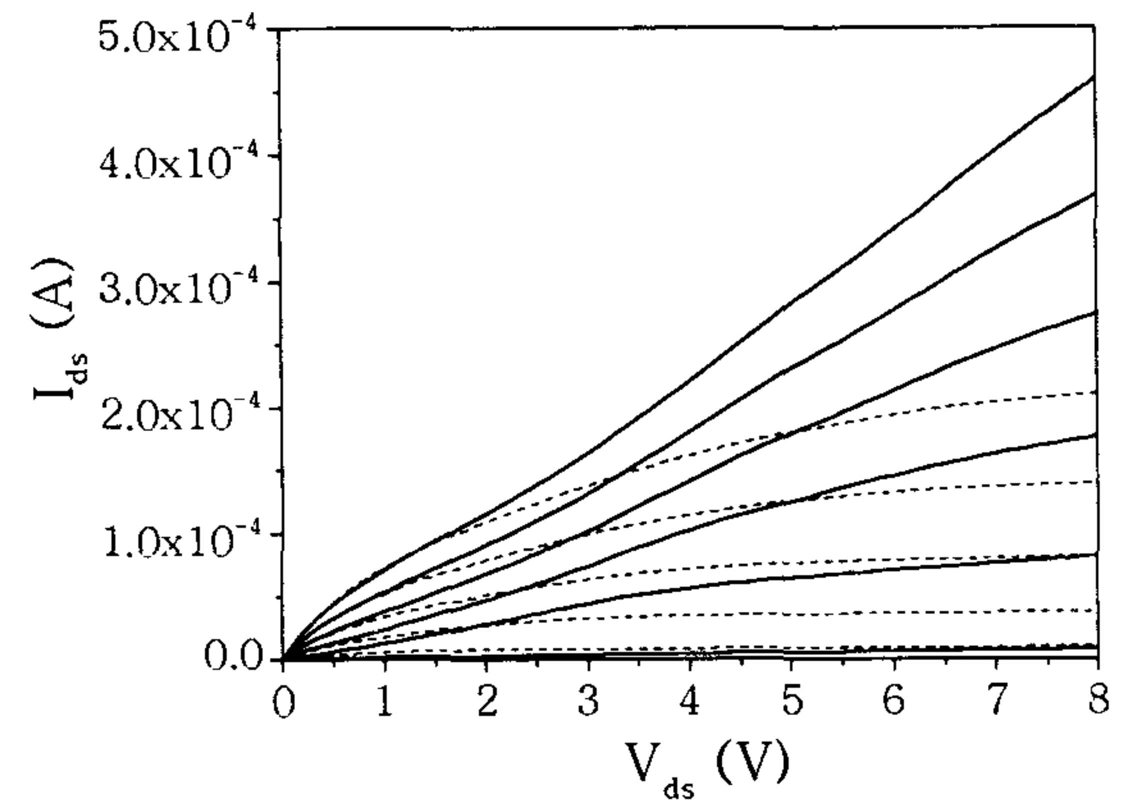


Fig.6 Simulated output characteristics for s a SG-TFTs with a twin boundary near the drain (solid line) or near the source (dash line). From top to bottom, V_{gs} =10V, 8V, 6V, 4V, 2V, and 0V

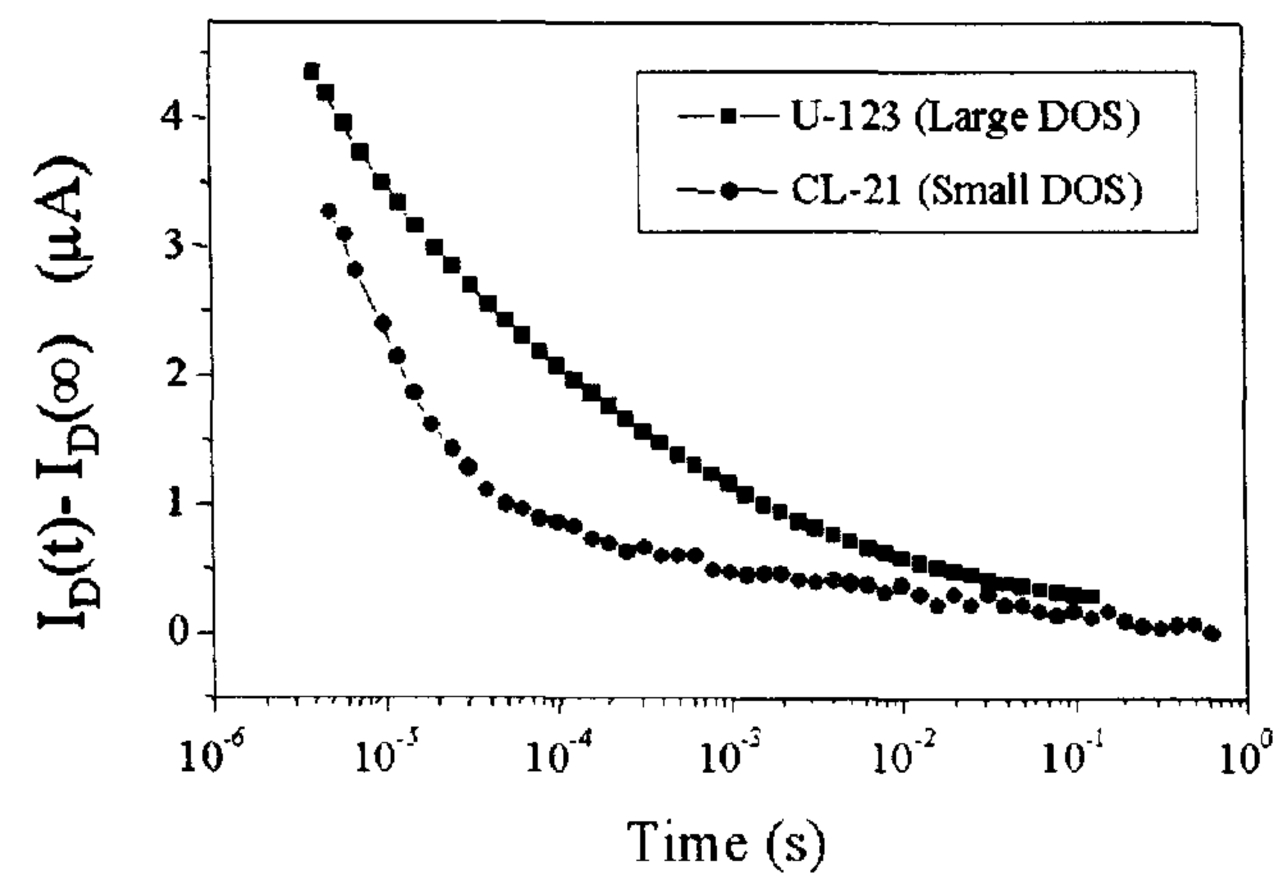


Fig.7 Switch-on Transient for two LTPS TFTs with different trap concentrations. The off time between pulses was 1s.

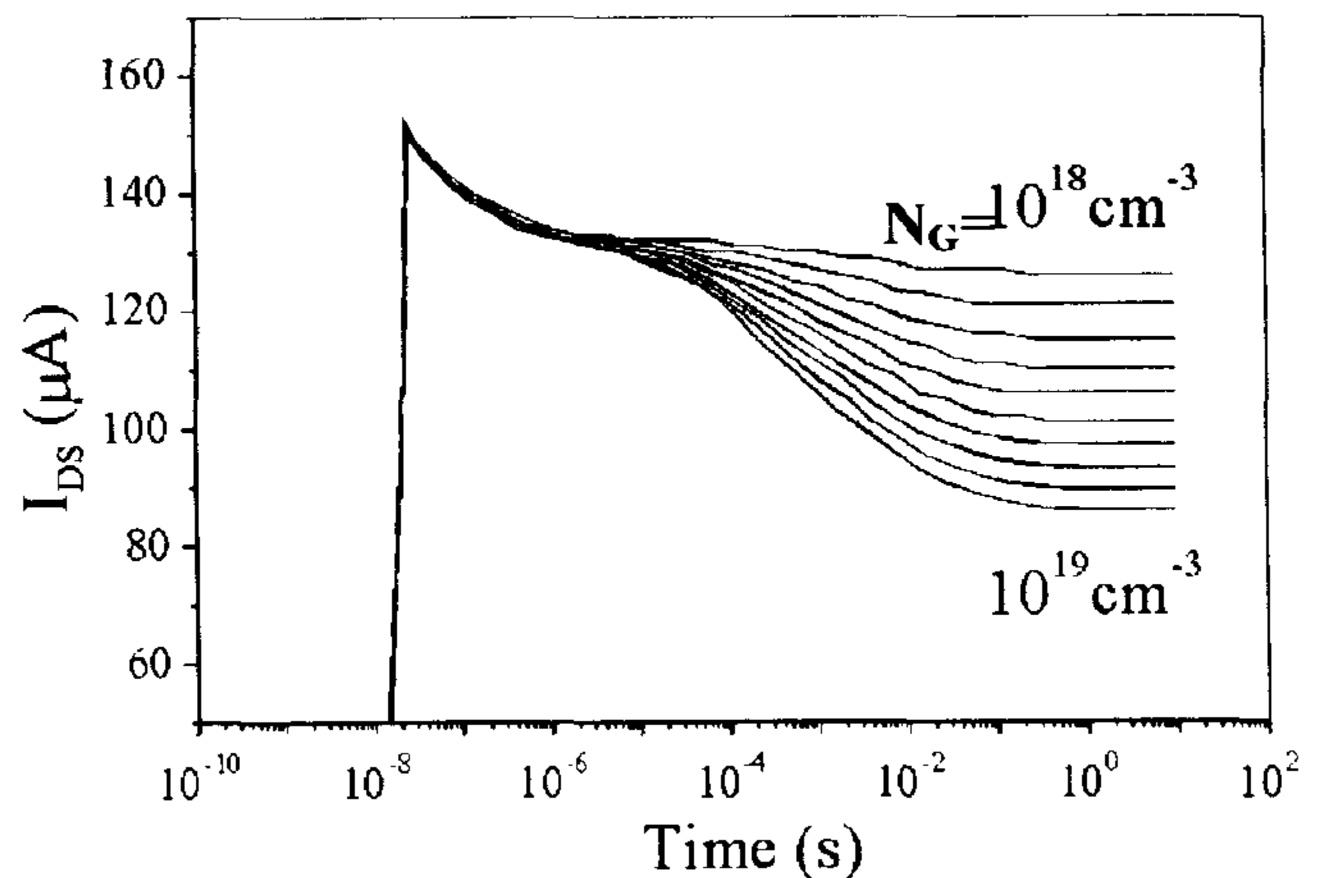


Fig.8 Simulated Switch-on transient for different deep acceptor trap concentrations. $N_{deep}=N_G\exp((E_G-E)/E_0)$; E_0= 0.1eV; σ_n= 10^{-22} cm^2; σ_p=10^{-18} cm^2.

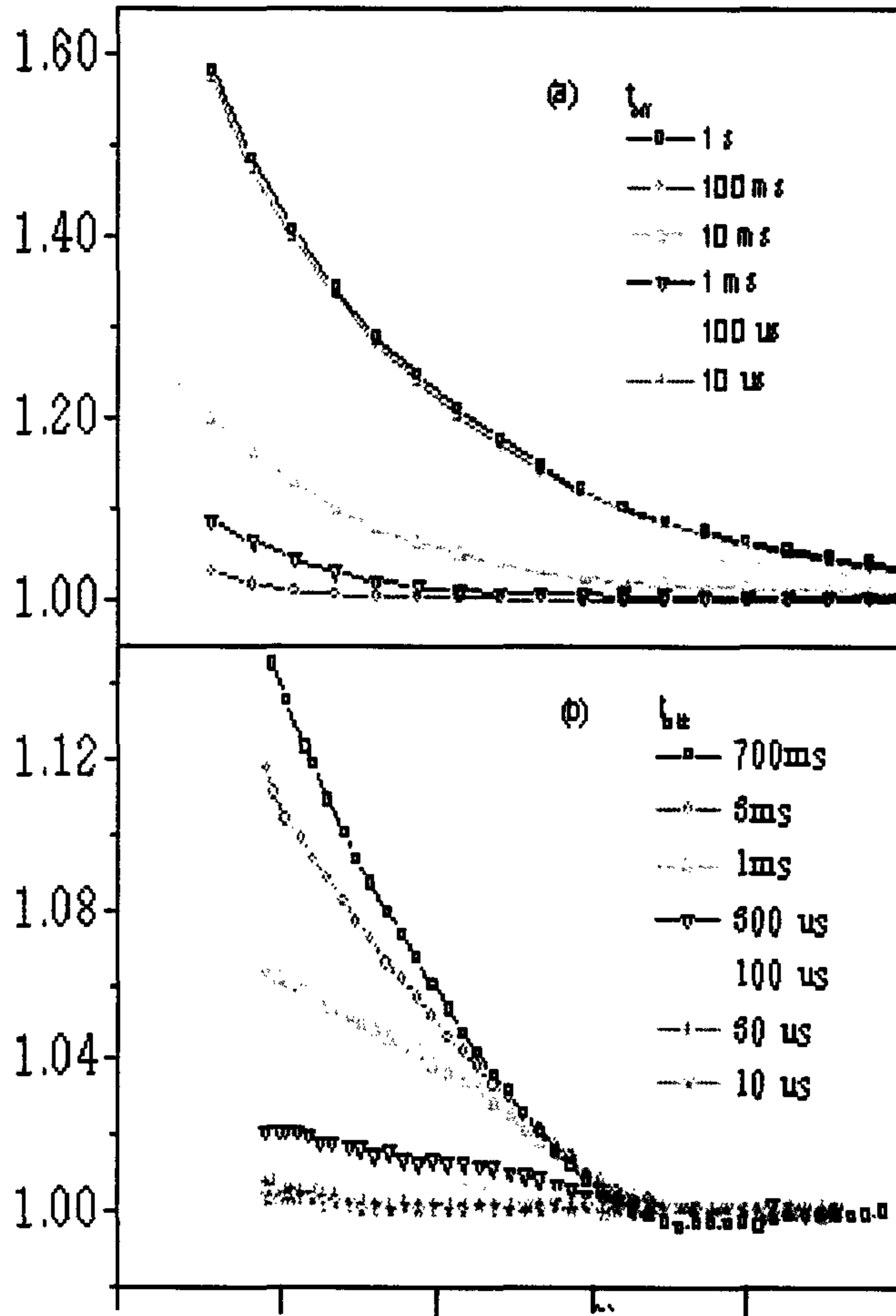


Fig9 Gate switch-on transients for different off-times between pulses. (a) LTPS TFT; (b) SG-TFT

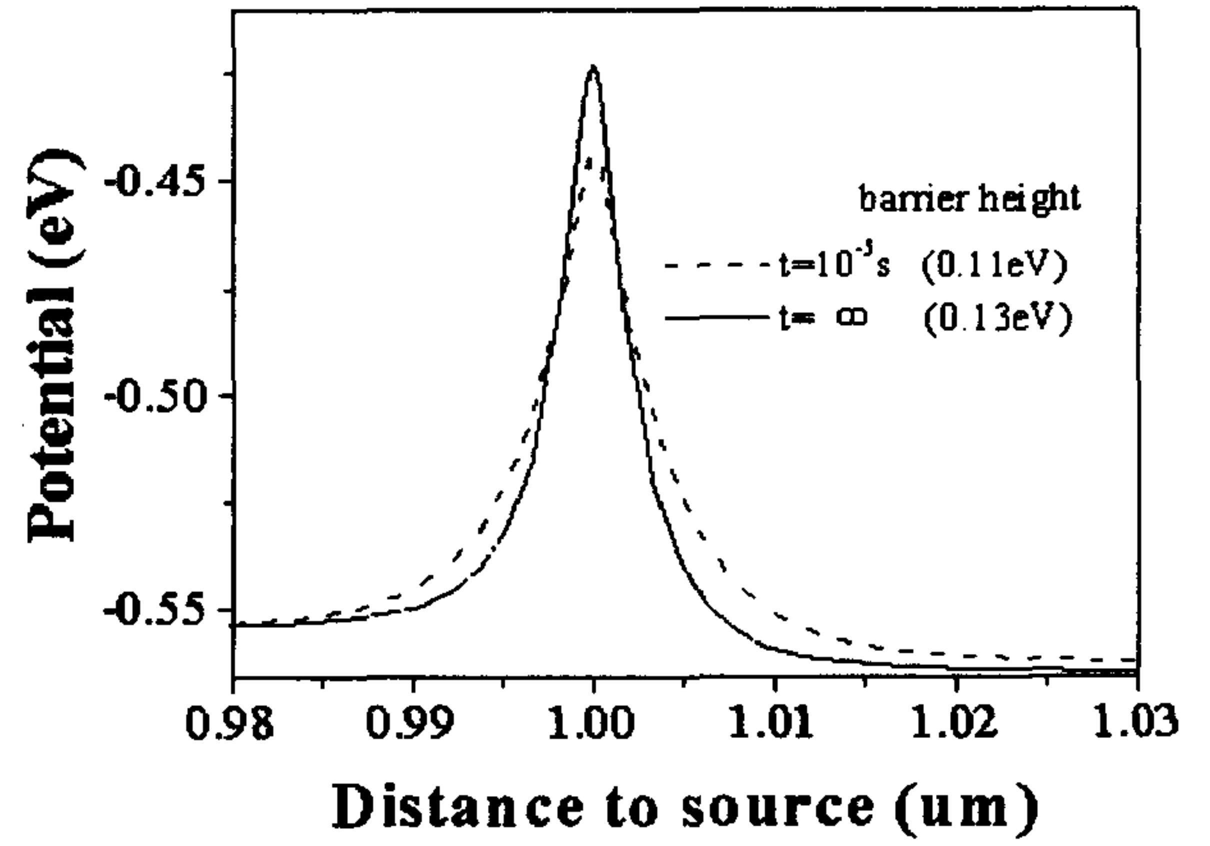


Fig.10 Twin boundary barrier as a function of time, after gate switch on. Dashed curve: $t = 10^{-5}$s ; solid curve: $t=\infty$.

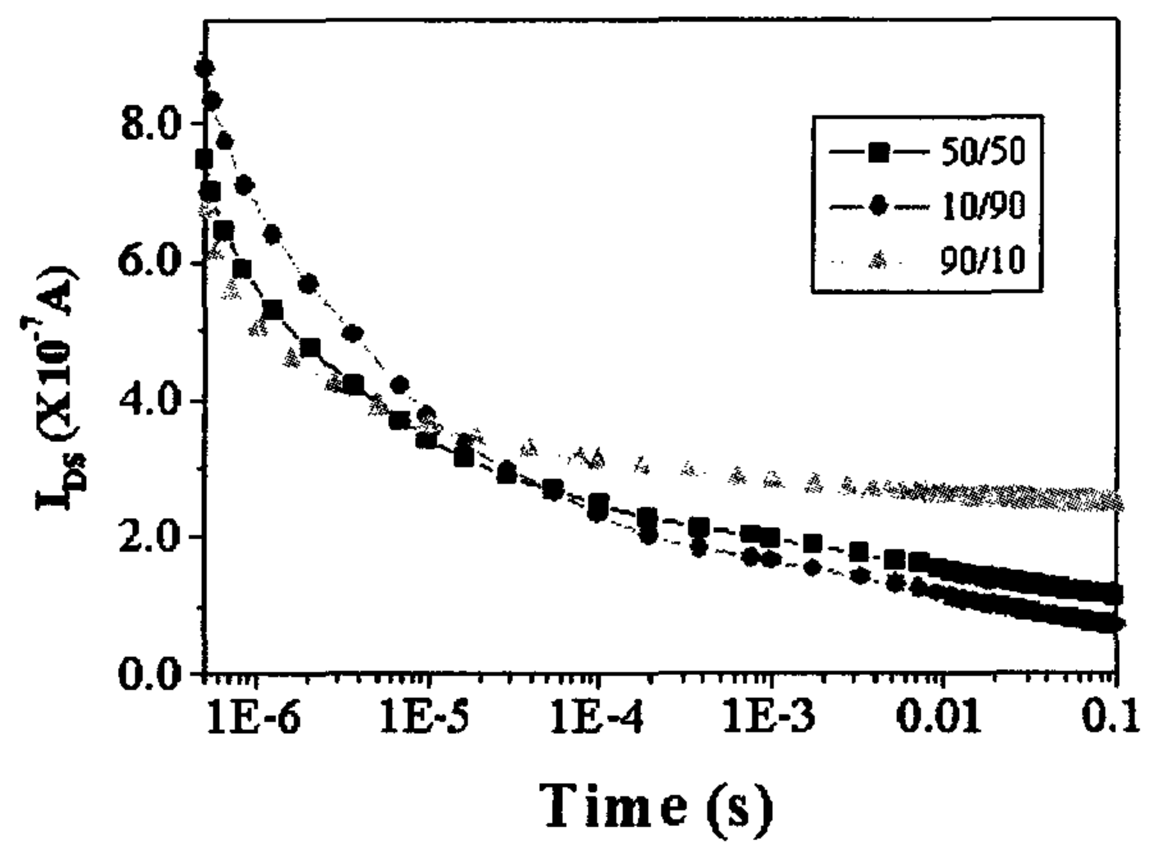


Fig.11 Effect of the time dependence of the twin boundary barrier on the switch-on transient, for different ratios of bulk traps to boundary traps.