21.2: Dual Select Diode AMLCDs: A Path Towards Scalable Two Mask Array Designs

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Abstract

In this paper an alternative Active Matrix LCD technology is described with scalable, low cost processing. The Dual Select Diode AMLCD requires 60% lower capital investment in the array process than a-Si TFT arrays and results in 20% lower cost LCD modules. Development at several AMLCD manufacturers is in progress.

1. Introduction

The TFT LCD has been widely successful as the dominant flat panel display for diagonal sizes ranging from 2 in. to 37 in. TFT arrays for AMLCDs require a semiconductor-type manufacturing process with 4 to 6 photolithography steps and multiple cleaning, deposition, etching and inspection steps. Attempts have been made to reduce the number of mask steps to 2 or 3 [1,2] at the expense of performance and/or yield. For example, the two-mask process proposed Richou et al. [1] used a top gate a-Si TFT and ITO data buslines. Since the a-Si layer in the TFT was exposed to the backlight, this design was susceptible to TFT photoleakage currents and resulting cross-talk. In addition, an extra passivation step was still needed and the narrow, high resistance ITO buslines precluded scale-up to larger size.

In some factories a four-mask a-Si TFT process has been successfully implemented by combining the patterning of the a-Si and the source-drain metal in a single photolithography step. This is done using a special mask [3] that allows for partial, diffractive exposure of the photoresist in the channel region of the a-Si TFT. However, the process needs an additional dry etch step to etch back the photoresist and a unique, difficult to manufacture photomask. Such simplifications can lead to cost reductions, but often also require tighter process control to maintain high yield. A simpler array process with two or three mask steps would be highly desirable.

For large displays in LCD TVs the design rules for patterning the TFT array are approximately the same as for smaller notebook and desktop monitor displays: a resolution of 4 μm and an overlay accuracy of 1 μm. For generation 5 and higher glass substrates this patterning accuracy prescribes the use of very expensive step-and-scan aligners and quartz masks. An alternative array process with relaxed design rules would be advantageous in reducing the cost of lithography.

This brings up the basics of active matrix addressing: The purpose of a pixel switch in an AMLCD is to charge the LC load capacitance accurately to the data voltage during the select time and retain the charge during the non-select period. The fundamental question arises: Is there a more cost-effective method to accomplish this task? This paper provides an affirmative reply to this question. A different pixel circuit will be described which meets the requirements for a simplified process with relaxed, scalable design rules.

2. The Dual Select Diode pixel circuit

In the Dual Select Diode (DSD) AMLCD each pixel consists of a differential circuit with two equal nonlinear resistors or TFDs (Thin Film Diodes). When sufficient voltage is applied across the nonlinear resistors, they conduct and bias the pixel electrode accurately to $(V_{s1}+V_{s2})/2$ (see figure 1). When the voltage across the resistor ladder is subsequently reduced to zero, the diodes no longer conduct and the voltage node between the diodes becomes floating. The data voltage applied to the opposite electrode of the LC capacitor on the color plate (shown as a dotted line in figure 1) is then accurately stored on the pixel.

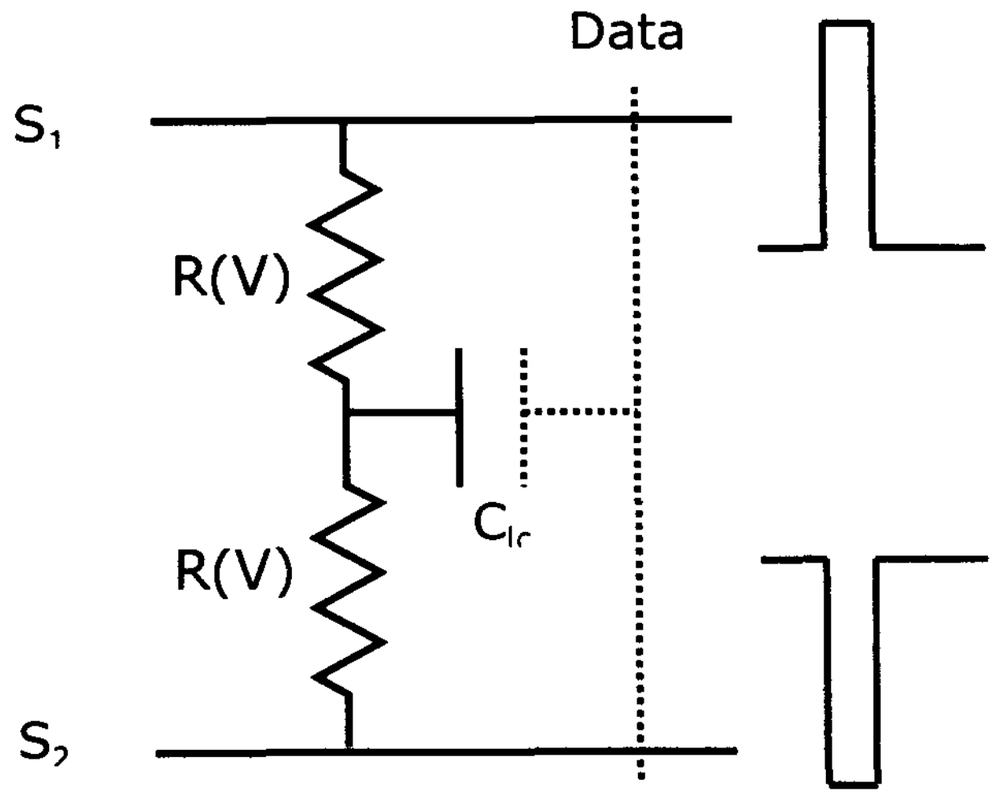


Figure 1. DSD pixel circuit and basic drive waveforms

The DSD pixel circuit gives superior gray scale control as compared to a circuit with a single TFD, since the differential bridge circuit of the resistor ladder cancels out TFD variations across the display area and over time [4,5]. The ON resistance of both TFDs within one pixel can be, for example, 1 Mohm or 3 Mohm, without affecting the gray scale. In both cases the pixel electrode settles at $(V_{s1}+V_{s2})/2$, only the settling time varies. As long as the settling time is less than the select time, accurate gray level performance is obtained. When $V_{s2} = -V_{s1}$ the simplest possible drive scheme is achieved, where the pixel electrode is reset to 0 V each time the line is selected and the data voltage V_d

is stored on the pixel.
The DSD circuit also cancels out RC delays on the buslines and therefore allows scale-up to large display size [4,5].

3. Diode characteristics

Nonlinear resistors or bidirectional thin film diodes have been applied in AMLCDs with single branch diode circuits since 1980. Several semi-insulator materials have been used, including Ta_2O_5, Si-rich SiN_x and Diamond-like Carbon (DLC). The conduction mechanism in the diodes is dominated by Frenkel-Poole field-dependent conductivity:

$$\sigma(E) = \sigma_0 \exp(\alpha\sqrt{E}) \qquad (1)$$

where σ_0 is the zero field conductivity, E is the electric field and α is the nonlinearity parameter:

$$\alpha = \frac{q}{kT}\sqrt{\frac{q}{\pi\varepsilon_0\varepsilon_r}} \qquad (2)$$

ε_{Ta2O5}=24
ε_{SiNx}=9
ε_{DLC}=4

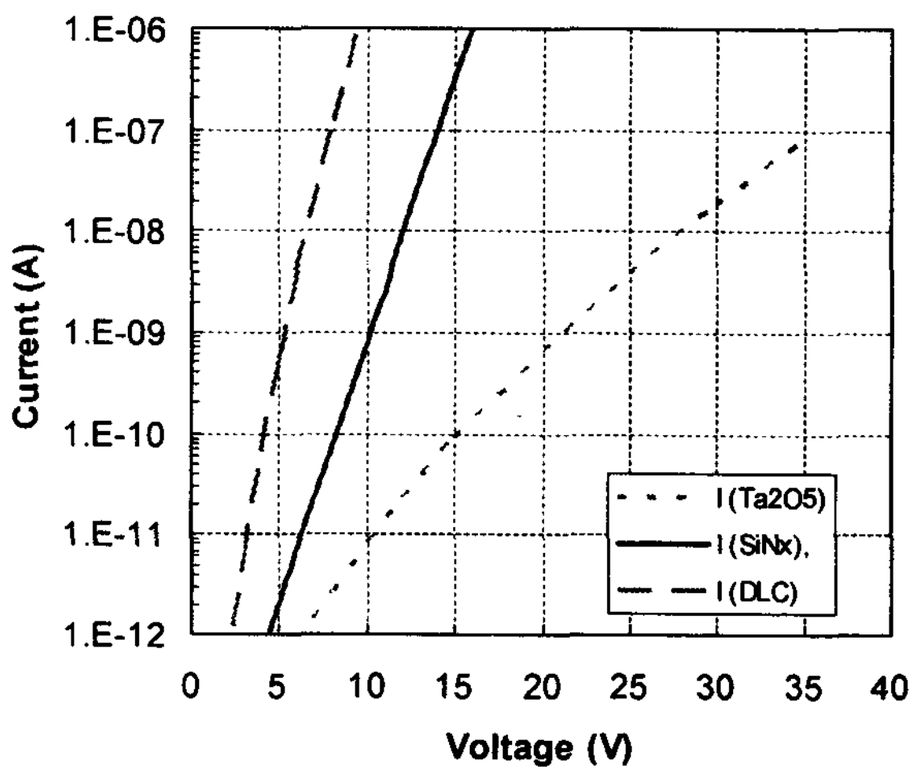


Figure 2. Typical IV characteristics (6,7) for Ta_2O_5, SiN_x and DLC diodes(dielectric constants in insert)

The best diodes are obtained with a semi-insulator with a low dielectric constant ε_r, as follows from equation (2). A low dielectric constant also minimizes the diode capacitance, so that cross-talk is reduced. From this perspective, Diamond-like Carbon appears to be a good candidate for further development. Some initial results have been reported on diodes and LCDs with Diamond-like Carbon [6,7,8].
Ta_2O_5 diodes have been widely used and are obtained by anodizing Ta. Unfortunately, Ta_2O_5 has a high dielectric constant which precludes large, high resolution displays. Si-rich SiN_x has the advantage that it can be processed in standard PECVD equipment found in every a-Si TFT LCD line.

4. Gray Scale Accuracy

Single diode TFD LCDs have previously been reported with 6 bit and 8 bit gray scale accuracy using a 5-level row drive [9]. These displays, however, required close to 1% uniformity in the SiN_x thickness. They also were susceptible to image retention and could not be scaled to diagonal sizes larger than about 12 in. due to RC delays on the select (row) lines. The DSD circuit solves these problems. In the DSD pixel circuit the two TFDs within one pixel need to have similar or close to similar IV characteristics. It is easy to calculate the pixel voltage error, if the two TFDs are not exactly equal, i.e. in the case of imbalance in the circuit.
Si-rich SiN_x diodes often follow more closely exponential IV curves [5], rather than the Frenkel-Poole curves of equation (1):

$$I = I_0\left[\exp\left(\frac{V}{V_c}\right) - \exp\left(\frac{-V}{V_c}\right)\right] \qquad (3)$$

where I_0 is the current pre-factor and V_c=0.875 V' at room temperature for optimized diodes. In most DSD drive schemes only one polarity of the curve is used. If the current in one branch of the DSD circuit is different from the other, the two diode equations are:

$$I_1 = I_0\exp\left(\frac{V_1}{V_c}\right) \quad \text{and} \quad I_2 = (I_0 + \Delta I_0)\exp\left(\frac{V_2}{V_c}\right) \qquad (4)$$

After full charging of the LC pixel capacitance the currents I_1 in the first TFD and I_2 in the second TFD are equal.
Therefore the voltage across the diodes differs by:

$$V_1 - V_2 = V_c \ln\left(\frac{I_0 + \Delta I_0}{I_0}\right) \qquad (5)$$

The resulting DC offset on the LC pixel voltage (the DC error) is:

$$\Delta V_{DC} = 0.5(V_1 - V_2) = 0.437\ln\left(1 + \frac{\Delta I_0}{I_0}\right) \qquad (6)$$

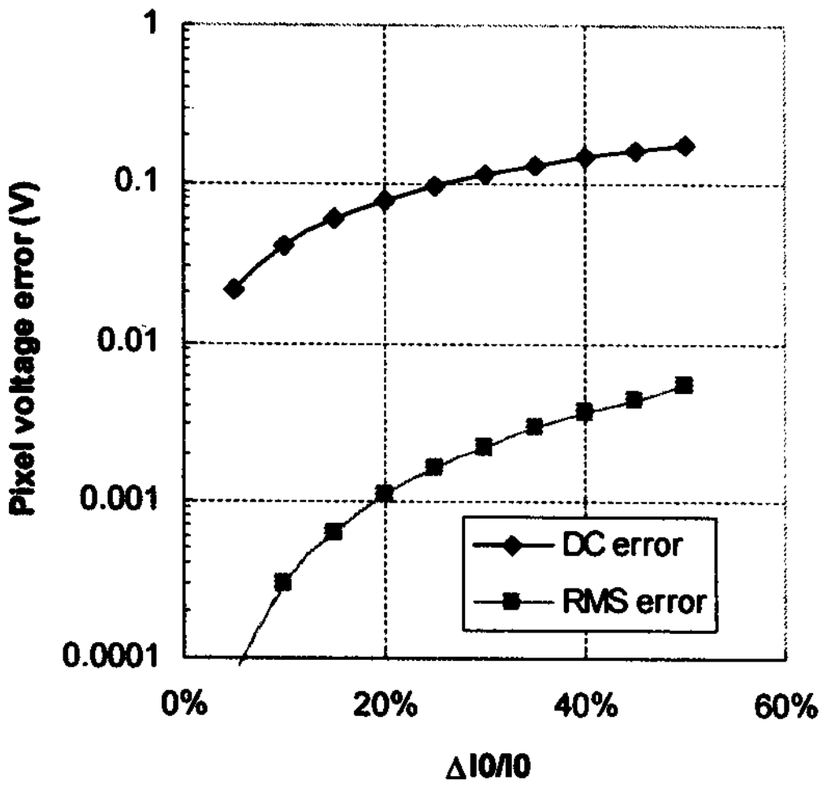


Figure 3. Dependence of DC and RMS error in LC voltage on % difference in diode currents of DSD circuit for V_{LC} = 3 V.

The difference in the RMS voltage, which determines the gray scale error is much smaller:

$$\Delta V_{RMS} = 0.5 \frac{\Delta V_{DC}{}^2}{V_{LC}} \qquad (7)$$

In figure 3 the DC and RMS errors are plotted. To prevent image retention the DC error needs to be smaller than 50 to 100 mV. To prevent gray scale errors the RMS error needs to be smaller than about 5 mV. This translates into a maximum acceptable variation of 25% in the current between the two diodes in the same pixel, when V_c=0.875 V. This is expected to be easily achieved in production. Long range variations in the diode current across the viewing area can exceed a factor of three or more in the DSD circuit without affecting gray scale uniformity [4].

5. Drive methods

The basic drive scheme shown in figure 1 leads to some vertical cross-talk. To improve charge retention on the pixels and eliminate vertical cross-talk a further improved DSD drive scheme was introduced, which adds an offset or holding voltage V_h to both select voltages and non-select voltages [10,11]. The polarity of the holding voltage changes every row and every frame (figure 4). The pixel electrode voltage then settles at V_h or - V_h during the select time and the voltage across the LC charges to $V_{data} \pm V_h$. This so-called offset-scan-and-hold drive method requires a custom row select driver IC and a low voltage line inversion data driver. The line inversion drive can be achieved with a data driver IC with a single 5 V or 3.3 V supply voltage.

Driver ICs for DSD AMLCDs with the offset-scan-and-hold drive method have recently been developed [12,13]. They include a row driver with 256 channels and a line inversion data driver with 384 channels

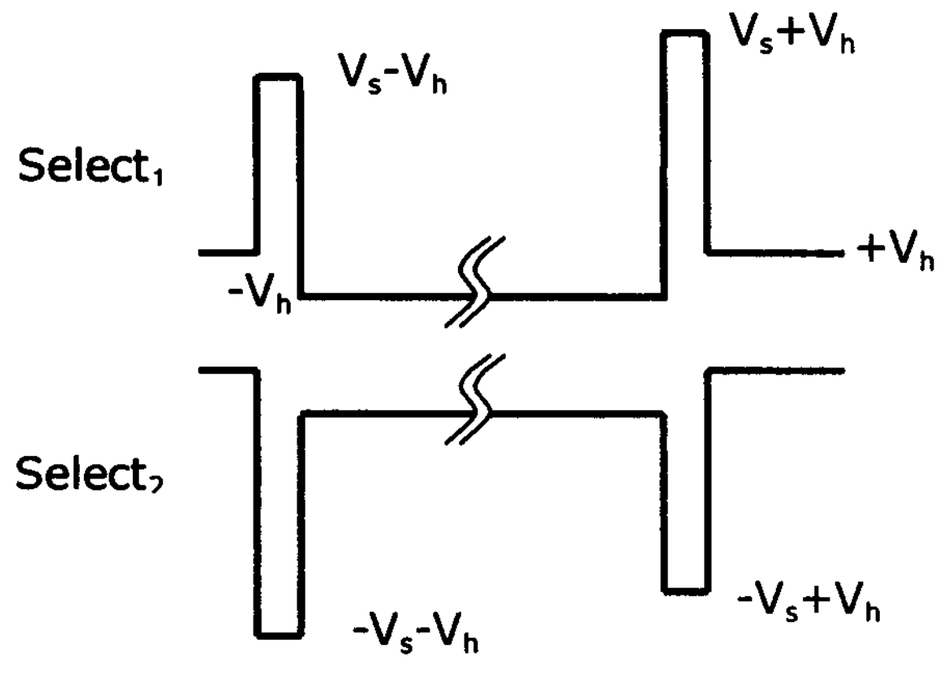


Figure 4. Offset-scan-an-hold drive waveforms on two select lines of one row

6. Two and three mask array processes

TFD LCDs with Ta_2O_5 or SiN_x diodes can be manufactured with only two photomask steps [14,15]. In the simplest process with SiN_x diodes (figure 5) the ITO layer is patterned first as the pixel electrode and bottom electrode for the diode. Then, the Si-rich SiN_x film is deposited with a thickness of around 100 nm in standard PECVD equipment. Deposition time is only 40 seconds. Film thickness and the ratio of Si to N in the film determine the diode current-voltage characteristic. Then, the top metal is deposited and patterned as the select line metal and the top electrode for the diode. The SiN_x film can be patterned during the same mask step as the select line. In the three-mask process the Si-rich SiN_x layer is patterned separately.

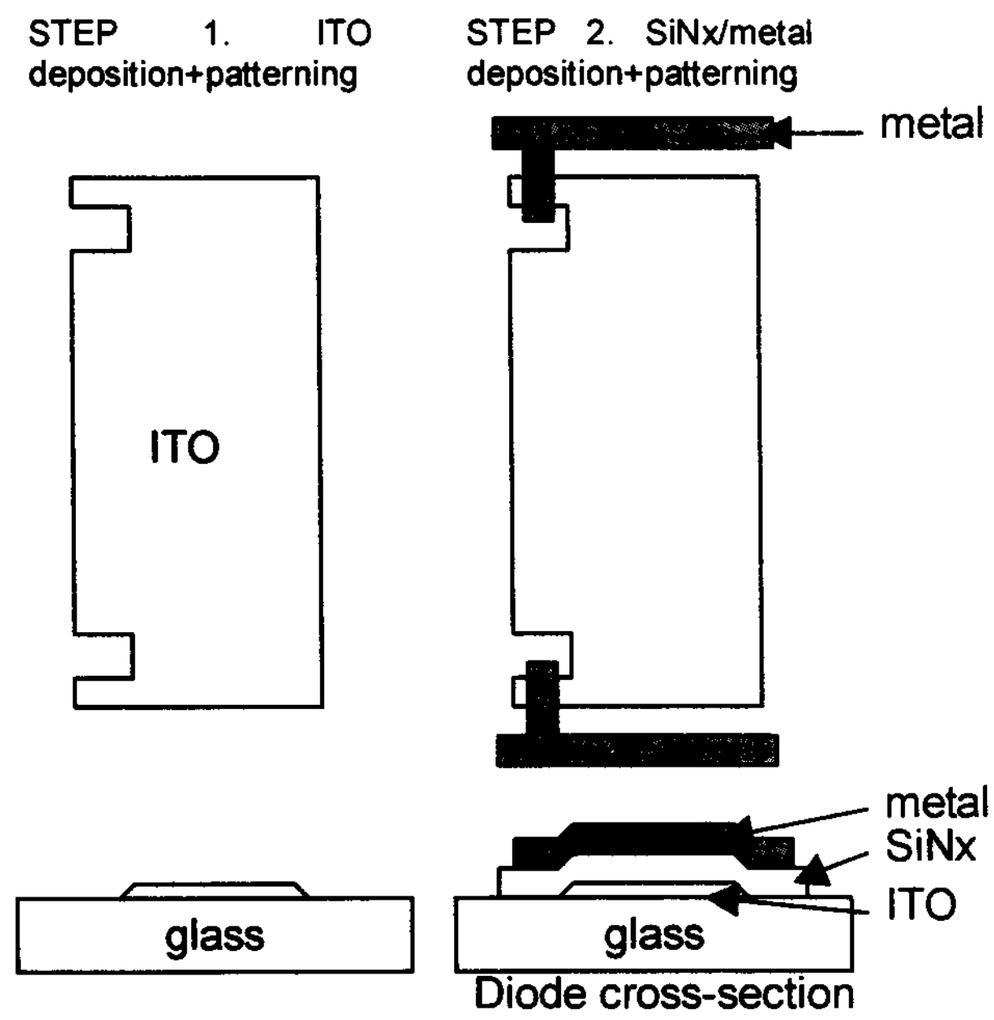
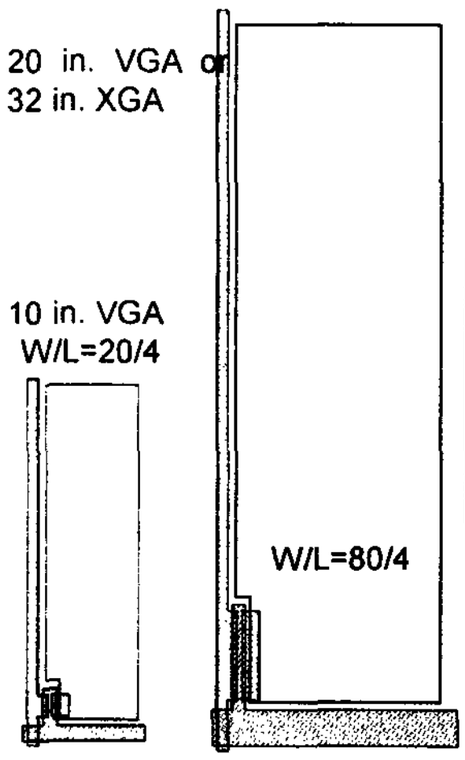


Figure 5. Two mask process for DSD active matrix

A passivation layer is generally not required in diode LCDs [14,15], since the top electrode of the diode protects the diode. On the opposite color plate the ITO is patterned into stripes to function as the data buslines.
The manufacture of DSD AMLCDs requires 60% less capital investment for the array process than TFT LCDs [16]. The overall module cost of a DSD AMLCD panel was calculated to be at least 20% less than for a-Si TFT panels [16].

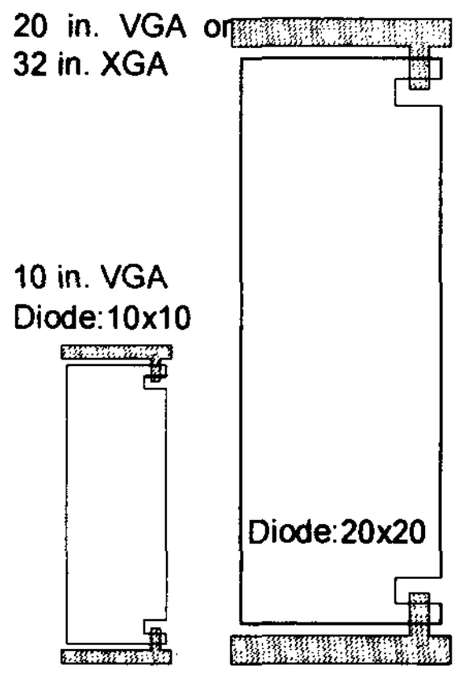
7. Design rules

The patterning of large AMLCDs requires expensive step-and-scan exposure equipment and complex large quartz masks. In order to maintain sufficiently low gate-source capacitance, the design rules for patterning 10 in. and 30 in. TFT LCDs are about the same (figure 6). Patter-to-pattern overlay accuracy is 1 μm and minimum feature size is 4 μm.
In DSD LCDs, on the other hand, the design rules are already relaxed for 10 in. displays and they scale with pixel size. This is the result of the vertical current flow in the diodes. When the pixel pitch doubles, the LC load capacitance quadruples and the side dimensions of the diodes double (figure 7). The overlay accuracy can also be further relaxed from 3 to 6 μm.



TFT array	Resolution	Overlay
10 in VGA	4 μm	1 μm
32 in XGA	4 μm	1 μm

Figure 6. Non-scaling design rules in TFT array



DSD array	Resolution	Overlay
10 in VGA	10 μm	3 μm
32 in XGA	20 μm	6 μm

Figure 7. Scaling design rules in DSD array

Relaxed design rules allow the use of much lower cost exposure equipment, such as proximity printers normally used for color filter patterning.
Another advantage of relaxed design rules is the easy production of LCDs on plastic substrates. A single SiN_x diode LCD manufactured with a low temperature process on PES plastic substrates was reported recently [17].

8. Compatibility with LCD TV

To be considered for application in LCD TVs, a new AMLCD technology must be scalable to large area, compatible with wide viewing angle technologies, compatible with overdrive methods to improve response time and have a lower manufacturing cost than existing TFT LCD technology. It is believed that DSD AMLCDs satisfy all these requirements. SPICE simulations of a 40 in. DSD W-XGA AMLCD indicate that uniform gray scale performance is possible with V_c=0.875 V, row busline resistance of less than 1.3 kohm and column busline resistance of less than 20 kohm (see figure 8).

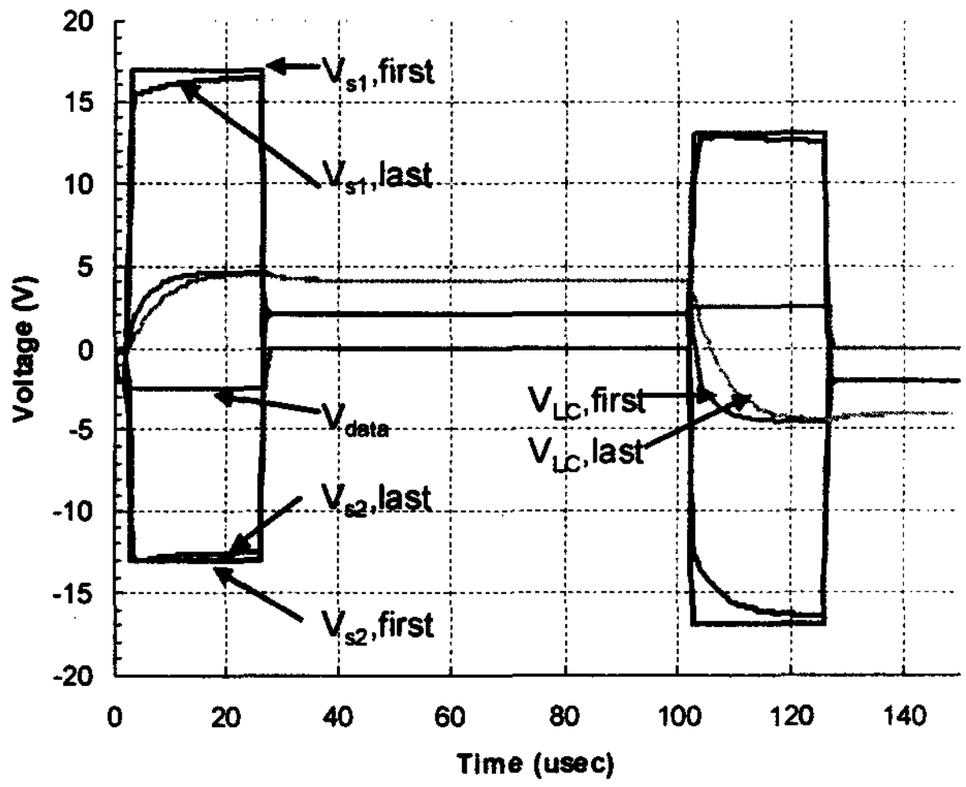


Figure 8. SPICE simulation of pixel charging in 40 in. W-XGA DSD AMLCD. Select voltages on S1 and S2 and LC voltage at first and last pixel on row are shown

DSD technology is compatible with several wide viewing angle technologies, including MVA (Multi-domain Vertical Alignment) and PVA (Patterned Vertical Alignment). In PVA LCDs [18] the ITO on the color plate is already patterned, so that no extra processing would be required to pattern the ITO data buslines on the color plate in DSD AMLCDs. There is less compatibility with IPS (In Plane Switching), since DSD AMLCDs have row and column buslines on opposite substrates.

Improvements in response time to achieve video performance in LCD TVs are directly applicable to DSD LCDs. The same type of overdrive waveforms applied to the data voltages in TFT LCDs can also be implemented in DSD LCDs.

9. Challenges

Since TFD LCD technology is not mainstream, some challenges remain to achieve commercial success.

The manufacturing yield is difficult to predict, until volume production provides statistical data. Simple processes, however, generally lead to a higher yield. The relatively low breakdown voltage of SiN_x diodes will require the use of ESD protection circuits and possibly also redundant pixel designs.

In the two-mask DSD LCD process the data lines are ITO stripes on the color plate. They need to have sufficiently low resistance to keep the RC delay on the dataline acceptable. ITO sheet resistance on TFT color plates is typically around 35 ohms/square. For 20 in. and larger DSD LCDs the sheet resistance of the ITO needs to be 20 ohms/square or less, which can be achieved by an increase in the ITO thickness. Alternatively, a metal trace can be added to the ITO data line to reduce resistance.

Another challenge is the optimization of the SiN_x diode to obtain display lifetimes of 50,000 hours required for LCD TVs. Single TFD LCDs with Si-rich SiN_x diodes have been reported with an 8 bit gray scale and lifetime of more than 10,000 hours [19,20,21]. Since the DSD pixel circuit cancels out most of the diode degradation, the lifetime of DSD LCDs is expected to exceed this lifetime significantly.

10. Status

Prototype color DSD AMLCDs with 10.4 in. diagonal size and VGA resolution were developed in 1998 with a three mask array process [5,11]. Figure 9 shows an image on the prototype. In the prototype a basic drive scheme (as shown in figure 1) without holding voltage was used. This drive method resulted in some vertical cross-talk. The offset-scan-and-hold drive method will eliminate or minimize this cross-talk [10,11].

Figure 9. Image on 10 in. color VGA DSD AMLCD

Several AMLCD manufacturers are currently developing DSD LCDs with sizes in the 10 to 20 in. range.

11. Summary

An alternative AMLCD technology has been described with a 20% lower module production cost and easier scalability to larger sizes than TFT LCDs. The DSD AMLCD can be applied in displays ranging from cell phones to large area TVs. When based on Si-rich SiN_x diodes, they can be manufactured in existing AMLCD factories using less than 40% of the array equipment or in passive matrix LCD plants with some additional equipment. Some Gen 2 to Gen 3.5 fabs, which are no longer productive for notebook and larger panels, are good candidates for initial DSD LCD production. Alternative insulator materials for the diodes, including Diamond-like Carbon, hold great promise. For cell phone applications a low power 3.3 V data driver can be used. This, combined with a possible aperture ratio in excess of 70% and an RGBW quad color filter arrangement, can lead to ultra-low power and low cost portable AMLCDs.

6. Acknowledgements

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