# A New DAC Employing Source-follower type Analog Buffer with P-type Poly-Si TFTs in Active-Matrix Displays

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## Abstract

*We propose and simulate a new integrated DAC analog buffer composed of only p-type poly-Si TFTs in AMLCD and AMOLED. Proposed circuit employs a voltage level shifter which $V_{OUT}$ has a linear functional relation to $V_{IN}$. The proposed scheme enables to allow a constant $V_{GS}$ of buffer transistor so that the charging speed of pixel data address is improved.*

## 1. Introduction

Low temperature poly-Si (LTPS) is widely used as a pixel and peripheral circuit in AMLCD and AMOLED due to high mobility and large on-current [1]. Recently, the integration of pixel elements and peripheral driver has attracted a considerable attention for reducing the external driving circuitry and fabrication cost. For the panel integration, the building blocks such as shift-register, level shifter, latch, DAC should be designed for row and column driver.

One of the most important circuits is analog buffer which charges a pixel data voltage through coulmn line. Various researches such as CMOS op-amp [2], $V_{TH}$ cancelling [3], double-offset cancelling [4] and Vth cancelling with bootstrapping [5] have been reported in order to improve charging accuracy, time, and power consumption. However, large area consuming [2], additional storage capacitors [3][4] and many control signals [4], low charging speed of $V_{TH}$ cancelling type [3][5] may be still problems.

The purpose of our work is to design a p-type poly-Si analog buffer for DAC integrated in the panel. The proposed buffer employs a voltage level shifter which improves charging speed of pixel data address by allowing a constant charging capability of buffer transistor. Also, a new two-transistor circuit employing asymmetric active layer width is proposed for enhancing the charging accuracy. We successfully verified the circuit operation by SmartSPICE simulation.

## 2. The Proposed Circuit

### 2. 1. Scheme of Improving Charging Speed

As shown in Figure 1, source-follower type buffer employing $V_{TH}$ cancelling [3] has a problem of low charging speed because the charging speed decreases as the charging is to be finished. We have already proposed an improved analog buffer employing $V_{TH}$ cancelling without any $V_{TH}$ storage capacitor [5]. It reduces the charging time by employing a boot-strapping, however, the low charging speed is still to be solved. In the $V_{TH}$ cancellation type source-follower, $V_{GS}$ of buffer transistor is decreased to $V_{TH}$ value so that the output voltage is slowly charged up to input voltage value.

We employ a new source-follower type analog buffer of which the scheme does not employ $V_{TH}$ cancellation. In the proposed circuit, the output voltages are linearly functional to the input voltages. Figure 2 shows a proposed scheme and a voltage level shifter which is composed of two p-type poly-Si TFTs. When T1 and T2 operate in saturation, the current equation when the charging is finishied is obtained as follows:

$$I = (k_1/2)(W/L)(V_{BIAS}-V_{DD}-V_{TH1})^2$$
$$= (k_2/2)(W/L)(V_{IN} - V_{OUT} - V_{TH2})^2 \quad \cdots\cdots\cdots(1)$$

(where $k = \mu$ Cox, W: width, L: length, $\mu$: mobility)

Here, when the conventional line beam of XeCl excimer laser crystallization is scanned, the mobility and threshold voltage of T1 and T2 are assumed to be same ($V_{TH1} = V_{TH2}$) [6].

$$V_{BIAS} - V_{DD} = V_{IN} - V_{OUT} \quad \cdots\cdots\cdots(2a)$$
$$\therefore V_{OUT} = V_{IN} + (V_{DD} - V_{BIAS}) \quad \cdots\cdots\cdots(3a)$$

Therefore the output voltage ($V_{OUT}$) is not the same with input voltage ($V_{IN}$) but has a functional relation to $V_{IN}$. Since $V_{GS}$ ($=V_{BIAS}-V_{DD}$) larger than $V_{TH}$ is assured even when the charging is finished, the fast charging would be obtained.

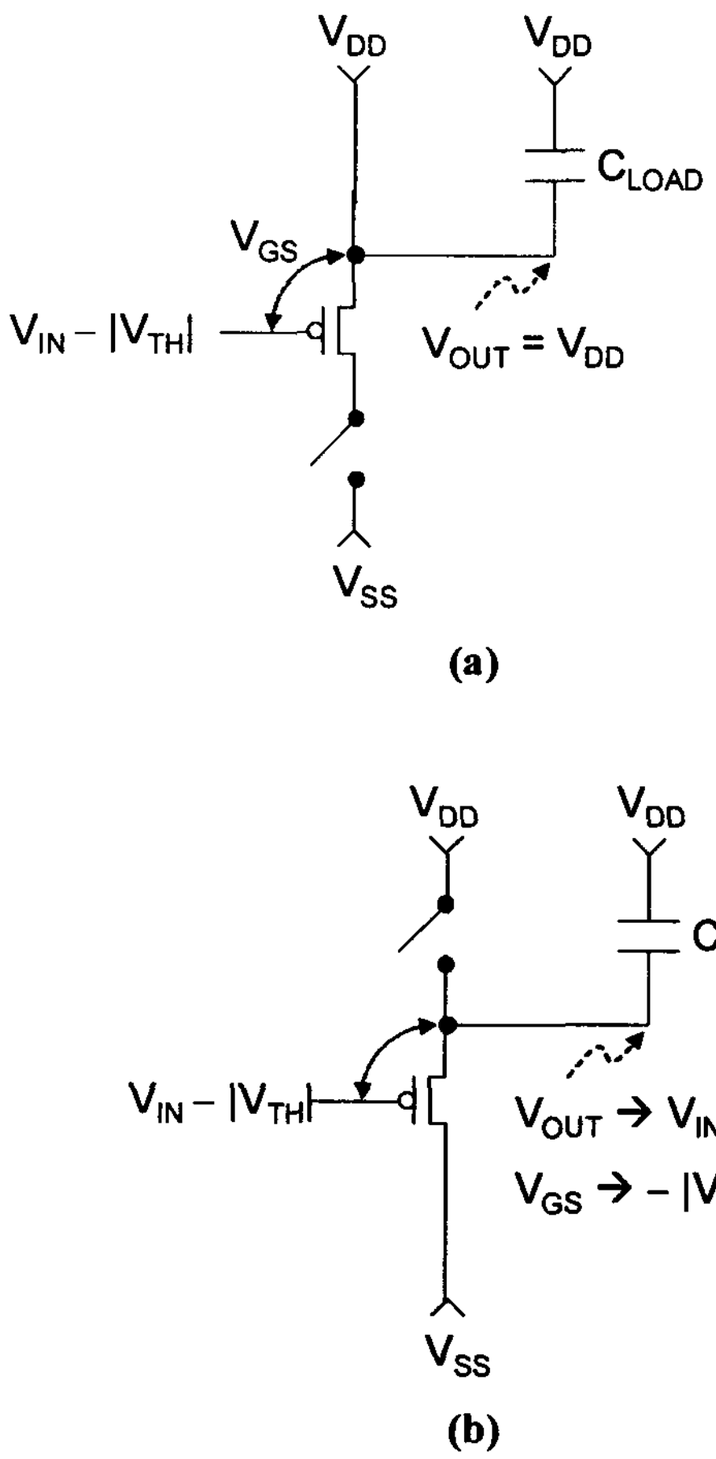



**Figure 1.** The driving operation of the conventional source-follower type analog buffer. (a) precharge step for $V_{OUT}$ $=V_{DD}$ , (b) output voltage buffering step in which $V_{OUT}$ reaches $V_{IN}$. The charging speed decreases as $V_{OUT}$ goes to $V_{IN}$.

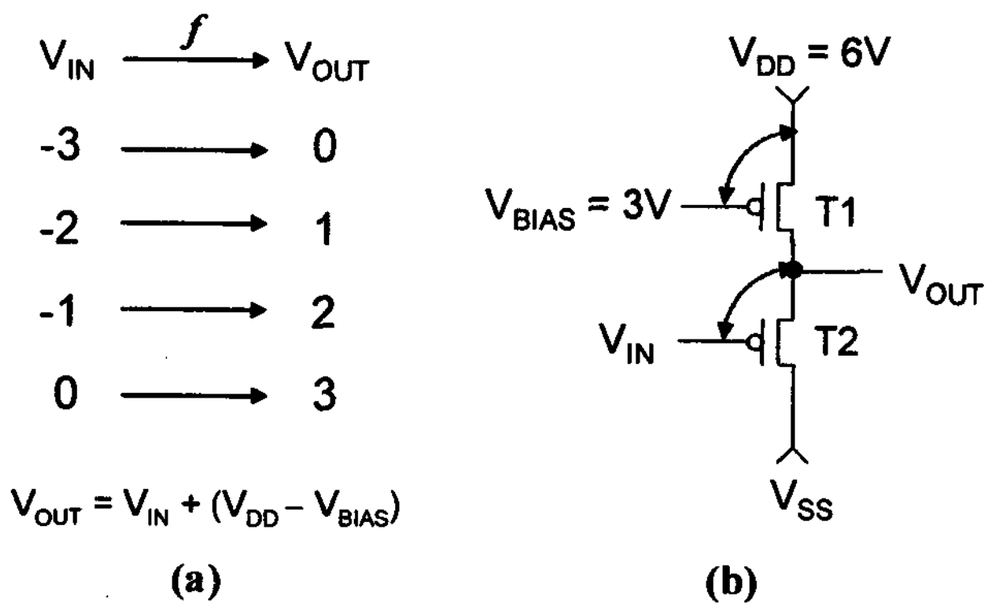



**Figure 2.** (a) The proposed driving scheme of analog buffer (b) A voltage level shifter of which the circuit does not employ $V_{TH}$ cancellation scheme (Type I). $V_{OUT}$ has a linearly functional relation to $V_{IN}$.

## 2. 2. Scheme of Accuracy Improvement

The accuracy of proposed analog buffer depends on the voltage level shifter (Figure 2). T1 and T2 turn on in saturation regime, however, T1 would turn on in linear operation when $V_{OUT}$ is higher than $V_{BIAS}$. In order to prevent the undesirable linear operation of T1, the feed-back type voltage level shifter is preferable as shown in Figure 3. The gate and drain node are connected so that T1 operates in saturation regime as a rule. It is noted that it does not require an additional $V_{BIAS}$ voltage source. In the proposed feed-back type, the functionality of input and output voltage is as follows:

$$V_{OUT} - V_{DD} = V_{IN} - V_{OUT} \quad \cdots\cdots\cdots(2b)$$

$$\therefore V_{OUT} = (V_{IN} + V_{DD}) / 2 \quad \cdots\cdots\cdots(3b)$$

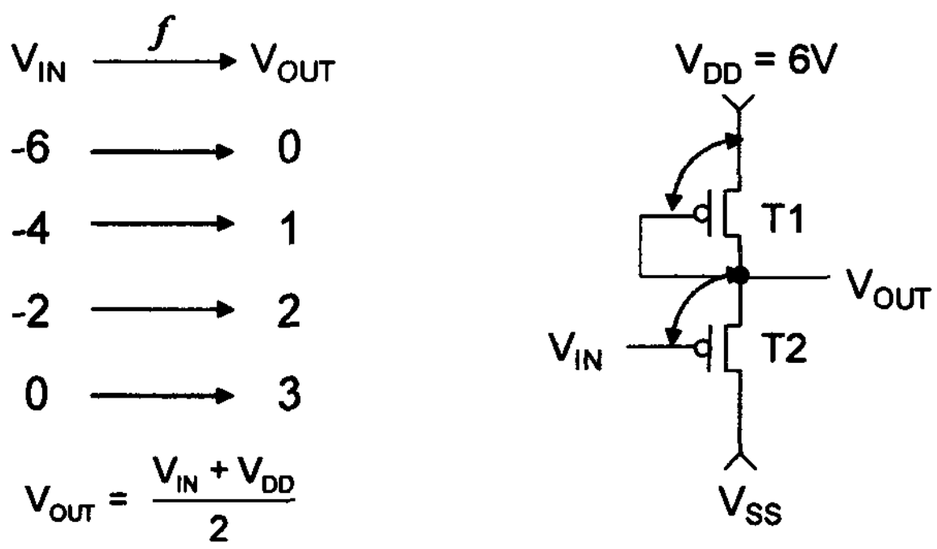
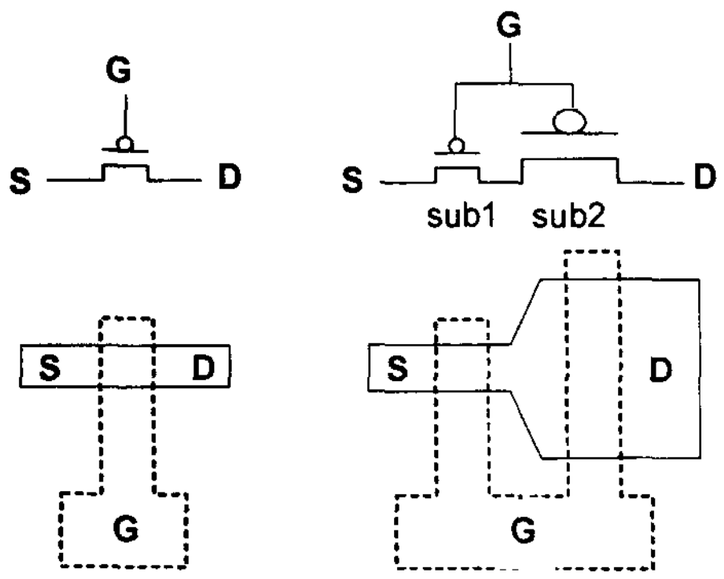
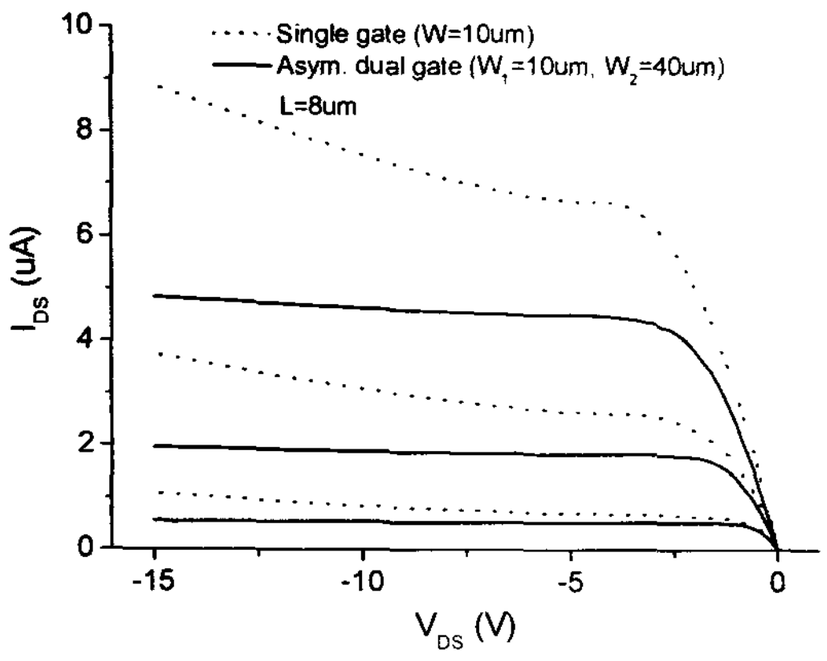



**Figure 3.** (a) The proposed driving scheme of analog buffer (b) Feed-back type voltage level shifter (Type II). T1 would always operate in the saturation regime.

The output resistance ($r_o$) of transistor determines the saturation characteristics. Figure 4b shows the output curve of the fabricated conventional single gate p-type poly-Si TFT. Drain current ($I_{DS}$) increases slightly as $V_{DS}$ increases because $r_o$ is not sufficiently large. Then the eq. (2) could not be solved from eq. (1). It is noted that low $r_o$ enlarges the offset deviation of $V_{OUT}$.

In dual gate structure, asymmetric dual gate is effective to increase $r_o$ in SOI [7] and poly-Si devices [8][9]. In this paper, we propose a new circuit-based structure employing asymmetric channel width in order to improve the output impedence for a good saturation current (Figure 4a). The p+ doped floating region between the dual gate acts as a sub-source and sub-drain electrode, thus two different TFTs (narrow-width subTFT1 and wide-width subTFT2) seems to be connected in series.




**(a)**

**(b)**

Figure 4. (a) The proposed structure of dual gate poly-Si TFT with asymmetric channel widths (Type III). (b) The comparison of output characteristics. The proposed device exhibits a large $r_o$. Dotted line is measurement result and solid line is SPICE simulation result.

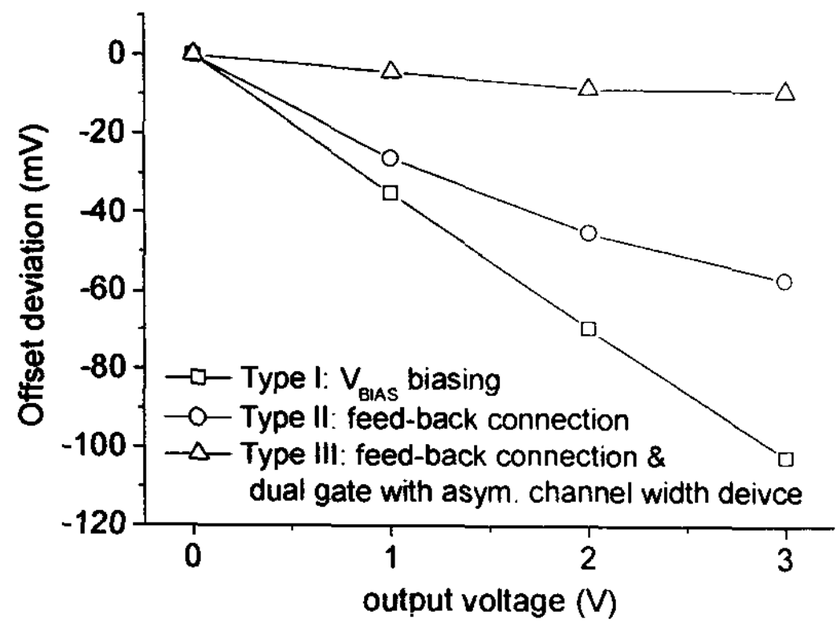



**Figure 5.** The offset deviation comparison of the proposed voltage level shifters.

The reason of the enlarged output impedance in the proposed circuit is as follows. When $V_{DS}$ increases in the saturation, the floated node also increases and the current increases because the actual poly-Si TFTs have rather low channel resistances. The conventional dual-gate (symmetric channel widths) also exhibits the current increase in the saturation regime. The current of left TFT increases because the sub-drain node (floating n+) is increased. The current of right TFT is also increased, even though the decreased $V_{GS}$ (gate to floating n+ sub-source) suppress the $I_{DS}$ current increase by the negative feed-back. On the other hand, in the proposed structure, the current does not increase largely due to the different current driving capability of the asymmetric TFTs. In case of subTFT1, the current increase is reather small compared with the conventional circuit due to the large channel resistance of narrow-width channel. In case of subTFT2, the suppression of $I_{DS}$ current by $V_{GS}$ decrease is more effective due to high current driving of wide-width channel. Therefore, the output impedance of the proposed circuit is improved, resulting in a good saturation current.

In figure 4b, the solid line exhibits the SPICE simulation result of the proposed device in which the physical parameters of subTFTs are extracted from the measurement of the fabricated single gated TFT (dotted line). It is noted that the output resistance $r_o$ is effectively increased in the proposed device structure. As a simulation results the offset deviation is successfully decreased below 20 mV as shown in Figure 5. The size of TFT1 and TFT2 are W/L = 10μm/8μm and 40μm/8μm respectively.

## 2. 3. Analog Buffer and DAC Design

Figure 6 shows the proposed p-type analog buffer with asymmetric active channel width structure. T1 and T2 build a voltage level shifter. $V_{DD}$ is 6V, $V_{SS}$ is –6V and $V_{IN}$ (–6 ~ 0V) is obtained from resistor-string. Column load capacitance is assumed 20 pF for small size panel (~2 inch). The signal RS is reset, EN is charge enable, and OFF is buffer turn off control. First, RS turns on and the column load is charged to $V_{DD}$. When EN turns on, the column is charged to the fuctional value of $V_{IN}$ as described in eq. (3). For low power consumption, then OFF turns on and T2 turns off so that current through T1 and T2 does not flow.

When $V_{IN}$ is –6V, $V_{OUT}$ is 0V and $V_{GS}$ is –6V with nearly zero offset deviation. When $V_{IN}$ is 0V, $V_{OUT}$ is 3V and $V_{GS}$ is –3V with offset deviation below 20mV, which is the worst case of slow charging. Consequently, output voltages are 0~3V for 6-bit gray scale with offset deviation below 20 mV. Figure 7 shows DAC (digital to analog converter) driving scheme employing the proposed analog buffer. The decoder would select an input voltage from a resistor-string and a buffered analog voltage as described in eq. (3) is obtained from the proposed analog buffer.

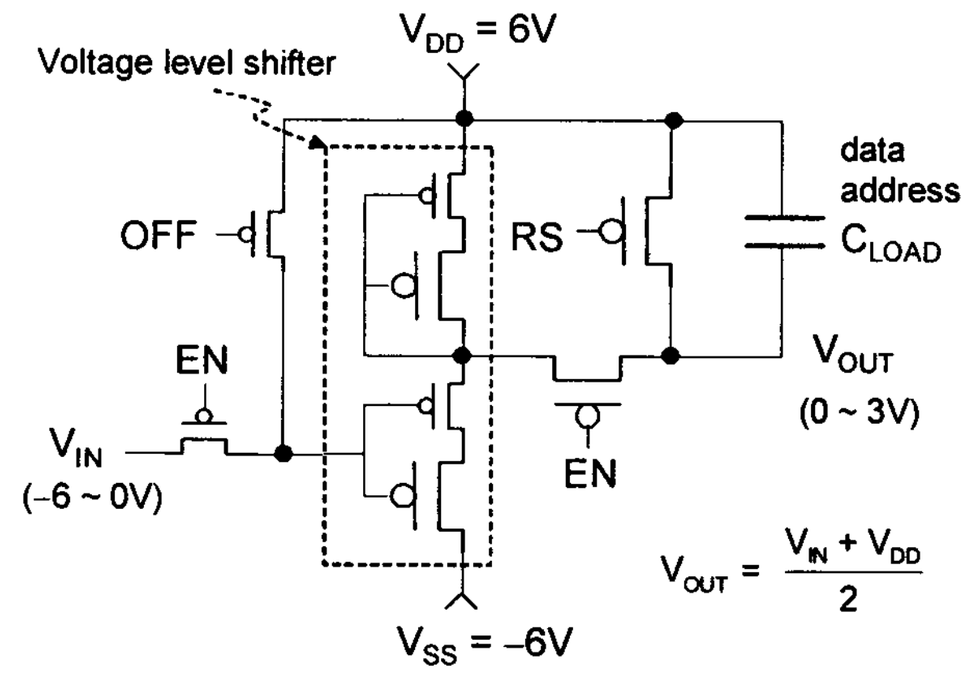



**Figure 6.** (a) The proposed analog buffer design employing feed-back biasing and dual gate TFT with asymmetric channel width structure (Type III). (b) timing diagram of driving buffer

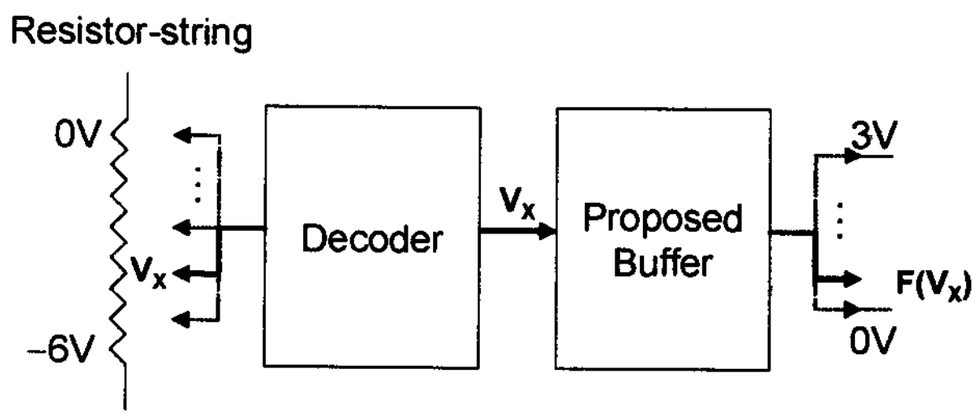



**Figure 7.** The DAC driving scheme employing the proposed analog buffer. The decoder selects an analog voltage ($V_X$) from resistor-string and an output voltage $V_{OUT}$ which has a linear function of $F(V_X)$ is obtained.

The proposed scheme of DAC driving with analog buffer may be promising circuit integrated in low voltage driving AMLCD and AMOLED. It is noted that the proposed circuit is composed of only p-type poly-Si TFTs. The p-type analog buffer may be integrated with digital circuit blocks such as p-type shift-register, level shifter, latch and decoder for PMOS integration in active-matrix displays [10][11][12].

## 3. Conclusions

A new DAC employing p-type poly-Si analog buffer improving the charging speed of pixel data address for AMLCD and AMOLED has been proposed. In the proposed buffer, the output voltages are linearly functional relation to the input voltages, of which the driving scheme allows a large and constant $V_{GS}$ of buffer transistor. In order to improve the accuracy of output buffer, a new two-transistor circuit with asymmetric active layer widths is also proposed. We verified the buffer operation by SPICE simulation and output voltages were 0~3V for 6-bit gray scale with offset deviation below 20 mV.

## 4. References

[1] J.Jin, AMLCD 2002, p1 (2002)
[2] K.C. Moon, IDW 2003, pp. 487~490 (2003)
[3] H. J. Chung, IEE Elecronic Letters, Vol. 37, no. 17, pp. 1093~1095 (2001)
[4] Y. Kida, Eurodisplay 2002, pp. 831~834 (2002)
[5] S.H. Jung, IDW 2003, pp. 1683~1684 (2003)
[6] T. Sasaoka, SID 2001, pp. 384~387 (2001)
[7] M.H. Gao, IEEE SOS/SOI Tech. Conf., pp. 13~14 (1990)
[8] M.C. Lee, IEEE EDL, vol. 25, no. 1, pp.25~27 (2004)
[9] L. Mariucci, AMLCD 2003, pp. 57-60 (2003)
[10] Y. M. Ha, SID 2000, pp.1116~1119 (2000)
[11] W. J. Nam, AMLCD 2002, pp.187~190 (2002)
[12] W.J. Nam, IDW 2003, pp.1685~1686 (2003)