P117: A New Level Shifter using Low Temperature poly-Si TFTs

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Abstract

We proposed a new cross-coupled level shifter circuit using low temperature poly-Si(LTPS) TFT. The proposed level shifter can operate on low input voltage in spite of low mobility and widely varying high threshold voltage of LTPS TFT. Also, the proposed level shifter operates at high frequency and reduces power consumption for having fast rising and falling time and shortening period flowing short-circuit currents.

1. Introduction

As capability of information processing improves rapidly, importance of display technology is being emphasized. The pervading wireless internet and mobile services has endowed a large market for portable devices, such as PDAs, mobile phones, portable game machines and digital camera. Low temperature poly-Si(LTPS) TFT is a remarkable technology which met the requirements for portable device - compact size, high quality image, low power consumption and low cost - because it is able to integrate peripheral driving circuits and other interface circuits on glass without additional inter-connection lines[1-3]. However poly-Si TFT has low mobility and high threshold voltage compared to single crystal MOSFET; circuits using poly-Si TFT have relatively slow operation speed and high power consumption.

Level shifter circuits transfer low-voltage data signal to the high-voltage data signal in the system. The conventional level shifter is difficult to operate in high speed and have low power consumption due to the large threshold voltage of poly-Si TFTs. Figure 1 shows a conventional level shifter circuit using the cross-coupled structure. We assumed that the threshold voltage of nTFT, which drives level shifter circuit, is nearly even with the input data voltage. For example, if the threshold voltage is 3V and input data voltage is 3.3V, V_{gs}-V_{th} of the nTFT is only 0.3V. Although the TFT is turned on, 0.3V is insufficient to drive level shifter circuits. Due to this insufficient driving capability, output node does not drop to 0V and always stays at high-voltage level or it does not rise to high-voltage level from 0V. Under the same conditions, other types of level shifters[4-6] encounter the same problem.

Therefore, we proposed the new level shifter circuit, which has high operating speed and low power consumption, for TFTs that have low mobility and high threshold voltage.

2. The proposed level shifter

2.1 Operation of proposed level shifter circuit

Figure 2 shows the proposed level shifter circuit which can solve speed and power consumption problems of conventional level shifter circuits using LTPS TFT. This proposed circuit is able to operate in low input voltage and widely varying high threshold voltage.

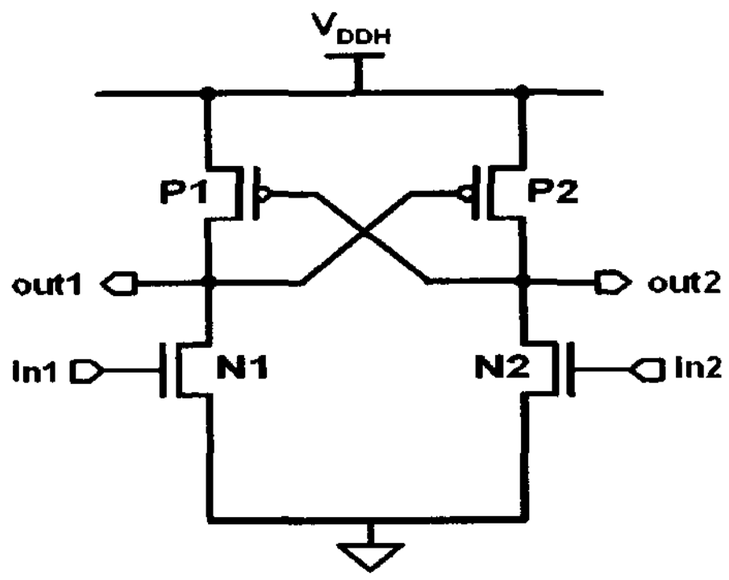

Figure 1. The conventional level shifter circuit.

The proposed circuit increases gate-source voltage of nTFT, the driving transistor of level shifter circuit, by boosting its capacitors. The composition of the proposed circuit is simple. As shown in the figure 2, two pTFTs and two capacitors are added to the conventional circuit in figure 1. Before analysis of operation, we assumed that the threshold voltages of nTFT and pTFT are closed to the value of input data voltage and V_{bias} is equal to input data voltage ($V_{bias}=V_{DDL}$).

Input signal waveforms are shown in figure 3. Both in1 and in2 are low states for initial time period, and during this time, P3 and P4 are simultaneously turned on so that boosting capacitor charges up to V_{bias}. Yet, N1 and N2 do not turn on. After initial time period, in1 goes to high and in2 is continuously at low state. Node Y still remains V_{bias} and node X is boosted as equal as charged amounts in capacitor (V_X). The voltage can be represented as following equations.

$$V_X = V_{bias} + \Delta V$$
$$\Delta V = V_{bias} - V_p$$

Where, ΔV is controlled in proportion to the bias voltage(V_{bias}), V_p is charged voltage in parasitic capacitances showing node X. Because of the peripheral parasitic elements, ΔV never reaches up to V_{bias} even if boosting capacitors, C1 and C2 are very large.

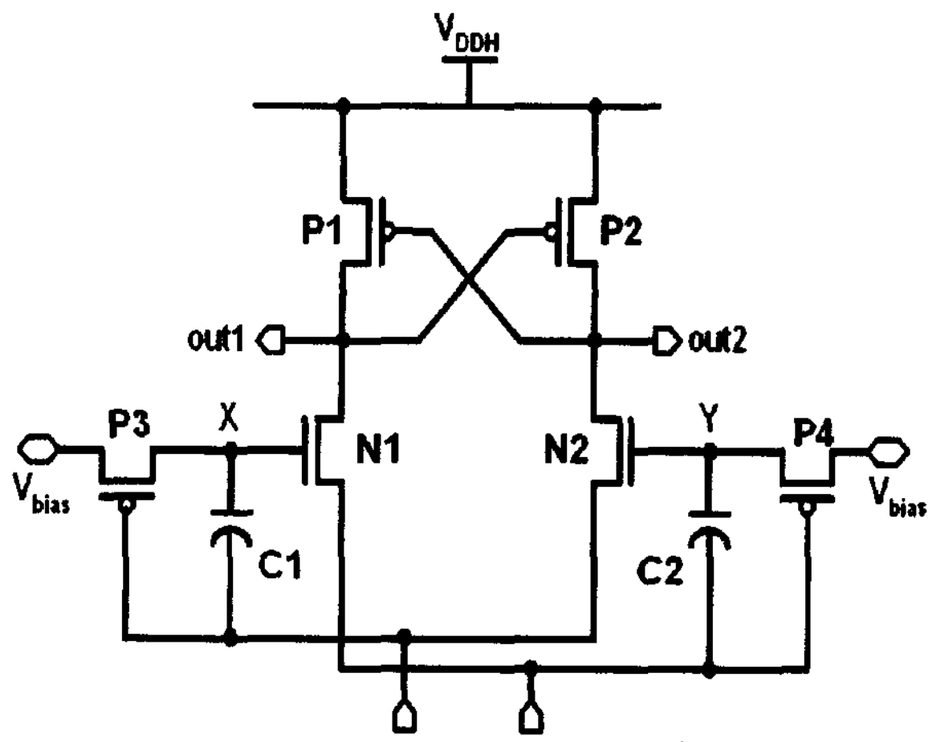

Figure 2. The proposed level shifter circuit.

When node X in figure 2 is boosted to V_x, N1 fully turns on as the gate-source voltage increases. As out1 goes to low, P2 is turned on, and then out2 goes to high voltage, V_{DDH}. As P1 turns off, out1 remains at low state. In the next phase, in1 goes to low and in2 goes to high, and then N1 turns off, N2 turns on. The following operation is the antithesis of its previous phase. Figure 4 shows these operations of node X and node Y.

In this proposed circuit, giving initial time is essential; without the initial time period, this circuit malfunctions because of its wrong initial value of node X and Y. If the voltage of input data signal goes high without charging the boosting capacitor during initial setting time period, node X or Y will go down to low in the next phase. When input voltage goes high again, node X and Y are only boosted up to the voltage of input data signal. Thus, nTFT is not turned on and level shifter circuit does not operate.

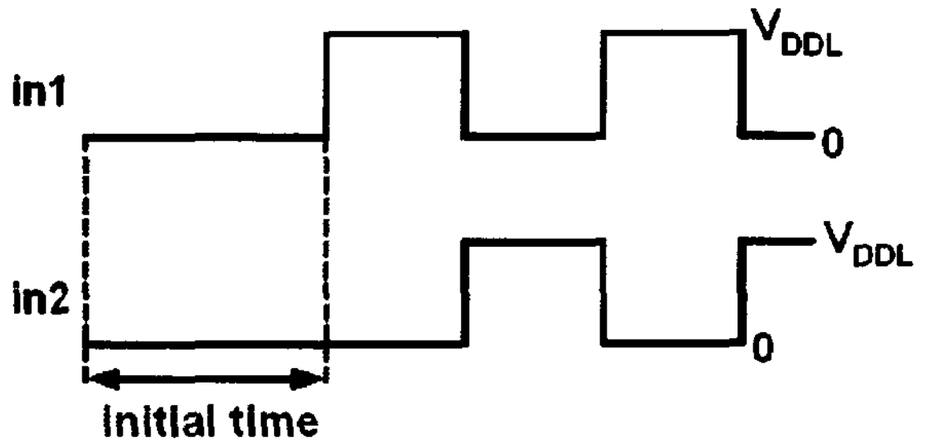

Figure 3. Input waveform of the proposed level shifter circuit.

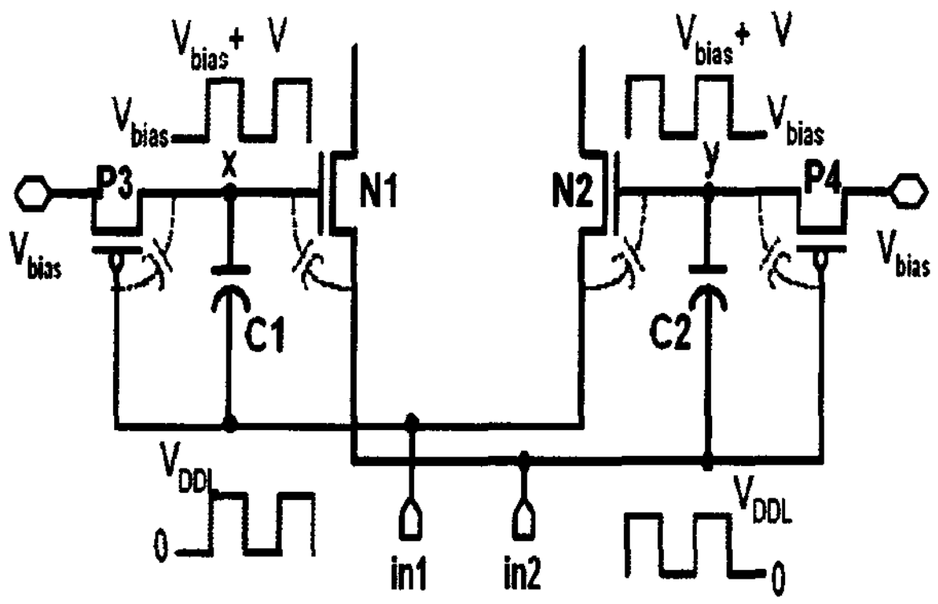

Figure 4. Operation of the proposed level shifter circuit.

2.2 Simulation results of proposed level shifter circuit using HSPICE

Figure 5 is the output waveform of conventional and proposed level shifter in operation frequency of 1MHz. The condition of simulation is as follows. Input voltage is 3.3V and the threshold voltage of nTFT and pTFT is respectively 3V. In this condition, the conventional level shifter does not operate.

Figure 6 shows the simulation results in maximum operating frequency of the conventional circuit and proposed circuit varying input voltage. We can confirm that the proposed circuit operates at higher frequency and lower input voltage than the conventional one. When threshold voltage of TFT is 3V, the conventional circuit begins to operate at input voltage of 4.5V and speed of 1MHz. On the other hand, the proposed circuit operates at a higher speed than 10MHz in input voltage of 3V. When threshold voltage of TFT is 2V, the conventional circuit does not operate at an input voltage lower than 4V but the proposed circuit is able to operate with an input voltage of 2.5V.

Subsequently, the proposed level shifter reduces power consumption. Because the proposed circuit shortens the period flowing short-circuit currents with increasing driving voltage (gate-source voltage of NTFT). In figure 7, results compare short-circuit current of proposed circuits to one of the conventional circuits. The period flowing short-circuit current of the proposed circuit is decreased to about 1/3 times of the conventional one.

2.3 Measured results of proposed level shifter circuit

The proposed level shifter circuit was fabricated using LTPS process technology, which the mobility of pTFT is superior to that of nTFT. The microphotograph of fabricated the proposed level shifter is shown in figure 8.

We added output buffer next to output of level shifter for probing. Figure 9 shows measured output waveform. Measured threshold voltage is about 3V. But practically, measured current driving capability of TFT has been 1/2 of simulation model and It has wide threshold voltage variation. For reasons of these, input voltage that enables to operate has been higher than the simulation results as like figure 9, which shows operating from input voltage of 4V. And large delay of output waveforms has been generated with effect of added output buffer.

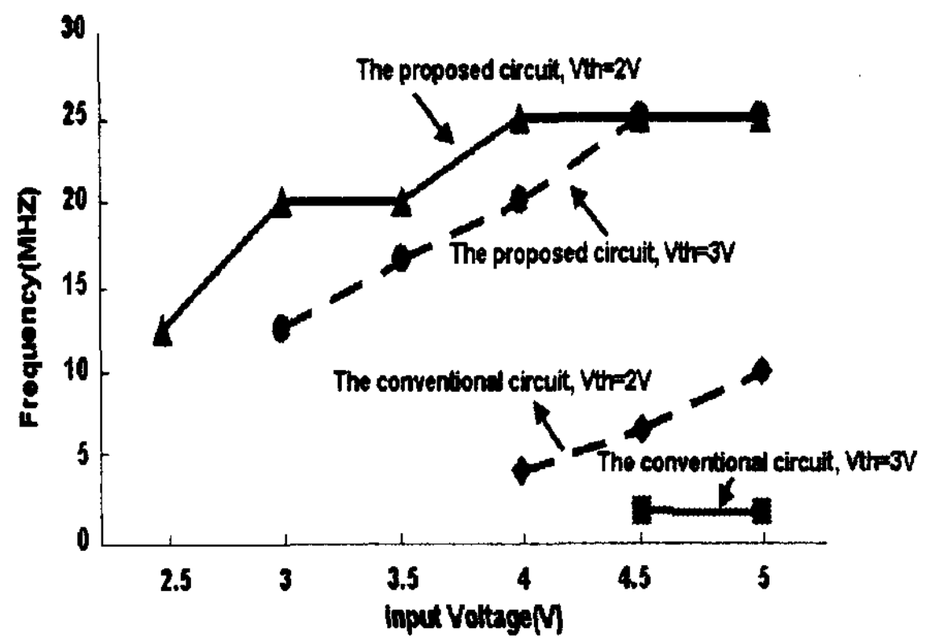

Figure 6. Maximum operating frequency as function of input signal voltage and threshold voltage.

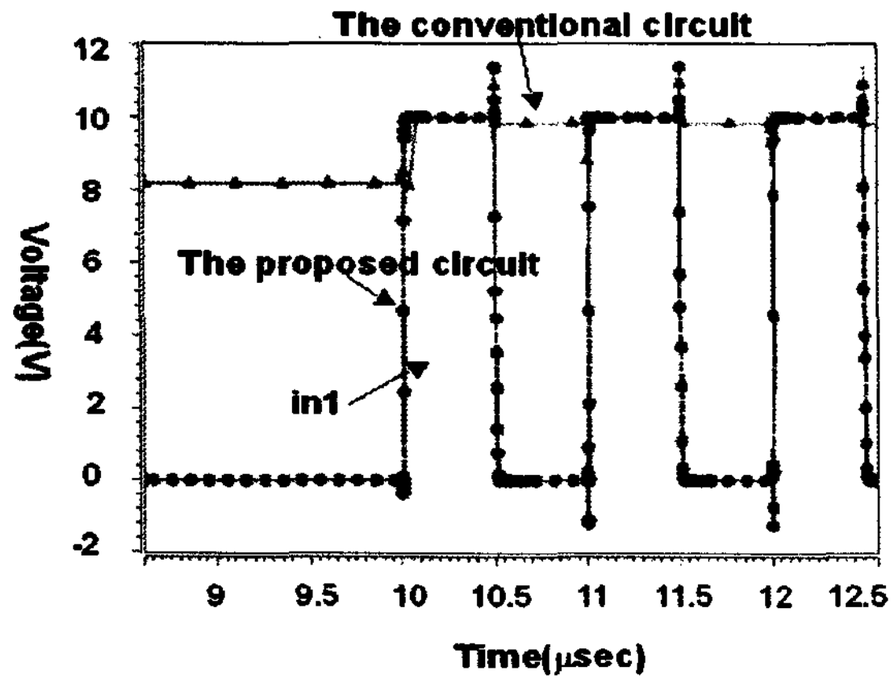

Figure 5. The simulated output waveform.

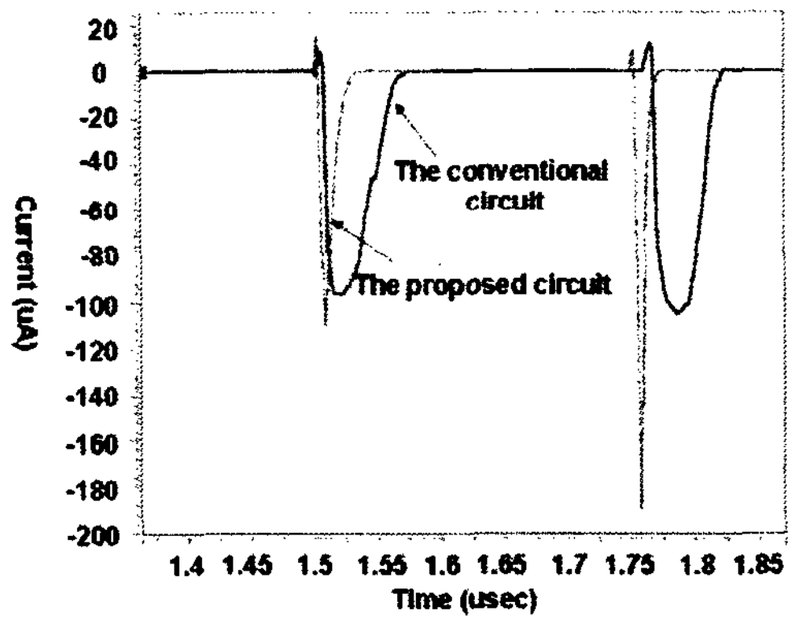

Figure 7. Short-circuit current flowing in level shift circuits.

3. Conclusions

We proposed a new level shifter circuits suitable for LTPS TFT technology. In high threshold voltage and its wide variation, the proposed circuit operates by increasing gate-source voltage with boosting capacitors. Due to the boosting capacitors, the proposed circuit requires a larger area than the conventional circuit but they have other merits that conventional circuits do not have. The proposed circuit is insensitive to process variations and it can operate at high frequency and low input voltage. Also, power consumption is reduced by the shortening of the period of flowing short-circuit currents.

4. References

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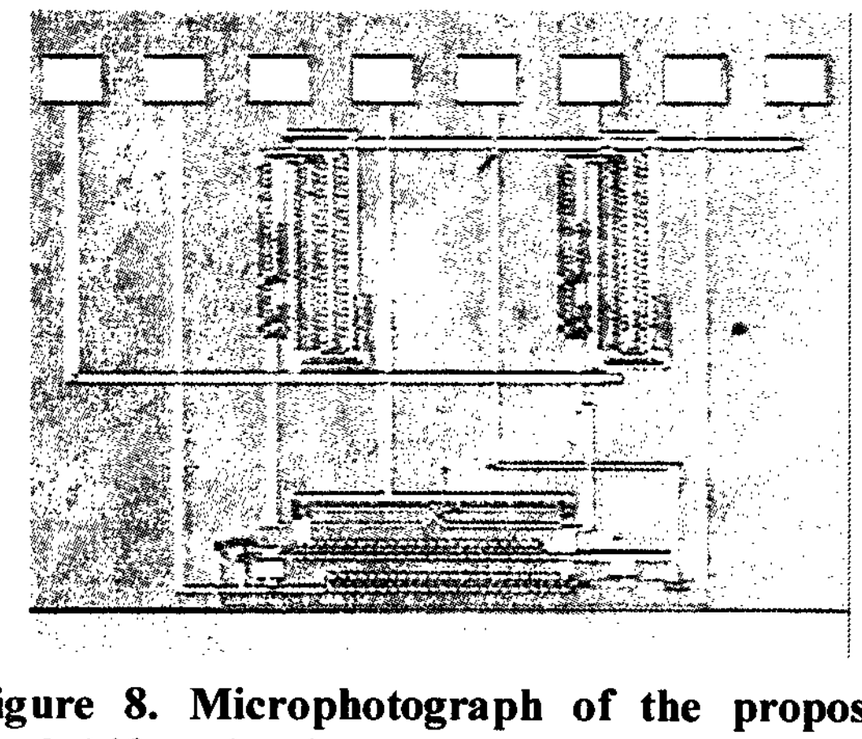

Figure 8. Microphotograph of the proposed level shifter circuit.

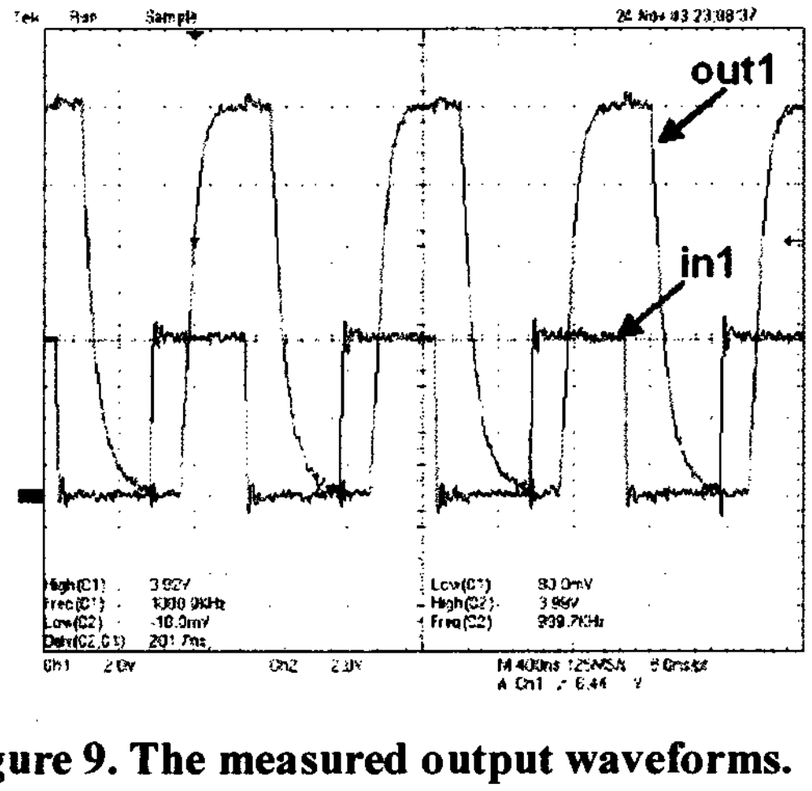

Figure 9. The measured output waveforms.