Advanced P-Channel Poly-Si TFTs for SOG

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Abstract

High performance p-ch poly-Si TFTs with excellent stability were developed. By using a frequency doubled DPSS CW laser, the a-Si on glass could be crystallized into one dimensional single crystalline silicon named as a sequential lateral crystallization (SLC) region. We fabricated p-ch TFTs on SLC region and the typical characteristic values of the TFTs were u_{fe} = 180 cm^2/Vs, V_{th} = -3 V, S.S. = 0.5 V/dec, and I_{off} = 1 pA/um@ V_d = -10V. It is found that the TFTs are very stable after bias stresses such as negative and positive gate biases, hot carrier bias and high current bias. These results indicate that the poly-Si in SLC region is suitable for system on glass (SOG) application.

1. Introduction

The demands for compact, light-weight and high-resolution displays are getting stronger in the mobile application fields. However it is difficult to fulfill these demands by using a conventional amorphous silicon (a-Si) technology because of the difficulties in driving circuit integration and the large size of TFTs. In this point of view, a low-temperature polycrystalline silicon (LTPS) technology has some advantages compared to the a-Si technology. Among the various crystallization techniques, excimer laser annealed (ELA) poly-Si has been spotlighted as a candidate for a promising method however this technique has still issues about mass production such as process instability, high cost and difficult maintenance. Meanwhile, system integration on glass is gaining attractions more and more for next generation information display. It is clear that TFTs for SOG should require better electrical characteristics than those for current AM devices and be more stable like SOI devices.

Recently, Hara *et al.* reported very impressive results on a new approach to make high-quality LTPS, called a CW laser crystallization (CLC).[1] According to their results, the CLC has many advantages such as simplicity, low-cost process and maintenance besides its electrical performances. However, the CLC poly-Si shows various microstructures from very small grains with average size of several tens of nanometers to directionally crystallized super large grains over 10 um-so called, sequential lateral crystallized (SLC) region. This phenomenon appeared regardless of the crystallization process conditions such as a laser power and a scanning speed.[2] Needless to say, SLC region shows a very good electrical performance among the microstructures.[2]

The objectives of this work are to verify the characteristics of the SLC poly-Si TFTs under various electrical bias stresses, and to give the possibilities of this novel technique as another candidate for mass production of a LTPS TFT-OLED

2. Results and Discussion

2.1 SLC poly-Si TFTs

A silicon oxide (SiO_2) layer of 400 nm was deposited on a glass (Corning 1737) prior to the deposition of an amorphous silicon (a-Si) layer. The thickness of the a-Si was 150 nm. We used plasma enhanced chemical vapor deposition (PECVD) method to deposit SiO_2 and a-Si layers. Dehydrogenation of the a-Si was done by a furnace annealing at 480 °C for 5 hrs. After these processes, we irradiated a CW laser to the samples on the 2-D translation stage with X-Y scanning.

A 2ω CW DPSS (diode pumped solid state) laser with the wavelength of 532 nm was used to crystallize the samples. Laser beam size onto the a-Si surface was 20 um (short axis, scan direction) × 800 um (long axis, transverse direction to scan direction), and the beam shape is Gaussian with short axis, top-hat with long axis. Output power and scanning speed of the laser were 10 W and 20 cm/s, respectively.

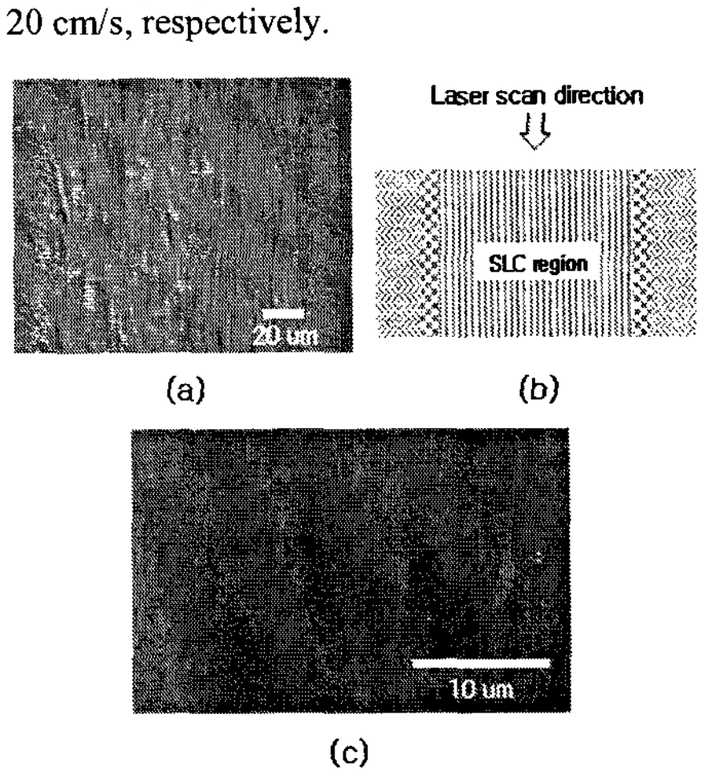


Figure 1. An optical microscope image of crystallized region after a CW laser scanning (a) and its schematic representation with sequential lateral crystallized (SLC) region (b). A SEM image shows SLC region (c).

Figure 1 shows a typical Nomarski optical microscope image of the crystallized region after a CW laser scanning (a) and its schematic representation with sequential lateral crystallized (SLC) region (b). Even though only a single scanning, the total width of crystallized region is over 500 um and especially the SLC region, reaches almost 130 um. In general, the microstructure of CLC poly-Si is appeared like Fig. 1 (b) with different size of grains.[1,

2] The grains are getting smaller from the SLC region to the outer regions. Note that the frozen stream-like region at the center (SLC region) is composed of large, especially very long (over 10 um) elongated grains along the laser scan direction as shown in a SEM image of Fig. 1 (c).

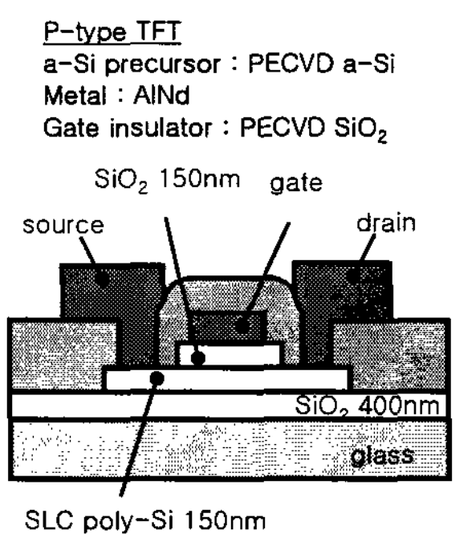


Figure 2. The cross-sectional schematic diagram of a SLC poly-Si TFT.

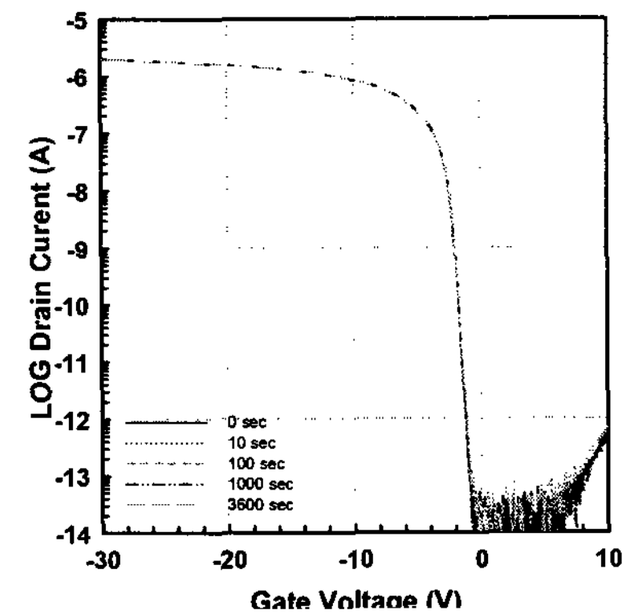
The p-channel poly-Si TFT with a coplanar structure was fabricated by using a SLC region as an active layer.(see Fig. 2) The fabrication process is described in the literature.[2]

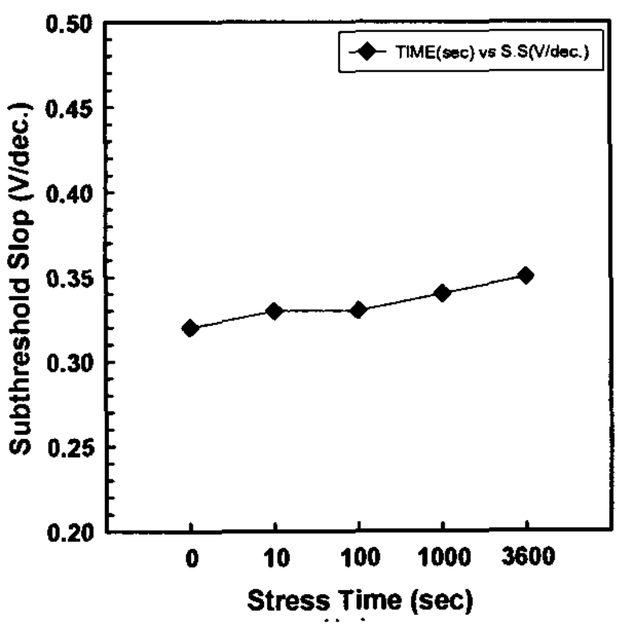
2.2 Stability against Various Bias Stresses

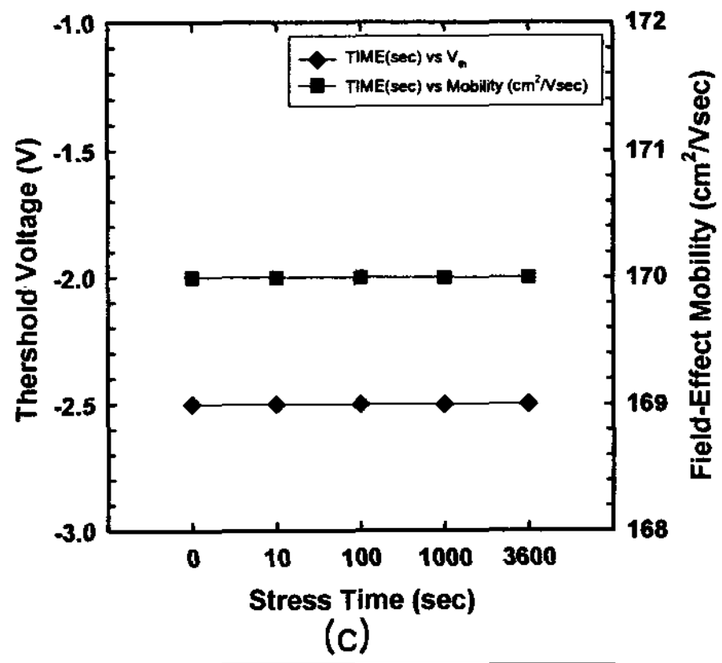
In this section, we describe the results of the electrical bias stress effect on the characteristic variation in p-type SLC poly-Si TFTs. We examined the characteristic changes of the TFTs under 4 different electrical bias stresses as a function of stress time; negative and positive gate biases, hot carrier bias, high current bias, respectively. In Figures 3 through 6, the results were described with the transfer characteristics variation (a), the subthreshold slope change (b), and the threshold voltage and the field effect mobility change (c) during bias stresses. The characteristic values such as mobility, threshold voltage and subthreshold slope, before and after bias stresses, were summarized in each figure with a table. Before we give an explanation of our results, we note that we do not carry out the attempts to enhance the electrical performances of SLC poly-Si TFTs, such as surface treatments by plasma and /or hydrogenation after TFT fabrication.

Generally, the poly-Si TFTs suffer from the gate bias stress because the weak-bonds at grain boundaries are easily broken during the stress and they generate enormous states result in obstructing carrier currents.[3] However, in Figures 3 and 4, the electrical characteristics (subthreshold slope as well as threshold voltage) of the SLC poly-Si TFTs do not change during the positive or negative stresses. This means that there are little weak-bonds, to increase deep states by being broken, in the SLC poly-Si. In addition, it can be considered that the SLC poly-Si matches well with the PECVD SiO_2. This is, of course, very important factor for mass productions and this can be one of the merits of the SLC poly-Si film.

It is well known that the poly-Si TFTs under hot carrier bias stress show some degradation in mobility, threshold voltage and subthreshold slope. All the reason of this degradation has responsible for the creation of acceptor-like interface states and of mid-gap states by the severe collision of hot carrier near the drain. [4] The results of Fig. 5 show that the SLC poly-Si TFT is very stable under hot carrier bias.



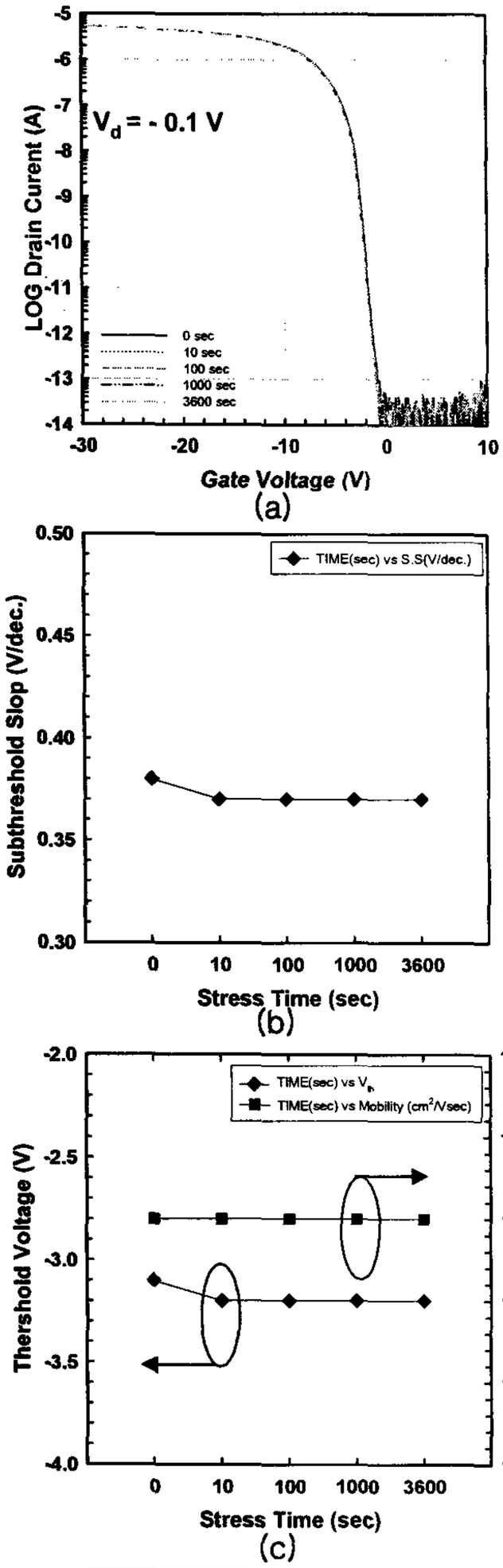




(c)

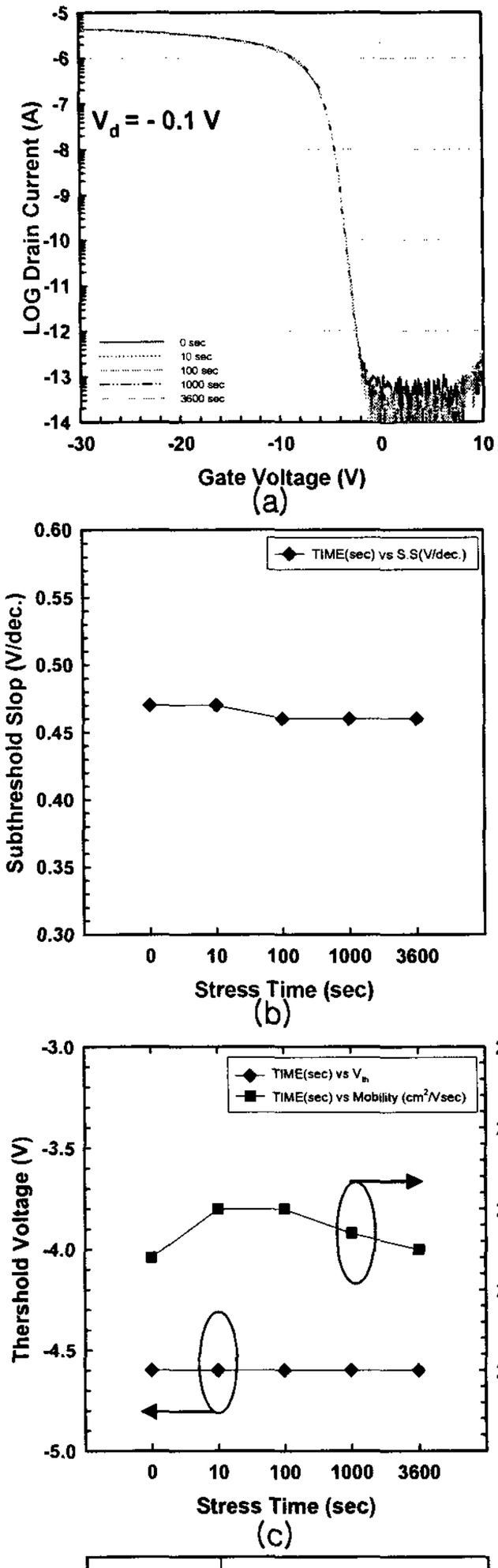
	Positive gate bias (V_G = +20 V)	
	Before stress (initial)	After Stress (1 hours)
Mobility (cm^2/V.sec)	170	170
V_{th} (V)	- 2.5	- 2.5
S.S. (V/dec)	0.32	0.35

Figure 3. Positive gate bias stress effect on the SLC poly-Si TFT(W/L=8/8); transfer characteristics (a), sub threshold slope variation (b), threshold voltage and field effect mobility variation (c). The characteristic parameters are summarized in the table before and after stress



	Negative gate bias (V_G = - 20 V)	
	Before stress (initial)	After Stress (1 hours)
Mobility (cm²/V.sec)	173	173
V_{th} (V)	- 3.1	- 3.2
S.S. (V/dec)	0.38	0.37

Figure 4. Negative gate bias stress effect on the SLC poly-Si TFT (W/L=8/8); transfer characteristics (a), sub threshold slope variation (b), threshold voltage and field effect mobility variation (c). The characteristic parameters are summarized in the table before and after stress



	Hot carrier bias (V_G = - 5 V, V_D = - 20 V)	
	Before stress (initial)	After Stress (1 hours)
Mobility (cm²/V.sec)	214	215
V_{th} (V)	- 4.6	- 4.6
S.S. (V/dec)	0.47	0.46

Figure 5. Hot carrier bias stress effect on the SLC poly-Si TFT (W/L=8/8); transfer characteristics (a), sub threshold slope variation (b), threshold voltage and field effect mobility variation (c). The characteristic parameters are summarized in the table before and after stress.

	High current bias (V_G = - 30 V, V_D = - 10 V)	
	Before stress (initial)	After Stress (1 hours)
Mobility (cm^2/V.sec)	176	176
V_{th} (V)	- 4.2	- 4.4
S.S. (V/dec)	0.50	0.48

Figure 6. High current bias stress effect on the SLC poly-Si TFT(W/L=8/8); transfer characteristics (a), sub threshold slope variation (b), threshold voltage and field effect mobility variation (c). The characteristic parameters are summarized in the table before and after stress

These excellent stabilities under gate bias and hot carrier bias stresses might be due to the crystalliniy of the SLC poly-Si layer in the channel. As shown in Fig. 1 (c), the probability of grain-boundary penetration of carriers is reduced when the channel is parallel to the scan direction like this works. Indeed, the rms roughness of SLC poly-Si films is a half of that of conventional ELC poly-Si films. Considering the size of the TFT (W/L=8/8), there are few grain boundaries in the channel, if any a few grain boundaries in it. Therefore the electrical characteristics are not affected by the bias stresses. While, different from above results, the SLC poly-Si TFT under high current bias stress shows some changes during the stress. The transfer curve shows slight parallel shift toward negative gate voltage direction, which results in subthreshold voltage shift from -4.2 to -4.4 V. According to Maeda *et al.*, this parallel shift of transfer curve is due to the breaking of Si-H bonds at the poly-Si/SiO_2 interface so that hole traps at these sites.[5] This explanation can be applied to our case because we used PECVD SiO_2 with SiH_4 gas and the maximum process temperature was not exceed 360 °C so that SiO_2 includes some hydrogen.

Although the reason why the SLC poly-Si TFTs are so stable against various bias stresses should be studied more, the experimental results of bias stress effects on the SLC poly-Si TFT indicate that the SLC poly-Si TFTs are enough to be adopted for switching and driving devices for AM-OLEDs and SOG.

3 Conclusion

We fabricated the p-type SLC poly-Si TFTs by using a CW laser scanning. The various bias stress effects on the electrical characteristics of the SLC poly-Si TFTs as a function of stress time were reported for the first time. The results showed that the SLC poly-Si TFTs are very stable under positive/negative gate bias stresses and hot carrier bias stress. This is due to the good crystalliniy of the SLC poly-Si films. Under high current bias stress, the transfer curve slightly shifted to negative gate voltage. This may result from the H in SiO_2 film. Considering the excellent electrical characteristics of the SLC poly-Si TFTs as well as the stability under various bias stresses, the SLC poly-Si TFTs can be applied for SOG.

4. Acknowledgements

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