P.127: Condensation and Baking Effects of Polymer Gate Insulator for Organic Thin Film Transistor

S. I. Kang, J. H. Park, S. P. Jang, and Jong S. Choi

Department of Electrical, Information and Control Engineering, Hongik University, Seoul, 121-791, Korea

e-mail: ksi3819@hanmail.net, Tel: +82-2-320-1488

Abstract

Performances of organic thin film transistors (OTFTs) can be detrimentally affected by the state of the gate dielectric. Because of the bad stability of polymers, OTFTs with polymer gate dielectrics often provide abnormal characteristics. In this study, we report the condensation effect of the polymer gate dielectric layer. For the observations of the effect of the condensation, the spin-coated polymer layers with various deposition conditions were fabricated and left under low vacuum condition for several days. It is observed that the thickness of polymer layer and the electrical characteristic of OTFTs vary with the condensation time.

1. Introduction

Over the past few years, organic thin-film devices, such as organic light-emitting diodes, OTFTs and photodetectors, have been investigated with the steady progress in device performances and ever increasing range of applications. Among various organic materials, polycyclic aromatic hydrocarbon pentacene is one of the most promising organic semiconductors mainly due to its high hole mobility. Many researchers have extensively studied materials to develop high-performance pentacene-based OTFTs, focusing on improving their electrical properties. The choice of the gate dielectric material is one of the most crucial factors for good OTFT performances. Also for inexpensive applications, gate dielectrics with low-cost fabrication methods are of great interest, including solution-processable polymer gate dielectrics which can be deposited by spin coating, spray coating, or printing, rather than by vacuum deposition[4],[5]. The use of polymer dielectric gate materials, such as poly(4-vinylphenol) and poly(methyl-methacrylate), has been reported for the OTFTs, recently[1]-[3]. However, there are still a number of problems with the polymers as gate dielectrics. One of the serious problems is the stability of polymer films. In this work, the characteristic variations of OTFTs with poly-4-vinylpenol(PVP) gate dielectric with the condensation and baking treatment have been investigated.

2. Experimental details

The structure of fabricated inverted staggered OTFT is shown in figure 1. The pentacene active layer and the metal electrodes were thermally evaporated through shadow masks on the PVP gate insulator consequently. Aluminum and gold were used as the gate and source/drain electrodes respectively. The channel length and width of the fabricated OTFTs were 100 μm and 5 mm, respectively. To investigate the stability of PVP insulating film, PVP was spin-coated at various weight percents, 4wt%, 8wt% and 10wt%, where ethanol was used as a solvent, and samples of each

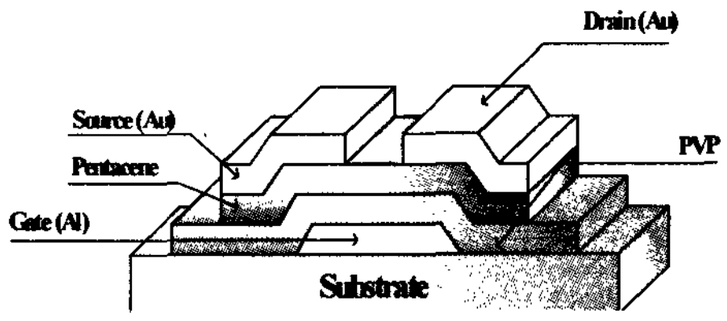


Figure 1. The structure of fabricated OTFT.

group (weight percent) were deposited at 2000rpm, 3000rpm, 4000rpm and 5000rpm respectively. The samples were soft-baked to remove the solvent under vacuum condition at 100 ° C during 1 hour. After the soft-baking, the samples were kept under low vacuum circumstance for PVP film condensation, and the variations of the PVP thickness with the condensation time were observed. On some samples, additional baking processes, named hard-baking process, were carried out to accelerate PVP film condensations.

3. Results and Discussion

As shown in figure 2, the PVP film thicknesses were decreased with the condensation time (without the hard-baking) except for the film deposited at the 2000rpm, which exhibited no thickness change up to 5 days. In order to observe the variation of OTFT

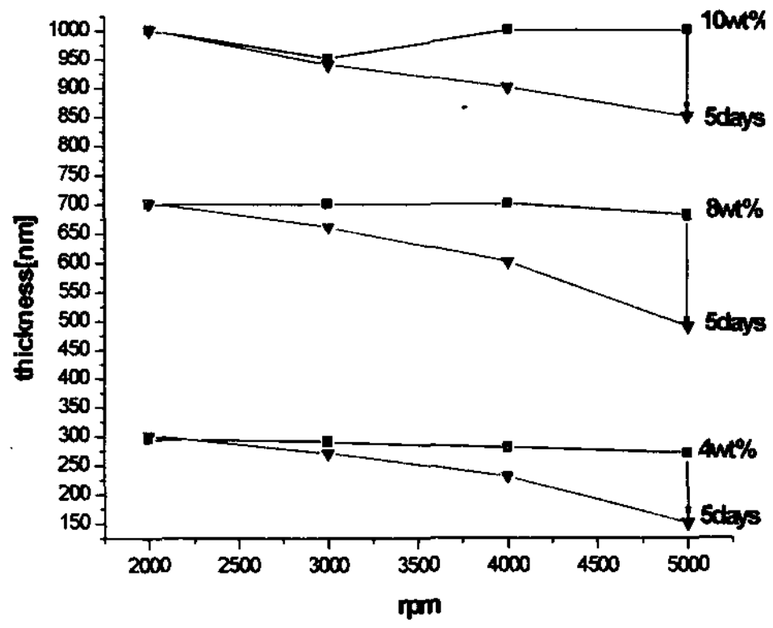


Figure 2: PVP Film thickness with various conditions and aging time.

characteristics with the condensation time, TFTs were fabricated with PVP gate dielectrics with different condensation times. The electrical characteristics of the OTFT with 8wt% PVP gate insulator spin-coated at 4000rpm are shown in Figure 3. As expected, the saturation currents of the OTFT with the PVP film condensed for 5 days were increased. It is considered that residual solvent was evaporated completely during the condensation and the decreased thickness of the dielectric layer induces an increased capacitance of the insulator.

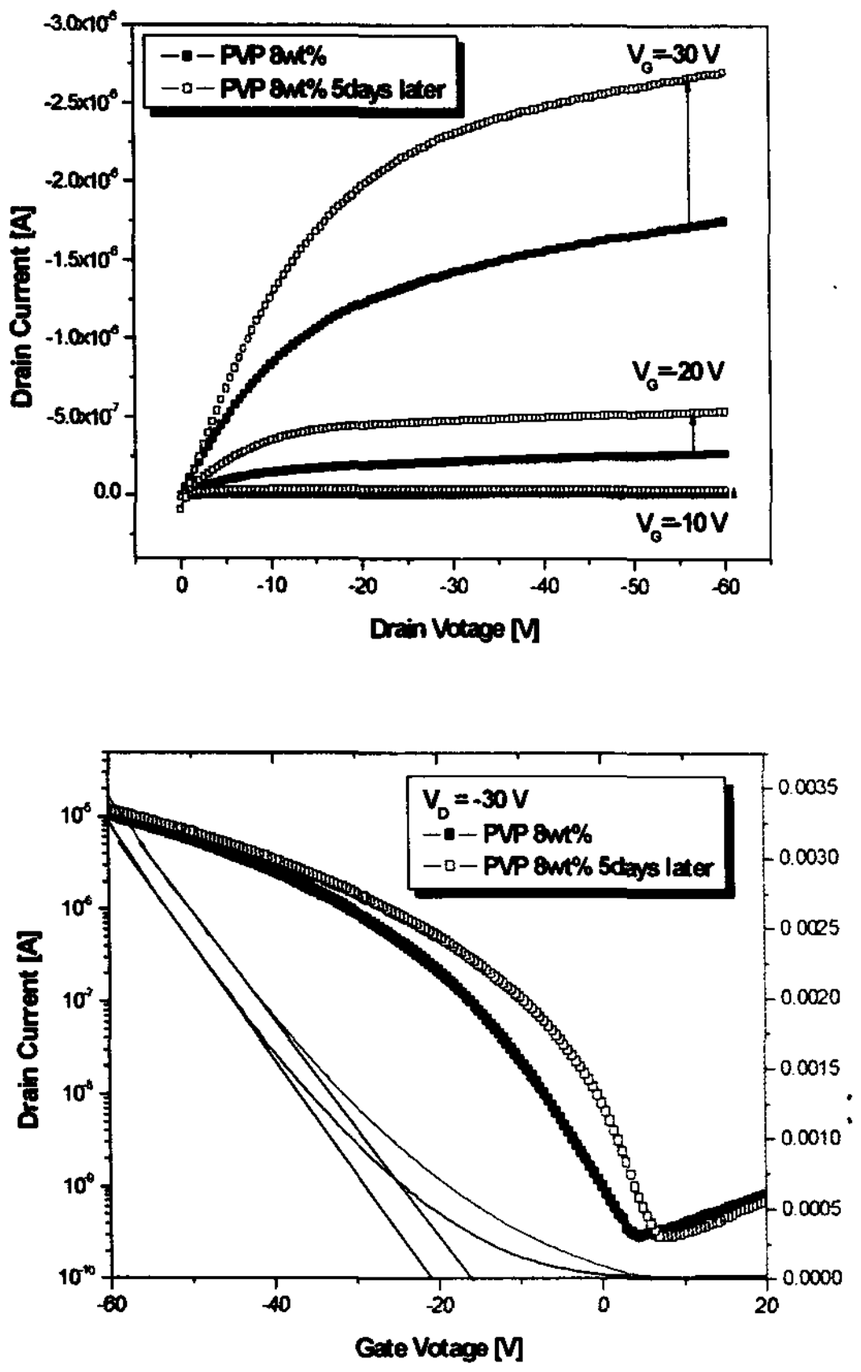


Figure 3: The electrical characteristics of OTFTs.

The solvent cannot be completely removed from the spin-coated PVP film by the simple soft-baking. In order to eliminate the residual solvent and accelerate the film condensation, the PVP layer was hard-baked at 180℃ for 1 hour under 3 mtorr argon gas circumstance. The thickness of hard-baked PVP film was 650nm and remained the same even with the following 5 day condensation, which is almost the same as that of the PVP film condensed for 5days without hard-baking. Moreover, as shown in figure 4, the electrical characteristics of the OTFT with the hard-baked insulator were much improved compared with those of the OTFT with 5-day-condensed insulator without hard-baking. The threshold voltage was decreased from -19V to -9V and the subthreshold slope was decreased from 4.1 V/decade to 2.9 V/decade. The hard-baked device also shows better saturation characteristic. The mobilities were extracted at a drain-source voltage of -30V and gate-source voltage of -15V, as shown in figures 3 and 4. The mobility of the OTFT with the just soft-baked PVP insulator was 0.082 $cm^2/V \cdot sec$. As expected from figure 4, the OTFT with the hard-baked insulator shows the highest mobility (0.41 $cm^2/V \cdot sec$), the lowest threshold voltage (about -9 V) and the lowest off-state current (about 10^{-11} A).

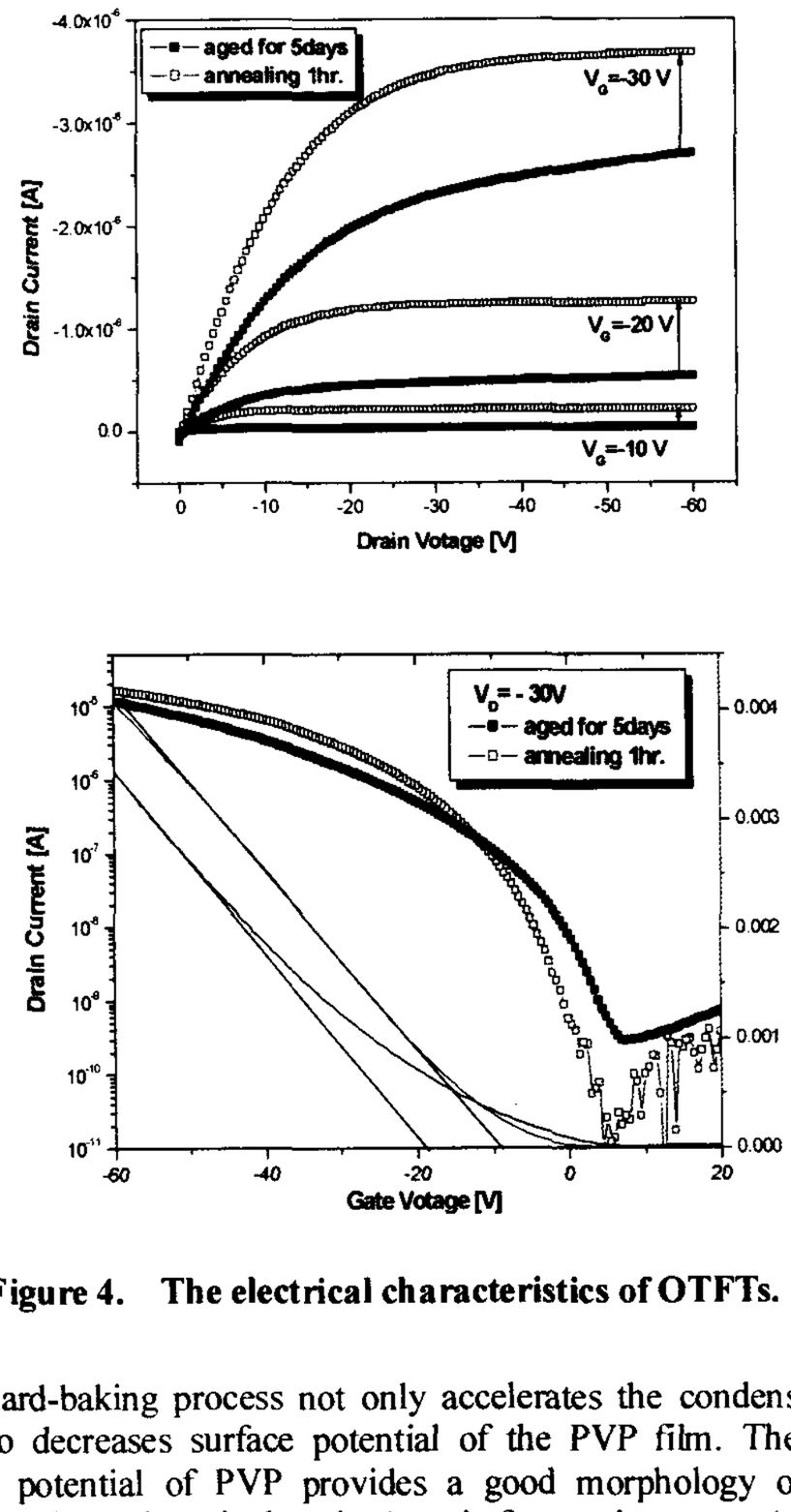


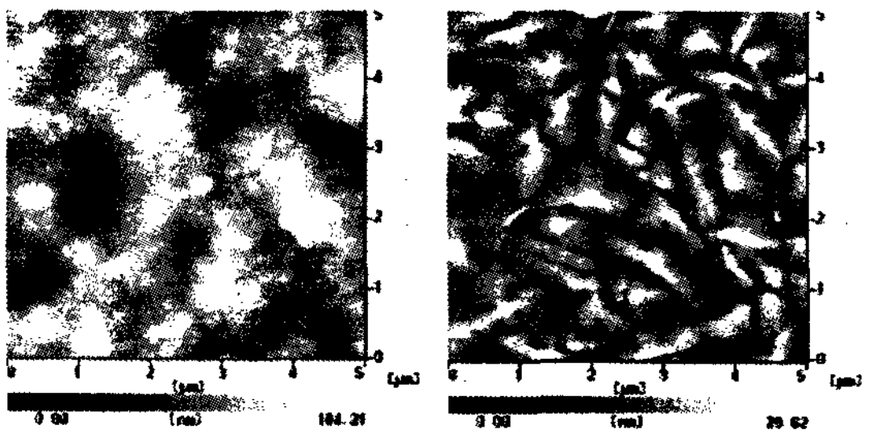
Figure 4. The electrical characteristics of OTFTs.

The hard-baking process not only accelerates the condensation but also decreases surface potential of the PVP film. The low surface potential of PVP provides a good morphology of the pentacene layer deposited on it. Atomic force microscopy (AFM) was utilized to for studying the surface morphologies of the pentacene layers on PVP films spin-coated under various conditions. The thickness of the pentacene layer is 30 nm, and the deposition rate is 0.5 Å/sec. Figure 5(a) shows the morphology of pentacene film on the soft-baked and condensed PVP layer, while figure 5(b) is the image of the pentacene film on the soft- and hard-baked PVP film.

4. Conclusions

The pentacene-based OTFTs with polymer insulators have been investigated. The residual solvent in spin coated polymer insulator can affect the characteristics of OTFTs. The residual solvent of PVP dielectric layer was eliminated by condensation or hard-baking process. Most characteristic parameters of OTFTs such as on/off current ratio and carrier mobility were improved by using condensed or hard-baked gate insulator. The grain size of deposited pentacene film on the hard-baked PVP layer was larger

than that of the PVP film only with soft-baking. It can be suggested that the optimized coating/condensation processes of PVP films may greatly improve the electrical properties of the pentacene films on them. For the exact understanding of this aspect and the further improvement of OTFT properties, further works are necessary.



(a) (b)

Figure 5. Atomic force microscopy (AFM) images of pentacene films deposited on spin-coated PVP with various conditions.

5. Impact

In this paper we demonstrate a condition for high quality PVP layer deposition. The stable PVP layer may allow more stable characteristics of OTFTs. The drying and condensing method of spin-coating polymer gate dielectrics needs further optimizations to improve OTFT characteristics.

6. Acknowledgements

This work was supported from Information Display R&D Center, one of the 21st Century Frontier R&D Program funded by the Ministry of Science and Technology of Korea.

7. References

[1] G. Horowitz, D. Fichou, X. Peng, Z. Xu, and F. Garnier, "A field-effect transistor based on conjugated alpha-sexithienyl," Solid State Commun., **72**, pp. 381–384, (1989).
[2] F. Garnier, R. Hajlaoui, A. Yassar, and P. Srivastava, "All-polymer field effect transistor realized by printing techniques," Science, **265**, pp.1684–1686, (1994).
[3] C.J. Drury, C.M. Mutsaers, C.M. Hart, M. Matters, and D.M. de Lee., "Low-cost all-polymer integrated circuits", Appl. Phys. Lett., **73**, 108, (1998).
[4] Y. Qiu, Y. Hu, G. Dong, L. Wang. J. Xie, and Y. Ma, "H_20 effect on the stability of organic thin-film field-effect transistors", Appl. Phys. Lett., **83**, 1644, (2003).
[5] J. Zaumseil, T. Someya, Z. Bao, Y. Loo, and R. Cirelli, "Nanoscale organic transistors that use source/drain electrodes supported by high resolution rubber stamps", Appl. Phys. Lett., **82**, 793, (2003).