Comparison of Degradation Phenomenon in the Low-Temperature Polysilicon Thin-Film Transistors with Different Lightly Doped Drain Structures

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Abstract

Degradation phenomenon in the low-temperature polysilicon (LTPS) thin-film transistors (TFTs) with different junction structures was investigated. A gate-overlapped lightly doped drain (GOLDD) structure showed better hot-carrier stress (HCS) stability than a conventional LDD one. On the other hand, high drain current stress (HDCS) at $V_{gs} = V_{ds}$ conditions caused much severe device degradation in the GOLDD structure because of its higher current level resulting in the higher applied power. It is suggested that self-heating-induced mobility degradation in the GOLDD TFTs be suppressed for using this structure in short-channel devices.

1. Introduction

Low-temperature polysilicon (LTPS) thin-film transistors (TFTs), with a level of electron mobility that is 2 to 3 orders of magnitude higher than that of amorphous silicon (a-Si), have attracted great attention in the flat panel display (FPD) such as active matrix liquid crystal display (AMLCD) and active matrix organic light-emitting diode (AMOLED). In particular, recent remarkable development in information technology (IT) is expected to rapidly expand the mobile display market, and, therefore, high-resolution and highly integrated system on panel (SOP) based on the LTPS technology has been widely investigated for mobile applications.

In order to integrate more system blocks on the same substrate, smaller design rule and shorter channel length in the TFTs are needed. However, it is difficult to reduce the polysilicon TFT size because several limitations such as still high operation voltage and existence of grain boundaries in the active layer accelerate degradation of shorter channel polysilicon TFTs. In other words, the improvement of the reliability of polysilicon TFTs is the most important requirement in the realization of the high-performance displays.

There have been many efforts to improve the reliability of polysilicon TFTs. Recently, the gate-overlapped lightly doped drain (GOLDD) structure has been proposed by several authors [1-3] for the improvement of the reliability of polysilicon TFTs. It was suggested that the GOLDD structure is effective for the drain avalanche hot carrier (DAHC) effect [4]. In spite of many reports on the advantage of GOLDD structure, however, the study on the degradation phenomena of the GOLDD TFTs has not been enough. Especially, self-heating-induced degradation of polysilicon GOLDD TFTs has not been investigated yet.

In this work, comparative study on the degradation phenomena of the polysilicon GOLDD TFTs versus conventional LDD TFTs was performed. It is suggested that both the hot carrier stress (HCS) and the high drain current stress (HDCS) be considered before evaluation of the reliability of these devices.

2. Experimental

A schematic cross-sectional view of the polysilicon TFTs studied in this work is shown in Fig. 1. The channel length and the LDD length were 4μm and

1.5㎛, respectively, for both devices. Buffer oxide and a-Si films were deposited by plasma enhanced chemical vapor deposition (PECVD). After dehydrogenation, a-Si films were crystallized by sequential lateral crystallization (SLS) method and then were islanded. The thickness of the gate oxide and the gate metal were 50nm and 150nm, respectively. For adjustment of flatband voltage, channel doping and pretreatment conditions before gate oxide deposition were optimized. After source and drain (S/D) junction formation by phosphorus ion doping, furnace annealing was performed at 500℃ for 2 hours in order to activate the dopants, and followed by S/D metal deposition by sputtering. The n- and n+ junction, respectively, had the same dose for both LDD TFTs and GOLDD TFTs. Finally, passivation nitride was deposited by PECVD and subsequently hydrogenation process was performed to improve the TFT characteristics.

Electrical characteristics of the TFTs were measured with HP4156A. Two different DC stress conditions, that is, HCS at DAHC region and HDCS at channel hot electron (CHE) region, respectively, were applied to the TFTs at room temperature. The stress time was 60s for both cases. Detailed stress conditions for each case are described in section 3.

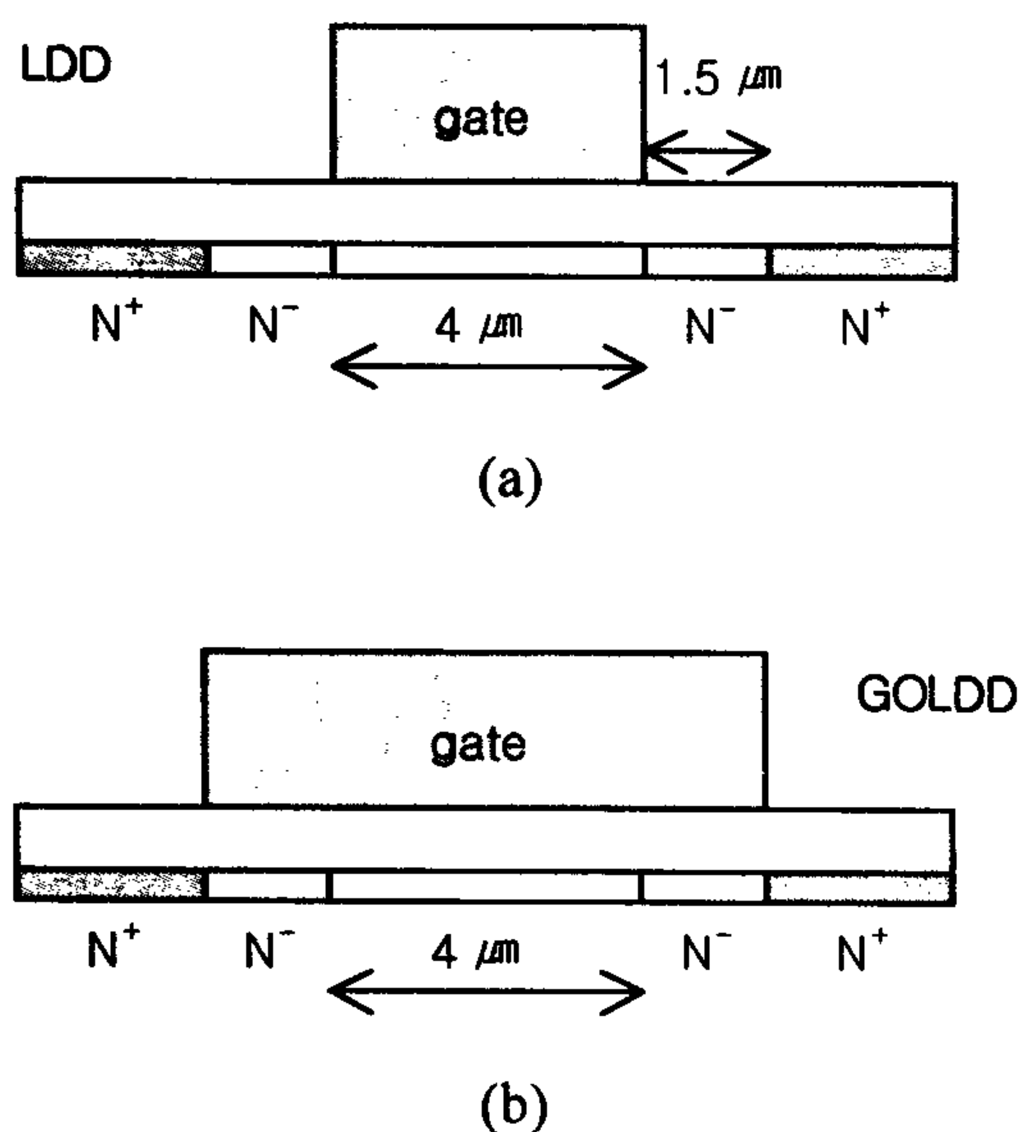
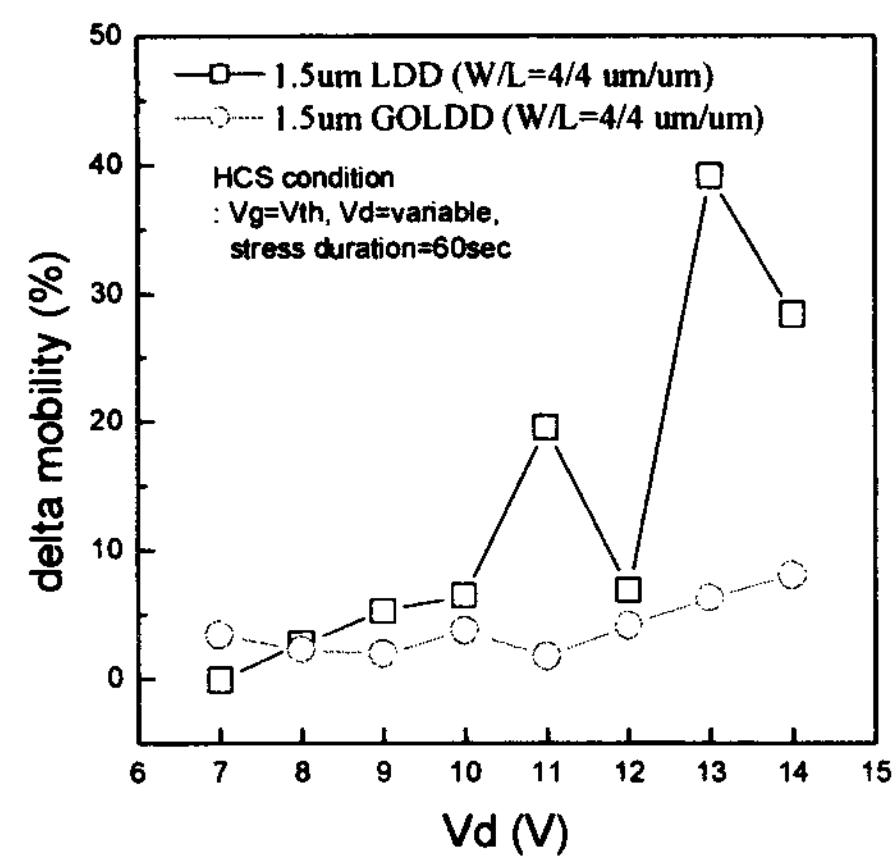


Figure 1. Schematic cross-sectional view of (a) LDD TFT and (b) GOLDD TFT

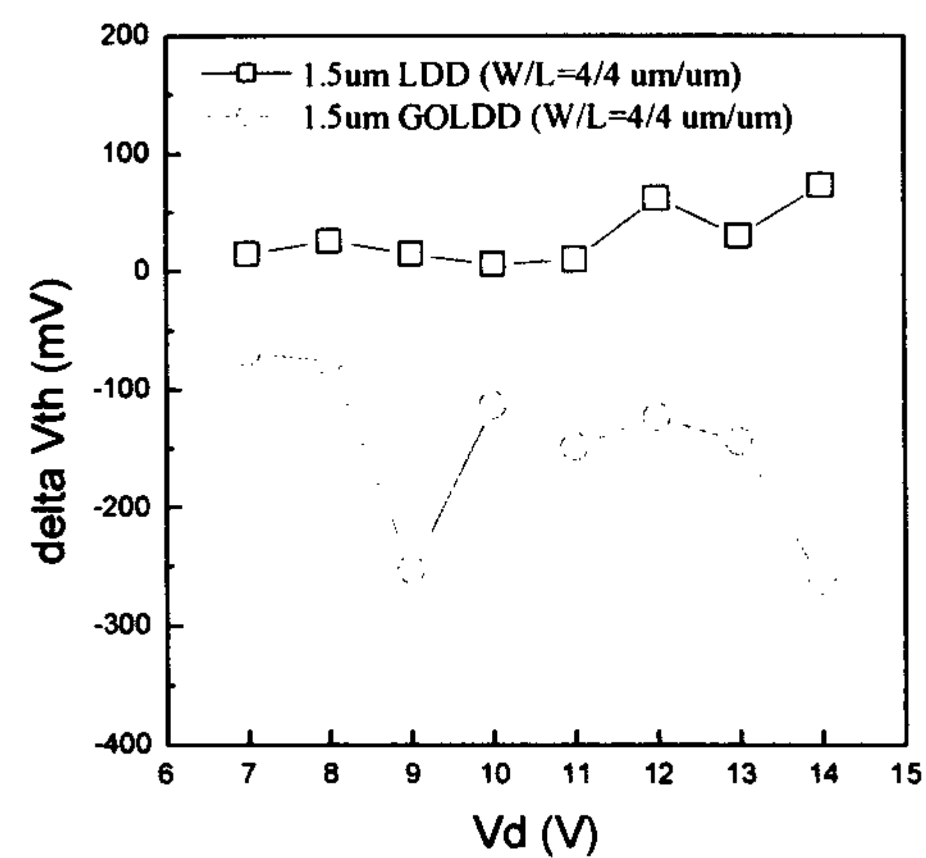
3. Results and discussion

A. Degradation of polysilicon TFTs under HCS

For comparison of degradation phenomena of the LDD TFT and the GOLDD TFT under HCS, the same DC stress conditions were applied to both TFTs. In detail, V_{gs} was maintained at V_{th}, and V_{ds} was varied from 7V to 14V with bias step of 1V. The stress was applied during 60s at each voltage step. The degradation was estimated for maximum field effect mobility variation and V_{th} variation, respectively.



(a)



(b)

Figure 2. Comparison of (a) mobility degradation and (b) V_{th} shift between LDD TFT and GOLDD TFT

Figure 2 (a) and (b) show field effect mobility degradation and V_{th} shift, respectively, with various HCS conditions for the LDD TFTs and the GOLDD TFTs. It can be seen that the GOLDD structure has strong immunity to the HCS with respect to the mobility degradation, which agrees with many other reports [5.6]. On the other hand, it is noted that the polarity of V_{th} shift in the GOLDD TFTs is opposite to that of the LDD TFTs in Figure 2 (b). The negative shift of V_{th} in the GOLDD TFTs can be due to the hole injection into the gate oxide resulting from large negative vertical field in the LDD region [7]. The larger V_{th} shift of the GOLDD TFTs indicates more hot carrier generation in this junction structure.

Figure 3 shows drain current degradation as a function of stress time for the LDD TFTs and the GOLDD TFTs. The smaller decrease of drain current after stress in the GOLDD structure supports the results of mobility degradation shown in Figure 2 (a), indicating that the reliability of this structure is better than the LDD one in the viewpoint of current drivability.

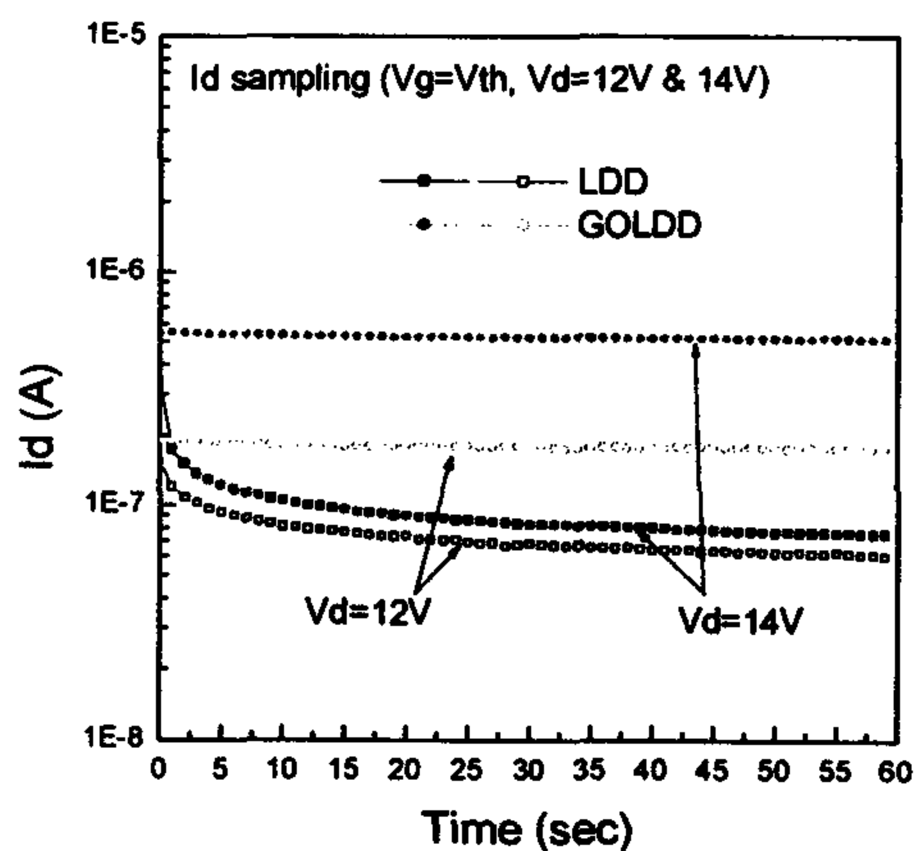


Figure 3. Comparison of drain current degradation as a function of stress time between LDD TFTs and GOLDD TFTs

B. Degradation of polysilicon TFTs under HDCS

For comparison of degradation phenomena of the LDD TFT and the GOLDD TFT under HDCS, the same DC stress conditions were applied to both TFTs in the channel hot electron (CHE) region. $V_{gs}=V_{ds}$ varying from 8V to 19V with bias step of 1V was applied. The stress time at each voltage step was 60s.

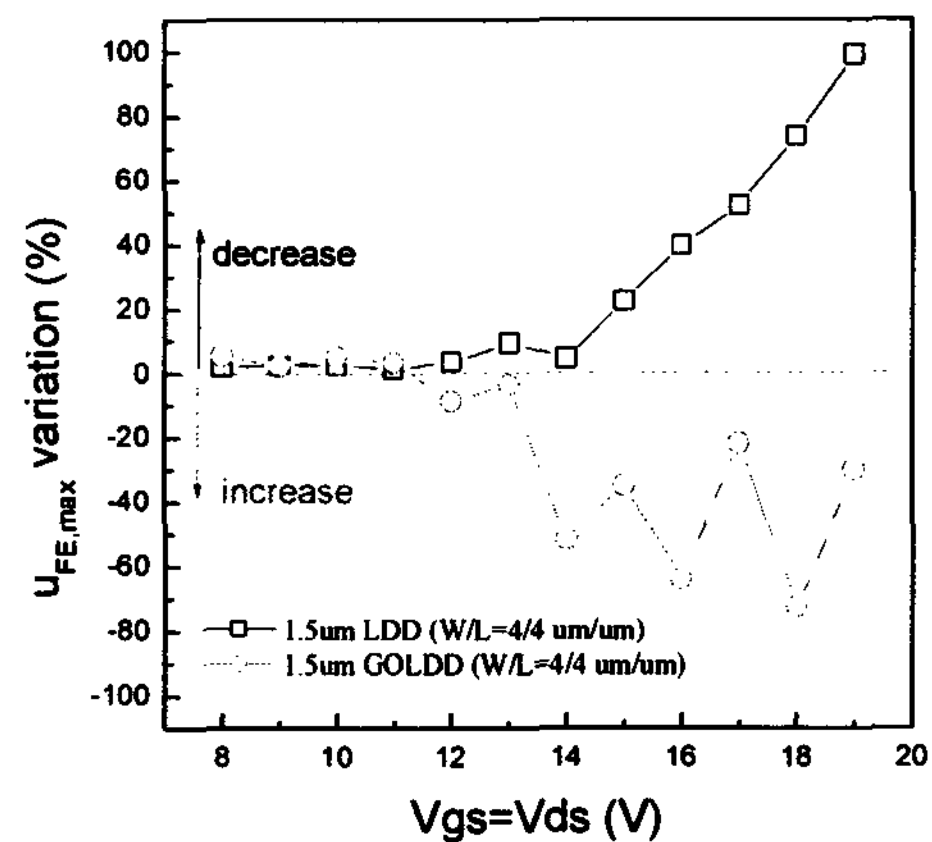


Figure 4. Maximum field effect mobility variation as a function of stress conditions in the LDD TFTs and the GOLDD TFTs

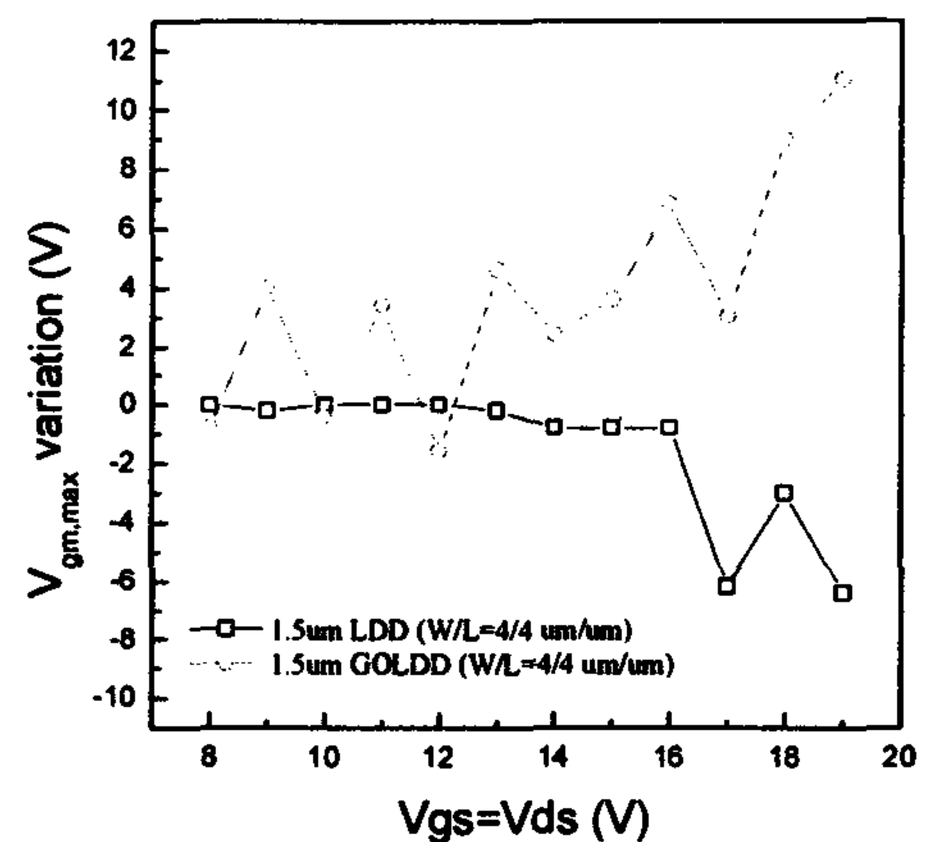


Figure 5. $V_{gm,max}$ variation as a function of applied bias conditions in the LDD TFTs and the GOLDD TFTs

Figure 4 shows field effect mobility variation as a function of stress voltages for the LDD TFTs and the GOLDD TFTs. It is noted that the mobility in the GOLDD TFTs increases with the applied stress voltages. This anomalous increase of mobility in the GOLDD structure is due to the increase of the gate voltage at which the maximum field effect mobility is obtained as shown in the Figure 5. This means that the field effect mobility rather degrades more severely after stress in the GOLDD TFTs.

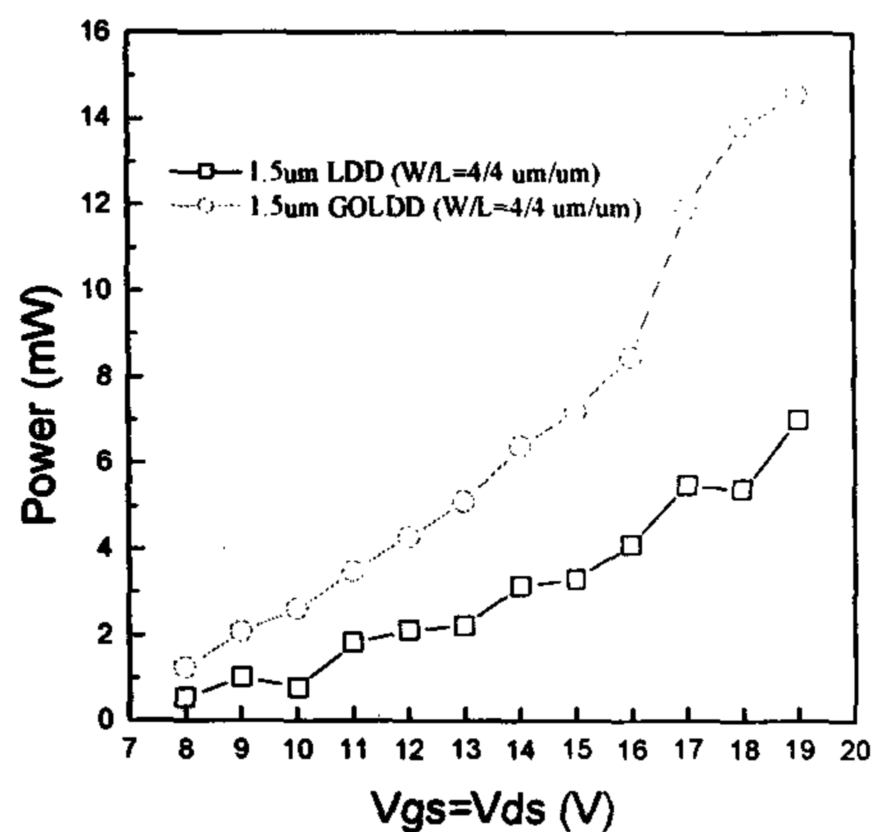


Figure 6. Stress power variation as a function of applied bias conditions in the LDD TFTs and the GOLDD TFTs

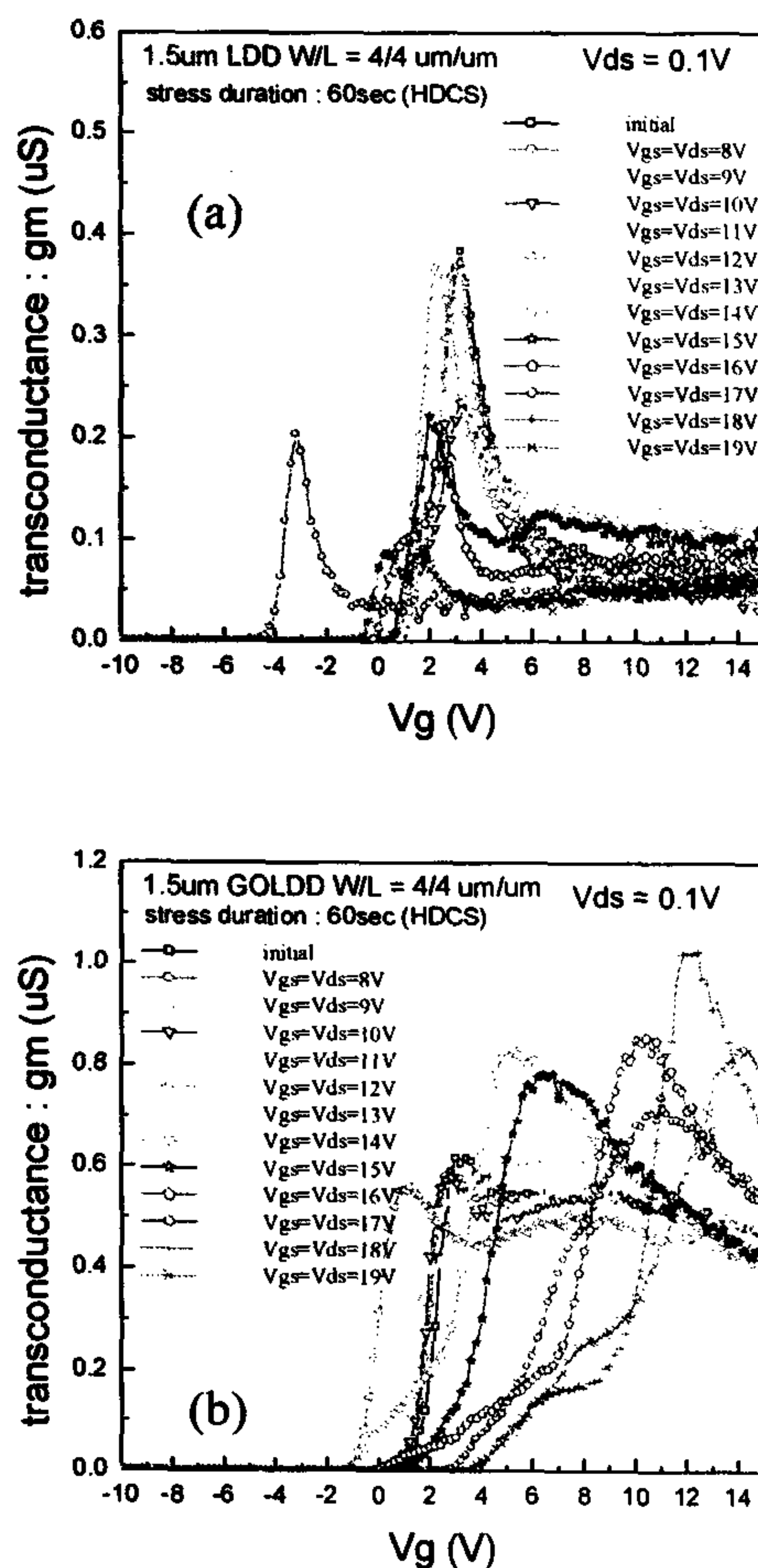


Figure 7. Transconductance variation as a function of applied bias conditions in (a) LDD TFTs and (b) GOLDD TFTs

The increase of the gate voltage at which the maximum field effect mobility is obtained after stress in the GOLDD TFTs can be explained by much severe self-heating-induced degradation of this structure. As shown in Figure 6, the power density in the GOLDD TFTs is higher than that in the LDD TFTs because of their larger current drivability, which degrades transconductance of the GOLDD TFTs much severely in the relatively low V_{gs} region. The transconductance degradation in the LDD TFTs and the GOLDD TFTs is shown in the Figure 7 (a) and (b), respectively, which supports the self-heating-induced mobility degradation in the GOLDD TFTs.

4. Conclusion

A GOLDD structure showed better HCS stability than a conventional LDD one. On the other hand, HDCS at V_{gs} = V_{ds} conditions caused much severe device degradation in the GOLDD structure because of its higher applied power density. It is suggested that self-heating-induced mobility degradation in the GOLDD TFTs be suppressed for using this structure in short-channel devices.

5. References

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