High Performance and Low Cost Single Switch Energy Recovery Display Driver for AC Plasma Display Panel

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Abstract— **A new high-performance and low cost single switch energy recovery display driver for an AC plasma display panel (PDP) is proposed. Since it is composed of only one auxiliary power switch, two small inductors, and eight diodes compared with the conventional circuit consisting of four auxiliary power switches, two small inductors, eight power diodes, and two external capacitors, it features a much simpler structure and lower cost. Nevertheless, since the root-mean-square (RMS) value of the inductor current is very small, it also has very desirable advantages such as a low conduction loss and high efficiency. Furthermore, there are no serious voltage-drops caused by the large gas-discharge current with the aid of the discharge current compensation, which can also greatly reduce the current flowing through power switches and maintain the panel to light at a lower sustaining voltage. In addition, all main power switches are turned on under the zero-voltage switching (ZVS) and thus, the proposed circuit has a improved EMI, increased reliability, and high efficiency. Therefore, the proposed circuit will be well suited to the wall hanging PDP TV. To confirm the validity of the proposed circuit, circuit operations, features, and design considerations are presented and verified experimentally on a 6-inch PDP, 50kHz-switching frequency, and sustaining voltage 141V based prototype.**

1. Introduction

The recent interest in flat panel display devices has made a plasma display panel (PDP) become a promising candidate for the conventional cathode ray tube (CRT) display, because a PDP is praised for its large screen size, wide viewing angle, thinness, and high contrast [1-8].

The AC-PDP is composed of addressing, sustaining (X), and scanning (Y) electrodes as shown in Fig. 1. The parallel display electrodes (i.e. X and Y electrodes) of 480 pairs, composed of transparent electrodes and bus electrodes, are formed on the front glass substrate. And, a dielectric layer and protection layer (MgO) are deposited on them. The addressing electrodes of 2556 lines (852 X 3 colors) orthogonal to display electrodes are formed on the rear glass substrate. The stripe barrier ribs are located between these addressing electrodes to separate each discharge cell. Three-color phosphors (i.e. red, green, and blue) are individually printed between barrier ribs. The space between two-glass substrates is filled with a Ne and Xe gas mixture. Therefore, an AC high voltage will ionize the gas to create the plasma. Then, the ultraviolet rays from the plasma excite phosphors to emit the visible light.

In general, PDPs are driven by the Address Display Separated (ADS) method as shown in Fig. 2. In this method, the PDP operation is composed of three intervals: the reset, address, and sustain periods [7, 8]. During the reset-period, all of the PDP cells are erased and prepared to carry out the address-operation by forming adequate wall charges. Then, during the address-period, selective write-discharges are ignited to form a required image by applying data and scan pulses to the addressing and scanning electrodes, respectively.

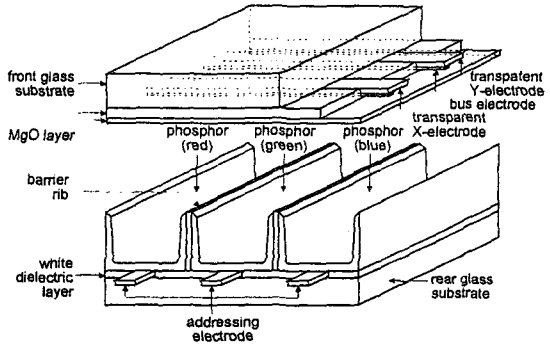

Fig. 1 Simplified sectional view of a three-electrode type surface discharge 42 inch AC PDP

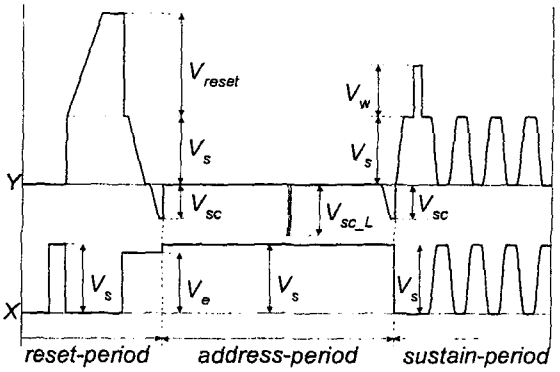

Fig. 2 Voltage waveforms applied to X and Y electrodes in ADS driving method

Since address-discharge itself emits an insufficient visible light, AC high-voltage square-wave pulses, which are generated by the sustain circuit, are continuously applied between sustaining and scanning electrodes for the strong light emission of selective cells.

To generate these AC high-voltage sustain pulses and process the required gas discharge current in the AC PDP, a well-known simple full bridge inverter (i.e. sustain circuit) is generally adopted to convert a dc voltage to a high frequency ac voltage. However, as mentioned above, the PDP is be regarded as a capacitor load C_p. Therefore, when

applying an ac high voltage and high frequency squarewave pulses with the amplitude of V_s between X and Y electrodes, an undesirable energy loss of $2C_pV_S^2$ for each cycle is generated in the non-ideal resistance of circuits and PDP during charging or discharging interval without an energy recovery circuit. Furthermore, the excessive surge charging and discharging currents will give rise to EMI noises and increase the surge current ratings of switches. Therefore, the high cost and low performance semiconductor devices should be used in this sustain circuit, which not only degrades the overall system efficiency but also causes a severe ringing in the panel voltage waveforms [1-7].

To relieve these problems, several prior ERCs have been proposed [1-3]. The prior circuit shown in Fig. 3 features a high efficiency and good circuit flexibility. Although it can recover most of the lost energy, it still has several fatal drawbacks. First, since its same two large auxiliary ERCs on both sides of the PDP are composed of four active power switches, eight power diodes, two inductors, and two external capacitors, the cost of production is high and the system is complex and bulky. Secondly, the energy-recovery capacitors are charged and discharged in a high frequency. As a result, the considerable heat generated by the equivalent series resistance (ESR) of energy recovery capacitors would shorten their lifetime. Therefore, several parallel-connected miler capacitors with the low ERS must be used instead of the electrolytic capacitor, which increases the cost of the production. Thirdly, since its auxiliary circuit usually handles large energy, it shows serious power dissipation and would require large heat sinks. Especially, the most serious problem of this circuit is a large voltage drop across the parasitic resistance of the circuit during gas discharge transients. Due to these undesirable voltage drops, the effective voltage applied to the PDP decreases, and so does the accumulated amount of the wall charge [4-6].

Another circuit proposed in [4] is very simple and has no above-mentioned voltage drop. However, its fatal problem is a very large circulating current that comes up to the value of the gas discharge current (i.e. 150A for 42-in PDP). Therefore, its excessive conduction loss degrades the overall system efficiency and a considerable heat generated by this current would require a large cooling system. In a real implementation, it is impossible to employ this Hsu circuit to the commercial PDP TV.

To overcome all these drawbacks, a new high-performance and low cost display driver for an ac plasma display panel (PDP) is proposed as shown in Fig. 5 (b). Since it has only one power switch, two inductors, and eight diodes instead of the large auxiliary circuit, the proposed circuit has significant advantages such as a simpler structure, less mass, lower cost of production, and fewer power devices. Furthermore, it features no serious voltage drops caused by the large gas discharge current with the aid of the discharge current compensation. Thus, its operational voltage margin is more improved and it helps to reduce the transition time of panel voltage polarity, which may produce more stable light waveforms. In addition, its circulating current is very small and the main power switches are all turned on with ZVS. Therefore, its overall system efficiency is very high and the burden on the cooling system is very light.

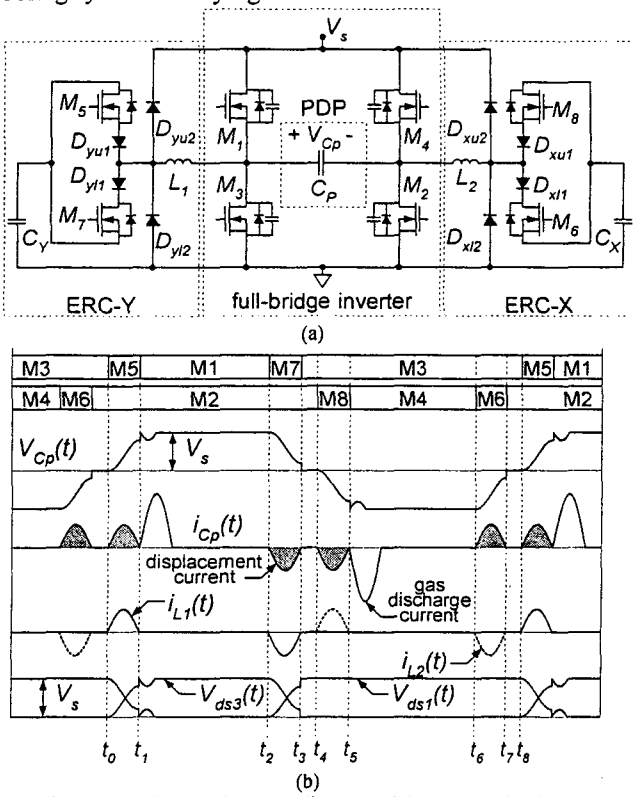

Fig. 3 Weber circuit (a) Schematic diagram of the Weber circuit (b) Key waveforms of the Weber circuit

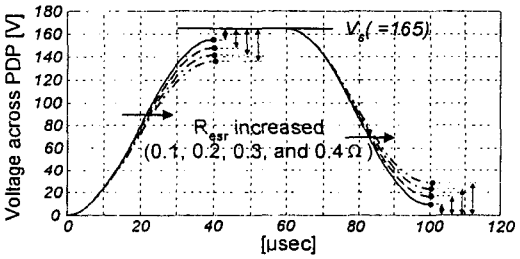

Fig. 4 Theoretical panel voltage waveforms of the prior circuit: V_s=165V, V_{on}=1.3V, C_p=80nF(42-inch PDP), rising time=0.4usec, L_1=L_2=0.2uH.

2. Review of Prior Circuit

Figs. 3 (a) and (b) show the schematic diagram of the Weber circuit and its key waveforms during the hereafter-described sustain-period.

One cycle period of the prior circuit is divided into two half cycles, t_0~t_4 and t_4~t_8. Because the operational principles of two half cycles are symmetric, only the first half cycle is explained. Before t_0, the voltage v_{Cp} across C_p is maintained to 0V with M_2 and M_3 conducting.

Mode 1 (t_0-t_1): When M3 is turned off and M5 is turned on at t_0, mode 1 begins. With the initial conditions of $v_{Cp}(t_0)$=0V, $v_{ds1}(t_0)$=V_s, $v_{ds3}(t_0)$=0V, and $i_{L1}(t_0)$=0A, a series resonance between C_1+C_3+C_p and L_1 occurs as follows:

$$v_{ds1}(t) = V_S - \left(\frac{V_S}{2} - V_{on}\right)\left\{1 - e^{-t/\tau}\left(\cos\omega t + \frac{1}{\omega\tau}\sin\omega t\right)\right\} \quad (1)$$

$$v_{Cp}(t) = v_{ds3}(t) = \left(\frac{V_S}{2} - V_{on}\right)\left\{1 - e^{-t/\tau}\left(\cos\omega t + \frac{1}{\omega\tau}\sin\omega t\right)\right\} \quad (2)$$

where $\tau=2L_1/R_{esr}$, R_{esr}=parasitic resistance of the circuit, V_{on}=forward voltage drop of the diode, $\omega=[1/\{L_1(2C_{oss}+C_p)\}-1/\tau^2]^{0.5}$, and switch output capacitor $C_1=C_3=C_{oss}$. Based on equation (2), the voltage waveform across the PDP can be plotted as shown in Fig. 4.

After a half cycle resonance between L_1 and $C_1+C_3+C_p$, the voltages across C_1, C_3, and C_p become V_s-(V_s/2-V_{on})(1+$e^{-\pi/(\omega\tau)}$), (V_s/2-V_{on})(1+$e^{-\pi/(\omega\tau)}$), and (V_s/2-V_{on})(1+$e^{-\pi/(\omega\tau)}$), respectively.

Mode 2 (t_1-t_2): After a half cycle resonance between L_1 and $C_1+C_3+C_p$, mode 2 begins at t_1. When M1 is turned on to sustain C_p at V_s, the voltage difference as high as V_s-(V_s/2-V_{on})(1+$e^{-\pi/(\omega\tau)}$) between C_p and input source V_s causes a serious hard switching of M1, resulting in an excessive surge current. At the same time, since the voltage across the PDP reaches the gas-discharge firing voltage and the subsequent large gas-discharge current (about 150A for 42-inch PDP) flows, serious voltage drops across the switching elements and the parasitic resistance of the circuit are generated as shown in Fig. 3 (b).

Furthermore, since this voltage drop can cause a serious voltage notch across the PDP as shown in Fig. 3 (b), the effective voltage applied to the PDP decrease and so does the accumulated amount of wall charge.

Mode 3 (t_2-t_3): When M1 is turned off and M7 is turned on at t_0, mode 3 begins. With the initial conditions of $v_{Cp}(t_0)=V_s$, $v_{ds1}(t_0)=0$, $v_{ds3}(t_0)=V_s$, and $i_{L1}(t_0)=0$A, a series resonance between $C_1+C_3+C_p$ and L_1 occurs as follows:

$$v_{ds1}(t) = V_S - \left(\frac{V_S}{2} - V_{on}\right)\left\{1 - e^{-t/\tau}\left(\cos\omega t + \frac{1}{\omega\tau}\sin\omega t\right)\right\} \quad (3)$$

$$v_{Cp}(t) = v_{ds3}(t) = \left(\frac{V_S}{2} + V_{on}\right) + \left(\frac{V_S}{2} - V_{on}\right)e^{-t/\tau}\left(\cos\omega t + \frac{1}{\omega\tau}\sin\omega t\right). \quad (4)$$

Based on equation (4), the voltage waveform across the PDP can be plotted as shown in Fig. 4. After a half cycle resonance between L_1 and $C_1+C_3+C_p$, the voltages across C_1, C_3, and C_p become (V_s/2-V_{on})(1+$e^{-\pi/(\omega\tau)}$), (V_s/2+V_{on})-(V_s/2-V_{on})$e^{-\pi/(\omega\tau)}$, and (V_s/2+V_{on})-(V_s/2-V_{on})$e^{-\pi/(\omega\tau)}$, respectively.

Mode 4 (t_3-t_4): After a half cycle resonance between L_1 and $C_1+C_3+C_p$, mode 4 begins at t_4. When M3 is turned on to sustain C_p at 0V, the voltage difference as high as (V_s/2+V_{on})-(V_s/2-V_{on})$e^{-\pi/(\omega\tau)}$ between C_p and ground 0V as shown in Fig. 3(b) and Fig. 4 causes a serious hard switching of M3, resulting in an excessive surge current. These facts imply that the increase in the parasitic resistance and diode forward voltage drop causes a serious hard switching operation, subsequent excessive surge current, serious power dissipation, EMI problem, and poor energy-recovery capability.

To solve these problems, it is necessary to reduce the parasitic component by designing the circuit board optimally as well as choosing switching devices with the small on-resistance and low forward voltage drop. However since it is impossible to get rid of parasitic components completely, above-mentioned problems are inevitable.

3. Proposed Circuit

Fig. 5 (a) show the block diagram of the whole AC PDP driver equipped with the proposed circuit in the address-display-separated (ADS) driving method, respectively. Figs. 5 (b) and (c) show the electrical equivalent circuit diagram and key waveforms of the proposed circuit, respectively. One cycle period of a proposed circuit is divided into two half cycles, t_0~t_3 and t_3~t_6.

Because the operation principles of two half cycles are symmetric, only the first half cycle is explained. Before t_0, the voltage v_{Cp} across C_p is maintained to V_s with M_1 and M_2 conducting as shown in Fig. 6 (a).

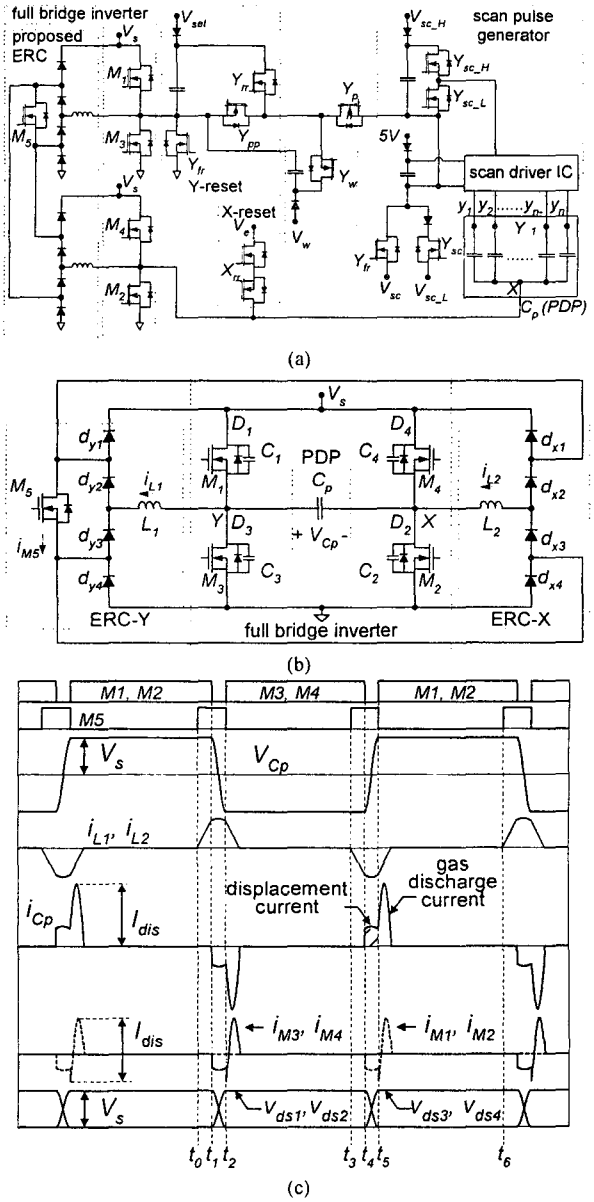

Fig.5 Proposed circuit (a) Block diagram of the whole AC PDP driver equipped with the proposed circuit (b) Electrical equivalent circuit diagram of the proposed circuit during sustain-period (c) Key waveforms of the proposed circuit

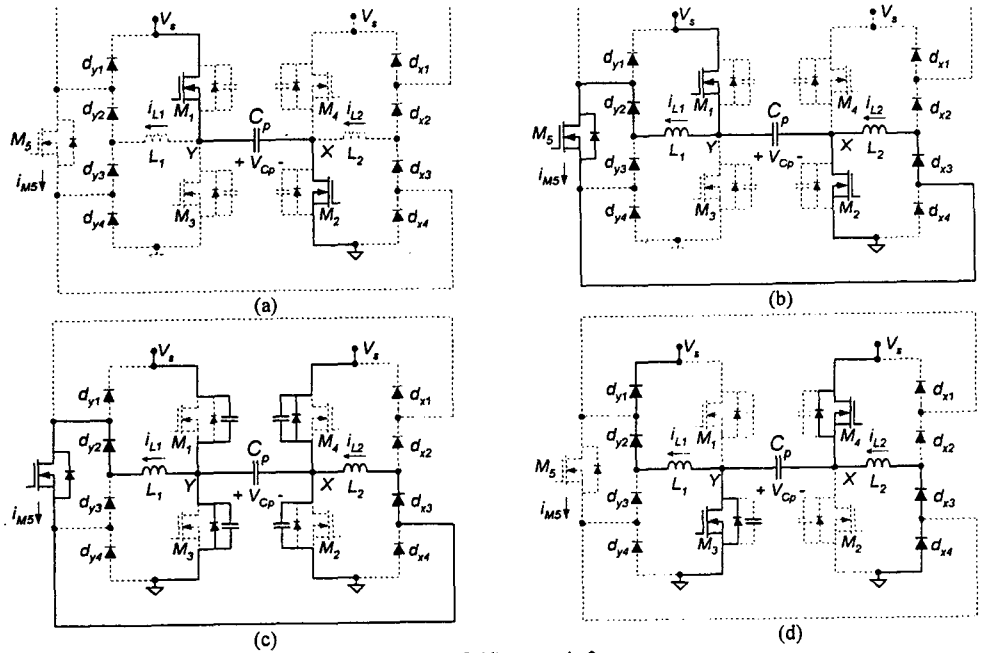

Fig. 6 Operation circuit diagram (a) Before t_0 (b) At mode 1 (c) At mode 2 (d) At mode 3

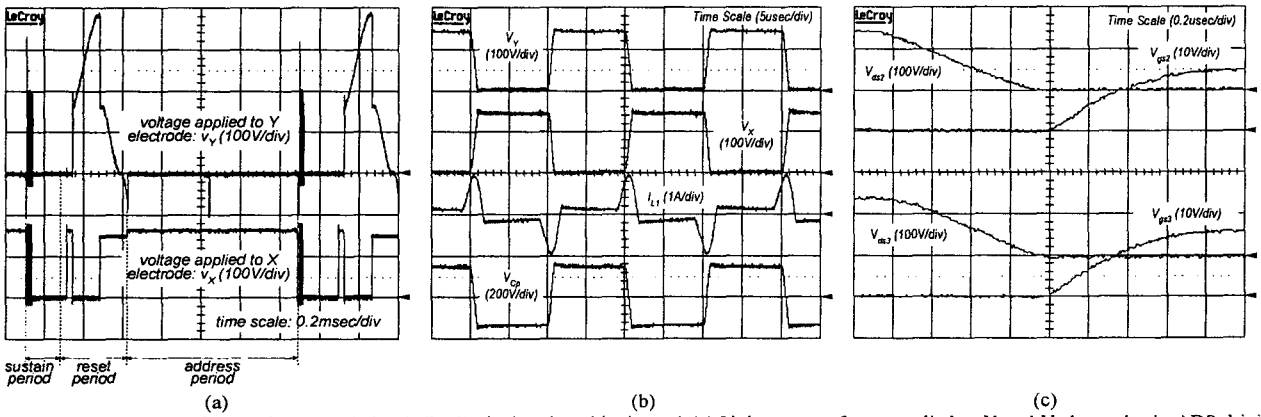

Fig. 7 Experimental waveforms of proposed circuit (In displaying the white image) (a) Voltage waveforms applied to X and Y electrodes in ADS driving method (b) Voltage waveforms across X, Y, and PDP and current waveform through L (c) ZVS turn on transients of M_1 and M_3

Mode 1 (t_0-t_1): When M_5 is turned on at t_0, mode 1 begins and the input voltage V_s is applied to the serially connected L_1 and L_2 with M_1, M_2, M_5, d_3, and d_4 conducting as shown in Fig. 6 (b). Thus, i_{L1} and i_{L2} increase linearly with the slope of $0.5V_s/L$ as followings

$$i_{L1}(t) = i_{L2}(t) = \frac{V_S}{2L}(t - t_0) \tag{5}$$

where it is assumed that the values of L_1 and L_2 are equal to L.

Mode 2 (t_1-t_2): When M_1 and M_2 are turned off at t_1, mode 2 begins. As shown in Fig. 6 (c), with the initial conditions of $i_{L1}(t_1)$= $i_{L2}(t_1)$=I_L=$0.5V_s(t_1$-$t_0)$/ L and $v_{Cp}(t_1)$=V_s, i_{L1} and i_{L2} start to charge the PDP, C_1, and C_2 and discharge C_3 and C_4 as follows:

$$V_{Cp}(t) = V_S - \frac{I_L}{C_{OSS} + C_P}(t - t_1) \tag{6}$$

where it is assumed that C_1, C_2, C_3, and C_4 are equal to C_{oss} and L_1 and L_2 act as a current source with the value of I_L. With this arrangement, the abrupt charging and discharging operations of C_p are avoided and the voltage across C_p is decreased toward $-V_s$.

Mode 3 (t_2-t_3): When v_{Cp} is clamped at $-V_s$, V_Y gets to V_s, and V_X drops to 0V at t_2, mode 3 begins. Since the voltages, V_{ds3} and V_{ds4}, across M_3 and M_4 are 0V, M_3 and M_4 can be turned on with ZVS as shown in Fig. 6 (d). Moreover, since the inductor currents, i_{L1} and i_{L2}, compensate a large portion of the plasma discharge current I_{dis} during this period, the plasma discharge current through M_3 and M_4 are considerably reduced as shown in Fig. 5 (c). Therefore, the voltage drops across the parasitic resistances are not serious and the wall charges are well accumulated. After M_5 are turned off, the inductor currents begin to decrease linearly with the slope of $-V_s/L$ and the energy stored in the inductors is fed back to the input power source.

The circuit operation of t_3-t_6 is similar to that of t_0-t_3. Subsequently, the operation from t_0 to t_6 is repeated.

4. Design Considerations

Since the brightness of a PDP is proportional to the operation frequency, the rising times, t_1-t_2 and t_4-t_5, are required to be as short as possible. The interval t_1-t_2 (or t_4-t_5) is the desired rising time, and C_p and C_{oss} are as known values. Thus, the values of L_1 and L_2 can be determined from equations (1) as follows:

$$L_1 = L_2 = \frac{(t_2 - t_1)(t_1 - t_0)}{4(C_P + C_{OSS})} \quad (7)$$

where L_1 and L_2 include the parasitic line inductance.

5. Experimental results

The prototype proposed ERC is implemented with specifications of L_1 = L_2 = 97uH, C_p = 2nF (6-inch PDP), M_1, M_2, M_3, and M_4 = 2SK2995, gate driver IC = IR2110, switching frequency = 50kHz, and V_s=141V. Fig. 7 shows the experimental results of the proposed circuit, when the white image is displayed. Fig. 7 (a) shows the voltage waveforms applied to X and Y electrodes during each period. This well coincides with aforementioned theoretical ADS waveforms.

As can be seen in Fig. 7(b), the current source built in the inductor completely charges the panel capacitor C_p to V_s or $-V_s$ with no serious voltage notch across the PDP. Since it compensates the large amount of plasma discharge current, the current through and the voltage drop across the power switch are considerably reduced respectively, which will attract more wall charge to deposit on the dielectric layer of the electrodes. In other words, the wall voltage is larger, and it helps the panel maintain to display the white image at lower voltage such as 141V compared with about 165V for prior circuit.

Furthermore, since the current through the inductor flows only when charging or discharging C_p, its circulating energy and conduction loss are very small. Fig. 7(c) shows that M_2 and M_3 are turned on after V_{ds2} and V_{ds3} drop to 0V, that is, ZVS of M_2 and M_3 is achieved. M_1 and M_4 are also turned on with ZVS. Fig. 8 shows that the input current is smallest at L_1= L_2=97uH and the smaller inductor can maintain the panel to display the white image at the lower sustaining voltage with the more effect of the discharge current compensation.

As can be seen in Table I, the number of devices used in the proposed circuit is less than that in the Weber circuit due to the simple auxiliary circuit. Therefore, it features a simpler structure, less mass, and lower cost of production.

Table I. The number of devices used to drive 6-inch PDP

		Weber circuit	Proposed circuit
power switch	M1, M4	2SK2995:2(EA)	2SK2995:2(EA)
	M2, M3	2SK2995:2(EA)	2SK2995:2(EA)
	auxiliary circuit	2SK2995:8(EA)	2SK2995:1(EA)
energy-recovery inductor: L_1, L_2		8.1uH:2(EA)	97uH:2(EA)
power diode		F10KF40:8(EA)	F10KF40:8(EA)
gate driver IC		IR2110:4(EA)	IR2110[1]:2(EA) IR2118[2]:1(EA)
external capacitor: C_x, C_y		2.2uF/150V:4(EA)	0(EA)

[1] high and low side driver having one floating channel. [2] single floating channel driver.

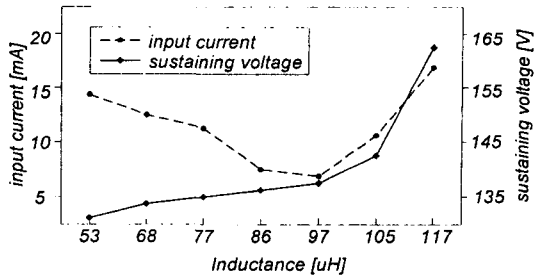

Fig. 8 Measured input current and sustaining voltage according to L_1(=L_2)

6. Conclusion

A new high-performance and low cost single switch energy recovery display driver for an AC plasma display panel (PDP) has been presented to overcome the drawbacks of prior circuits. Since it has only one auxiliary power switch, two small inductors, and eight diodes, it features a much simpler structure and lower cost. Its circulating energy is very small and the main power switches are all turned on with ZVS. Therefore, it features a high efficiency and the burden on the cooling system is very light. In particular, since it compensates the plasma discharge current, it could solve the problem of the undesirable voltage drop, which enables the panel to light at lower voltage than the prior circuit. Additionally, the inductor current helps to reduce the transition time of the panel polarity. Therefore, this proposed circuit is expected to be well suited for hang-on-the-wall.

Acknowledgement

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