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High Performance MRAM

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Abstract

For a high performance memory, density, speed, and power are of most concerns to replace conventional memories, such as SRAM, Flash and DRAM. In this talk, an MRAM cell with pillar write word line (PWWL) is adopted to reduce the switching current by approximately a factor of 2. In addition, a memory cell comprising one transistor and two uneven MTJs (1T2UMTJ) is implemented to achieve both high packing density of 6 F^2 bit size and high reading speed and throughput of less than 100 ns for two sharing bits. The 1T2UMTJ structure may be feasible for double data rate (DDR) application.

In this talk, the reading margin for the Mb-level capacity is firstly investigated. The R_{max}-R_{min} separation of 25 σ_0 and MR ratio of 37% for CoFeB single free layer at 0.3 V was achieved. Secondly, the switching behaviors on both single free layer and SAF free layer will be evaluated. The kink phenomenon on R-H loops were observed and discussed by defect injection on MTJ cells from micro-magnetic simulation. The write operation characteristics on single free layer will be then displayed. Finally, the promising toggle switch with lowered spin-flop field and wide current range will be also presented.

Reference

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