강유전체 메모리용 $Bi_{3.3}Eu_{0.7}Ti_3O_{12}$ 박막의 증착과 전기적 특성

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Preparation and Electrical Properties of Ferroelectric $Bi_{3.3}Eu_{0.7}Ti_3O_{12}$ Thin Films for Memory Applications

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Abstract : Ferroelectric Eu-substituted $Bi_4Ti_3O_{12}$ (BET) thin films with a thickness of 200 nm were deposited on Pt(111)/Ti/SiO_2/Si(100) substrate by means of the liquid delivery MOCVD system and annealed at several temperatures in an oxygen atmosphere. At annealing temperature above 600 °C, the microstructure of layered perovskite phase was observed. The remanent polarization of these films increased with increase in annealing temperature. The remanent polarization values ($2P_r$) of the BET thin films annealed at 720 °C were 37.71 μC/cm² at an applied voltage of 5 V.

Key Words : Eu-substituted $Bi_4Ti_3O_{12}$, liquid delivery MOCVD, microstructure

1. Introduction

Ferroelectic thin films have been investigated for applications in ferroelectric random access memories (FeRAMs).[1] FeRAMs have advantages of rapid response of polarization switching, low power consumption and long lifetime of 10^{12} read/write cycles. These strengths have led to the application of FeRAMs in small devices, such as smart cards, personal digital assistants and future personal computers. For the practical application of FeRAMs, large remanent polarization, low coercive field, fatigue-free behavior and low process temperature are required.[2,3]

Lead zirconium titanate (PZT) and strontium bismuth tantalite (SBT) are used for non-volatile ferroelectric memory devices. However, fatigue in PZT and high temperature processing and low polarization in SBT suggests the investigation for other suitable ferroelectric materials.[4,5]

Recent studies revealed that Bi^{3+} ions in BIT structure could be substituted by trivalent lanthanide ions (La^{3+}, Nd^{3+}, Sm^{3+}, Eu^{3+} and Pr^{3+}), and their ferroelectric properties were in the reasonable ranges for memory applications. Lanthanide-substituted BIT thin films are attractive lead-free materials for memory applications because of their relatively large remanent polarization and fatigue-free characteristics.[6]

In this study, we prepared Eu-substituted $Bi_4Ti_3O_{12}$ (BIT) thin films by means of the liquid delivery MOCVD system. After deposition of the ferroelectric thin films, the effect of the substrate temperature and the reactor pressure on the composition were investigated. In addition, the microstructure and the dielectric and electrical properties of the thin films were determined.

2. Experimental

A single mixture solution of $Bi(ph)_3$, $Eu(TMHD)_3$ and $Ti(O^iPr)_2(TMHD)_2$ precursors was prepared to be used in liquid delivery MOCVD. The precursors were dissolved together in n-butyl acetate. BET thin films were deposited on a Pt(111)/Ti/SiO_2/Si(100). Thereafter, the films were annealed at various temperatures in oxygen ambient for 1h. and post-annealed in oxygen ambient for 30 min., thereafter the deposition of a Pt top electrode with a diameter of 200 μm, in order to enhance the electrical properties of the thin film. The thermal stability of the BET precursors was confirmed by TG analysis. The composition of the films was measured by EPMA (JEOL, JXA-8900R). The crystallinity and microstructure of the films were analyzed by XRD (Rigaku, DMAX2500) and SEM (Hitachi, S-4200), respectively. The ferroelectric properties were measured with a standardized ferroelectric tester (Radiant Technologies Inc, RT-66A).

Typical deposition conditions are summarized in Table 1.

Table 1. MOCVD process conditions used to deposit BET thin films.

Deposition parameters	Range Investigated
Substrate Temperature	540 - 600 °C
Total reactor pressure	3 - 6 Torr
Vaporizer Temperature	200 - 220 °C
Carrier gas flow rate	200 sccm
Oxidizing gas flow rate	200 sccm
Stock solution conc.	0.05:0.01:0.05 [Bi:Eu:Ti]

3. Results and discussion

Fig. 1 shows the XRD patterns of the BET thin films with different annealing temperatures from 600 to 720 °C. The BET thin films crystallized into a layered perovskite phase after annealing. Annealing above 600 °C. resulted in well-saturated BET thin films. As the annealing temperature of the BET thin films were increased from 600 to 720 °C, the peaks in the XRD patterns became sharper. The BET thin films obtained exhibit a polycrystalline structure, with no pyrochlore phase or preferred orientation observed. This indicates that the Eu^{3+} ions can readily substitute for Bi^{3+} ions in this pseudo-perovskite structure.

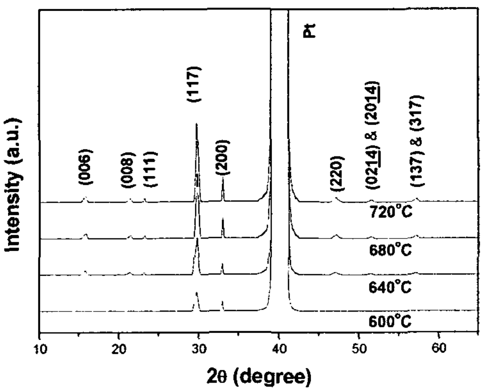

Fig. 1. XRD patterns of BET thin films.

The surface morphology of the BET thin films was recorded by SEM. As shown in Fig. 2, the average grain size of the BET thin films annealed at 720 °C ranged from 0.1 to 0.2 μm. The grain size of the films increases with increasing annealing temperature. It is assumed that crystal growth was enhanced, and thus that the ferroelectric properties of the films can be improved by increasing the temperature.

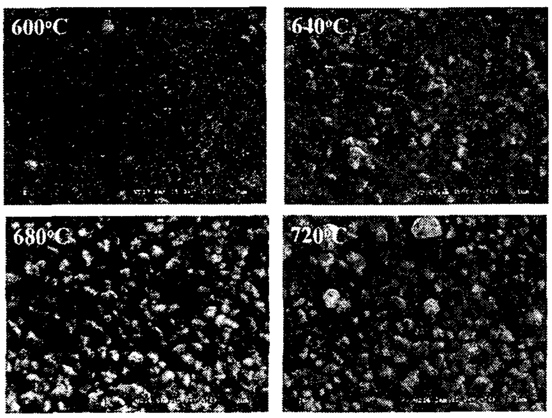

Fig. 2. SEM images of BET thin films annealed at various temperatures.

Ferroelectric hysteresis loops of BET thin film capacitor annealed at the temperature range from 600 to 720 °C are shown in Fig. 3. As presented in Fig. 3, the BET thin film capacitor is characterized by well-saturated polarization -electric field (P-E) curves with increasing annealing temperature. The $2P_r$ and $2V_c$ values of the BET thin film annealed at 720 °C were 37.71 $\mu C/cm^2$ and 2.46, respectively, at an applied voltage 5V.

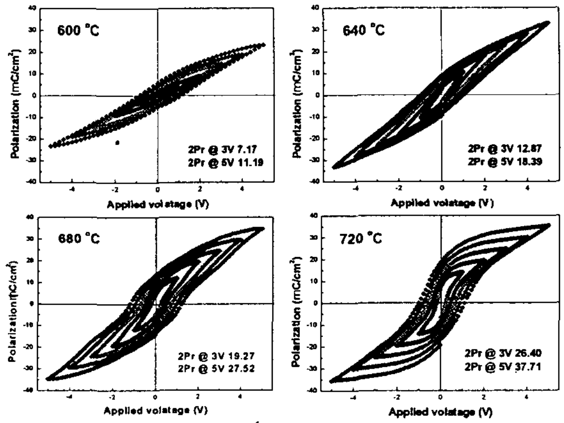

Fig. 3. Hysteresis loops of BET thin films annealed at various temperatures.

4. Conclusion

Europium-substituted bismuth titanate, $Bi_{3.3}Eu_{0.7}Ti_3O_{12}$, thin films were successfully grown on Pt(111)/Ti/SiO_2/Si(100) substrates by means of liquid delivery MOCVD system. The BET thin films showed good ferroelectric properties and low anneal temperature that could satisfy the requirements for high-density complementary metal oxide semiconductor (CMOS) devices. As a results, it indicates that the BET thin films are new candidates for non-volatile ferroelectric random access memory for integration in CMOS structures.

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