Application of Organic TFTs to Flexible AMOLED Display Panel

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Abstract

We fabricated an array consisting of organic TFTs (OTFT) and organic LEDs (OLED) in order to demonstrate the possible application of OTFTs to flexible active matrix OLED (AMOLED). The panel was composed of 64 x 64 pixels on 4 inch size poly-ethylene-terephehalate (PET) substrate in which each pixel had one OTFT integrated with one green OLED. The panel successfully displayed some letters and pictures by emitting green light with a luminance of 1.5 cd/m^2 at 6 V, which was controlled by the gate voltage of OTFT.

1. Introduction

The flexible AMOLED is attracting much attention because it enables a lighter and thinner display [1, 2]. In addition, large area displays can be made cheaply because of the low temperature process used and their possible roll-to-roll manufacturing. However, the flexible AMOLED display is at the proof-of-concept stage for conformable and rollable displays.

For the flexible AMOLED, the driving transistors, which should be able to supply sufficient current to OLED, should have high compatibility with plastic substrate. At present, three types of transistors such as low-temperature poly-silicon TFT and amorphous silicon TFT and organic thin film transistor (OTFT) are available for flexible AMOLED. Among them OTFTs exhibited the highest compatibility to plastic substrate because of their low temperature (~ 100^{o}C) process [3]. OTFTs have recently been well developed to exhibit mobility of ~ 5 cm^2/V.sec at the discrete-device level[4].

Several groups are working on flexible AMOLED. DuPont and Honeywell demonstrated flexible AMOLED using a-Si on glass as well as plastic substrate [5]. Lehigh University also fabricated flexible AMOLED on stainless substrate using poly-Si [6] and Philips chose polymer TFT to drive E-ink [7]. A meaningful result about AMOLED panel using pentacene TFTs was reported by Pioneer group but the substrate was not plastic but glass, and the gate was also an inorganic material such as Ta_2O_5 [8]. And we have presented the preliminary results about integration of pentacene TFTs with OLEDs on PET substrate [9]. To our knowledge, flexible AMOLED panels driven by organic TFTs with a large scale such as the panel in this paper have not yet been reported.

In the work reported here, we fabricated an array of 64 x 64 pixels on 4 inch size poly-ethylene-terephehalate (PET) substrate in which each pixel was composed of one OTFT and one OLED. The purpose of this panel was to investigate the current driving capability of OTFTs for OLEDs and to develop the fabrication process for flexible AMOLED. The OTFTs used poly(4-vinylphenol) (PVP) for gate insulator and pentacene for organic semiconductor. For OLED, two layers of Alq3 and TPD were employed to generate green light. In this letter we will discuss the fabrication process and operation results of the array considering the possible application of OTFTs to flexible AMOLED.

2. Experimental

A. Pentacene TFTs with PVP Gate Insulator

PVP has been used for a gate of OTFT on a Si substrate [10]. However, in our work, PVP process was developed for PET substrate. The PVP organic gate material consisted of PVP polymer and cross-link agent (CLA), and propylene glycol monomethyl ether acetate (PGMEA) as a solvent. We found that the optimum ratio of components was 10wt% of PVP mixed with 5wt% of CLA in 100wt% of PGMEA in terms of mobility and on/off current ratio. The CLA was activated by thermal heating and the optimum temperature was found by considering the chemical resistance against acetone used for photoresist stripping. The thermally cross-linked PVP provided a hydrophobic surface with the contact angle of 61.9^o corresponding to a surface energy of 25 dyne/cm, compared with the non-cross-linked PVP polymer film which had the contact angle of 52.1^o and surface energy of 35 dyne/cm. The low surface energy of the cross-linked PVP supplied a good surface condition for well-ordering of pentacene molecules.

For the fabrication of array we need photolithography process in order to pattern the PVP gate. Thus, the PVP gate should be highly resistant to organic solvents used for the process, especially to acetone used for photoresist stripping. Considering the chemical resistance we found out the optimum baking temperature to be 200 °C. Before acetone treatment PVPs baked at the lower temperatures than 200 °C produced similar transfer characteristics to PVP baked at 200°C. However, after acetone treatment, PVPs baked at the lower temperatures were seriously degraded while PVP at 200°C was sustained. Therefore, we employed 200 °C baking process although the high temperature process was not preferable for plastic substrate. There was dimensional instability in the array due to the high temperature process but it was not serious because of sustenance of glass substrate to PET substrate. However, we need to develop a low temperature or non-thermal process with sufficient chemical resistance for the future roll-to-roll process.

Pentacene film was deposited by thermal evaporation. The deposition conditions strongly depend on the gate material on which pentacene is supposed to be deposited. For the PVP gate the optimum evaporation temperature and thickness of pentacene film were extracted. According to the model of pentacene film growth [11] the density of nucleation sites N_I is proportional to deposition rate F, which is controlled by evaporation temperature, such as $N_I \propto F/D$, where D is diffusion coefficient of molecules on gate surface. Therefore in order to obtain the small density of nucleation sites producing the large grains the small deposition rate F is required. However, there is a lower limit of deposition rate. Pentacene molecules should be deposited before the residual molecules in vacuum chamber are absorbed on the substrate. Therefore we found an optimum deposition rate by varying the evaporation temperature. The largest mobility of 1.2 cm^2/V·sec was obtained at 190 °C, and it was reduced as the temperature increased or decreased from 190 °C. The high deposition rate above 190 °C produced the large density of nucleate sites, resulting in small grain size and then low mobility, which was 0.3 cm^2/V·sec at 218 °C. At 188 °C the mobility was 0.9 cm^2/V·sec caused by pre-absorption of the residual molecules in the chamber.

The field effect mobility also depended on pentacene thickness. It was increased with thickness and reached a maximum value of 1.2 cm^2/V·sec at 50 nm thick. The low mobility of thinner than 50 nm was caused by the gaps existing between grains. These gaps were reduced as the thickness increased and completely filled at 50 nm, producing the high mobility. The detailed description about thickness dependence of mobility will be discussed elsewhere [12]. Therefore, in order to make a high performance display panel it is important to sustain pentacene thickness at 50 nm over the entire substrate and also to obtain the large grains by maintaining the temperature at 190 °C during the deposition period.

Using such an optimized PVP gate and pentacene deposition process on PVP gate, we fabricated pentacene TFTs on PET substrate. They produced mobility of 0.9 ± 0.3 cm^2/V.sec, a sub-threshold slope of 0.27 V/dec and an on/off current ratio of 1.2 x 10^6 as shown in Fig. 1. The overall performance was good enough for application to AMOLED display.

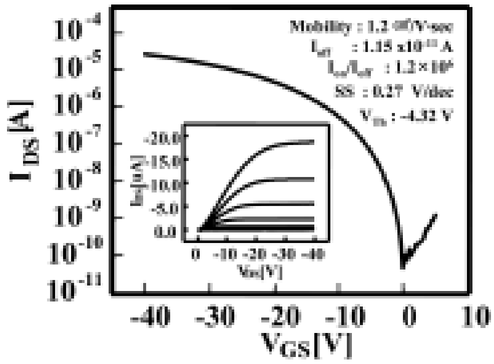

Figure 1. The electrical characteristics of pentacene TFTs using PVP gate on Plastic substrate

B. Fabrication of Array

We fabricated an array of OTFTs with a number of pixels of 64 x 64, in which each OTFT was integrated with one green OLED, on 4 inch size PET substrate with ITO electrode. The fabrication process was as follows. PET substrate was pre-shrunk for 1 hours at 200 °C and then attached on a glass to minimize the dimensional instability and to avoid being wrinkled during the subsequent thermal process. ITO on PET substrate was first patterned for the anode of OLED, and then an Al (50 nm) gate was deposited and patterned. Subsequently, PVP (300 nm) gate dielectric was deposited as described above and patterned by the conventional photolithography process. In this step, the edges of the anode were covered by a PVP layer to avoid the degradation caused by the edge field. Then pentacene (50 nm) was evaporated through a shadow mask, above which the source and drain electrodes (Au - 40 nm) were deposited through a shadow mask to complete the pentacene TFTs. For OLED, TPD (35 nm) and Alq3 (35 nm) were sequentially deposited followed by deposition of an Al (50 nm) cathode. Finally, an Al interconnection metal connected the drain of OTFT to cathode of OLED in order to avoid the cross of supply voltage lines over the source ground lines. The diagram of device cross section and the fabricated pixel were presented in Fig. 2, in which OTFT and OLED were placed side by side.

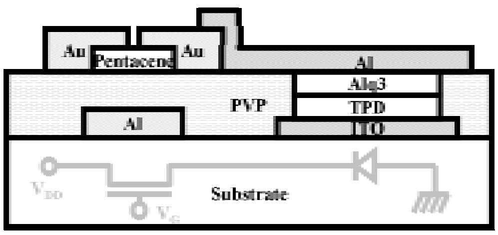

Figure 2. The pixel circuit and cross-sectional of the fabrication device

The mobility of OTFTs in array was reduced comparing with the discrete devices, it was relatively uniform with 0.5 cm^2/V·sec over the entire panel. The reduction of mobility around the edge area was estimated to be caused by contamination, non-uniformity of pentacene film.

We examined the driving capability of OTFT for OLED. An OLED with an area of 200 μm x 200 μm produced luminance of 1.5cd/m^2 at 6 V. Note that OTFTs should operate in saturation mode to provide a constant current to OLED so that the supply voltage should be larger than 19 V in this case. The OLED generated green light with a wavelength of 530 nm. They produced current density of 1.5 A/m^2, a luminous efficiency of 0.52 lm/W at 6 V as shown in Fig. 3.

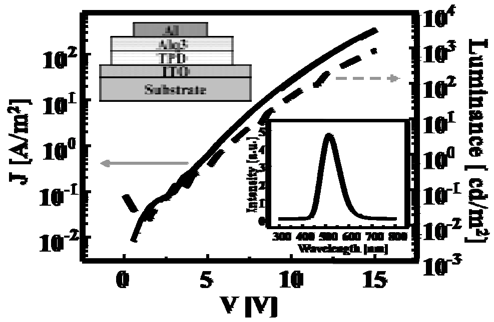

Figure 3. The electrical characteristics of OLED

The intensity of OLED was measured by varying the drain-source voltage, V_{DS}, from 0 V to -20 V at a fixed gate-source voltage, V_{GS}, and the measurements were repeated at the different gate voltages, which were varied from -15 V to -30 V. The intensity was controlled by the gate voltage and also the drain-source voltage of OTFT, and it was relatively compared at the different gate voltages as shown in Fig. 4.

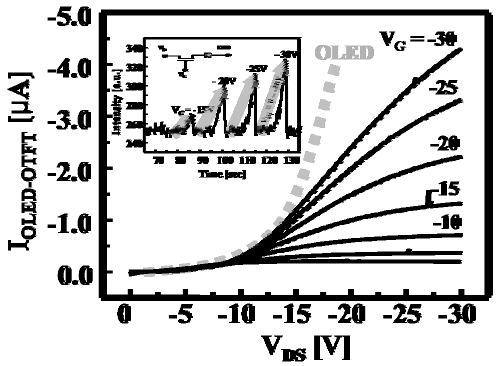

Figure 4. The electrical characteristics of OTFT–OLED pixel, and intensity of OLED depending on VGS and VDS of OTFT.

Thus, we could find out that OTFT successfully worked as a driving transistor for OLED by providing a sufficient current to OLED. In Fig. 5, the final panel with an array of pixels is shown together with the display of logo of Dong-A university as a demonstration.

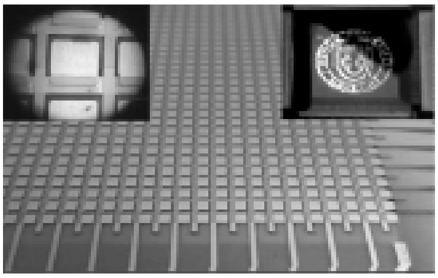

Figure 5. The picture of OTFT-OLED array fabricated on PET substrate; an enlarged pixel and the logo of Dong-A University, which is displayed on the panel, are inserted.

In an OLED display, in order to continuously supply the current to the OLED pixel while the other rows are addressed, at least two OTFTs are needed for one pixel. Two-TFT pixel circuit has high aperture ratio and increases reliability and yield because of low transistor count. As shown in Fig. 6, we fabricated AMOLED pixel consisted of two-OTFTs, one capacitor and one OLED.

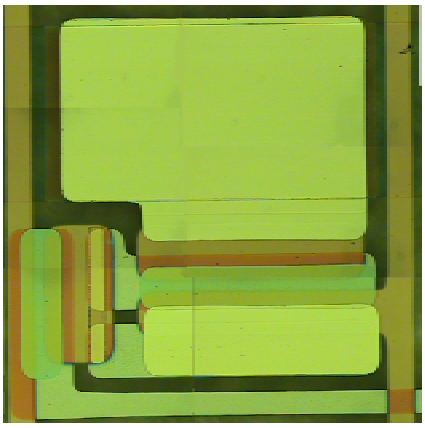

Figure 6. Photograph of pixel consist of OTFT-OLED

3. Conclusion

In conclusion, we developed a fabrication process of pentacene TFT with PVP gate on PET substrate and successfully fabricated an array of 64 x 64 pixels consisting of OTFTs and OLEDs. The panel demonstrated that the performance of pentacene OTFTs was good enough to drive OLEDs in an array on a large panel and is thus applicable to flexible AMOLED. However, we need to develop low temperature deposition process for PVP gate to avoid dimensional instability.

Acknowledgements

This research was supported by the MIC(ministry of Information and Communication), Korea, under the ITRC(Information Technology Research Center) support program supervised by the IITA(Institute of Information Technology Assessment).

References

[1] A. N. Krasnov, Appl. Phys. Lett., **80**, 3853-3855 (2002).

[2] A. Sugimoto, H. Ochi, S. Fujimura, IEEE J. Select. Topics Quantum Electron, **10**, 107-114 (2004).

[3] A. Sazonov, A. Nathan, D. Striakhilev, Journal of Non-Crystalline Solids, **266-269**, 1329-1334 (2000).

[4] T. W. Kelley, D. V. Muyres, P. F. Baude, T. P. Smith, T. D. Jones, in Proceedings of the 2003 MRS Spring Meeting, p.226. (2003)

[5] K. R. Sarma, presented at 3rd Annual Flexible Displays & Microelectronics Conf. Flexible Backplane Technologies (2004).

[6] M. Troccoli, T. Afentakis, T. Chuang, M. Hatalis, J. Hartzell, presented at 3rd Annual Flexible Displays & Microelectronics Conf. Flexible Backplane Technologies (2004).

[7] P. V. Lieshout, presented at 3rd Annual Flexible Displays & Microelectronics Conf. Display Technologies: Applications & The Electro-Optic Front Plane (2004).

[8] T. Chuman, S. Ohta, S. Miyaguchi, H. Sato, T. Tanabe, Y. Okuda, and M. Tsuchida, presented at SID (2004).

[9] C.K. Song, Y. X. Xu, H. S. Byun, G. S. Ryu, M. W. Lee, K. H. Kim, and C. H. Lee, presented at MRS Spring (2004).

[10] H. Klauk, M. Haik, U. Zschieschang, G. Schmid, W. Radlik J. Appl. Phys., **92**, 5259-5263 (2002).

[11] F. J. M. zu Heringdorf, M. C. Reuter, R. M. Tromp, Nature, **412**, 517-520 (2001).

[12] M. W. Lee and C. K. Song, JKPS, will be submitted. (2005)

[13] M. H. Choo, W. S. Hong, S. I. Im, Thin Solid Films, 420-421, 492-496 (2002).