Dual Damascene 공정에서 Bottom-up Gap-fill 메커니즘을 이용한 Cu Plating 두께 최적화

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Cu Plating Thickness Optimization by Bottom-up Gap-fill Mechanism in Dual Damascene Process

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Abstract : Cu metallization using electrochemical plating(ECP) has played an important role in back end of line(BEOL) interconnect formation. In this work, we studied the optimized copper thickness using Bottom-up Gap-fill in Cu ECP, which is closely related with the pattern dependencies in Cu ECP and Cu dual damascene process at 0.13 µm technology node. In order to select an optimized Cu ECP thickness, we examined Cu ECP bulge, Cu CMP dishing and electrical properties of via hole and line trench over dual damascene patterned wafers split into different ECP Cu thickness.

Key Words : ECP(Electrochemical Plating), CMP(Chemical Mechanical Polishing), Bottom-up Gap-fill, Dishing, SH(Step Height), AH(Array Height)

1. Introduction

The recent BEOL interconnect technology deposits barrier metal and seed Cu layer to via hole or trench pattern in dual Damascene process. It forms seam or Cu interconnect that there is no void in circuit using bottom-up Cu gap-fill technology. And it planarizes layer in Cu CMP process. Cu interconnect of multi-layer is formed by repeat of these process sequence. Bottom-up filling mechanism is consisted by accelerator that is admixture in electrolyte bath. It is used for gap-fill that there is no void or seam of via hole or trench in small feature size. After gap-fill step, bulge of positive profile is formed by accelerators of remaining much quantity on Cu film surface. In order to minimize bulge, we added leveler of big molecular weight that is another admixture. But it is impossible to remove bulge because of bottom-up gap filling characteristics. In case of big feature size, gap-fill becomes conformal plating by accelerator. Bulk Cu plating of wide line pattern forms negative profile. So, dishing happens at Cu CMP process. After ECP process, to minimize integration issue by SH(Step Height) and AH(Array Height) uses leveler as admixture that promotes planarization of plated Cu film surface or increases plating target thickness of Cu ECP process. In case of the former, it has limit to remove bulge perfectly. In case of the latter, it is not desirable in cost and TAT. Because Cu wastes, heavy metal, are happened much quantity in Cu CMP process, it can not become solution to increase Cu plating thickness. Hence, we have to minimize Cu plating target thickness of Cu ECP process in allowed extent of whole process integration, and optimize process.

2. Experiment

In this experiment, barrier metal was TaN/Ta bi-layer structure. We did sputtering etch step after TaN 100Å/Ta 150Å deposition, and removed TaN/Ta layer of via hole bottom electively. In sputtering etch step, we deposited Ta layer 100Å again adding flash step to via hole and neck of trench. Also, we confirmed gap-fill of dual Damascene structure using TEM(Transmission Electron Microscope) after Cu ECP process. We adjusted Cu plating condition changing bulk plating step time. And we confirmed SH and AH using SEM after Cu ECP process. Finally, we measured dishing after Cu CMP process and Metal line resistance of layer.

3. Result and Discussion

Figure 1 shows cross-section SEM images of blanket wafer per different plating target thickness. In this experiment, we used bottom-up gap-fill mechanism. We confirmed near result to 0.13µm technology node target plating. And we knew that Cu ECP became conformal plating similar to CVD in large pattern.

Table 1 shows Cu ECP and Cu CMP process time per different plating target thickness. We confirmed that Cu ECP process and Cu CMP process time decreased according as Cu ECP target thickness decreased. We consider that this may bring desirable results in cost and TAT.

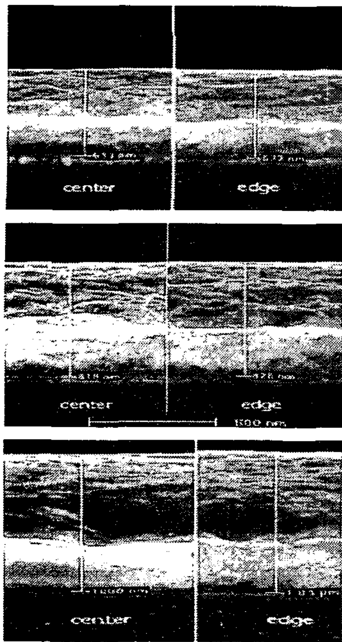

Fig 1. SEM images of blanket wafer per different plating target thickness:

(a) post 0.6μm plating ,

(b) post 0.8μm plating, and

(c) post 1.0μm plating.

Table 1. *Cu ECP and Cu CMP process time per different* plating target thickness.

Cu ECP Thickness	Cu ECP Process Time	CMP Process Time(A test)	CMP Process Time(B test)
0.6μm	61 sec	92.9 sec	133.0 sec
0.8μm	70 sec	106.5 sec	138.3 sec
1.0μm	80 sec	126.6 sec	148.2 sec

Figure 2 shows Cu CMP dishing result per different plating target thickness at wafer center and edge. We confirmed that dishing increased according as Cu ECP thickness decreased. Dishing of edge was bigger than center of wafer.

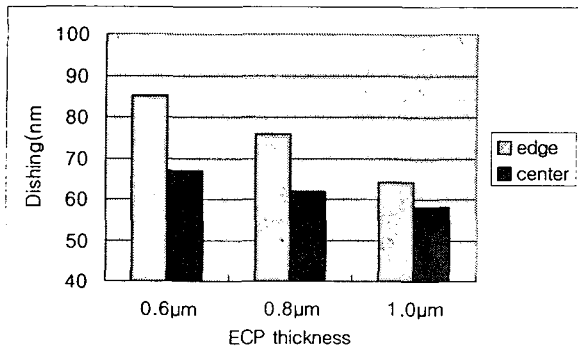

Fig 2. Cu CMP dishing result per different plating target thickness at wafer center and edge.

We experimented electrical test to find out effect that different Cu ECP thickness condition affected in electrical property of metal wiring. Figure 3 shows sheet resistance per different target plating thickness. Metal line Resistance value of 0.6μm target plating showed most broad distribution. Also, we confirmed that resistance distribution became broad gradually according as Cu ECP thickness decresed. This result was similarly with aspect of dishing data after Cu CMP.

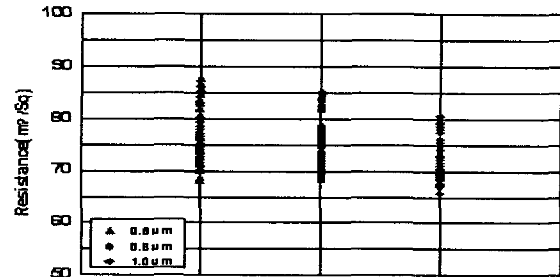

Fig 3. Sheet Resistance per different target plating thickness.

4. Conclusion

In this work, we experimented the optimized copper thickness using Bottom-up Gap-fill in Cu ECP. We confirmed that 0.8μm and 1.0μm Cu plating condition in 0.13μm technology node were no big difference in integration aspect and electrical properties with Cu CMP. 0.6μm plating condition that Baseline size reduced 40% showed bad property in broad resistance distribution of metal line and dishing after Cu CMP process in electrical properties. In conclusion, when we adopt Cu ECP thickness for cost and Cu CMP integration, 0.8μm and 1.0μm are a suitable plating thickness.

감사의 글

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