Subthreshold Characteristics of a 50 nm Impact Ionization MOS Transistor

Jee-Young Yoon, Jang-Woo Ryu, Min-Chul Jung, and Man Young Sung*
Korea Univ.*
*semicad@korea.ac.kr

50 nm Impact Ionization MOS 소자의 Subthreshold 특성

윤지영, 유장우, 정민철, 성만영*
고려대학교*

Abstract : The impact ionization MOS (I-MOS) transistor with 50nm channel length is presented by using 2-D device simulator ISE-TCAD. The subthreshold slope cannot be steeper than *kT/q* since the subthreshold conduction is due to diffusion current. As MOSFETs are scaled down, this problem becomes significant and the subthreshold slope degrades which leads an increase in the off-current and off-state power dissipation. The I-MOS is based on a gated *p-i-n* structure and the subthreshold conduction is induced by impact ionization. The simulation results show that the subthreshold slope is 11.7 mV/dec and this indicates the I-MOS improves the switching speed and off-state characteristics.

Key Words : I-MOS, impact ionization, avalanche, subthreshold slope, gated *p-i-n*

1. INTRODUCTION

As device scaling has continued rapidly for the past decades to achieve high speed and high packing density of ICs, many physical limits have become more important considerations. Power supply voltages have not been reduced as fast as device dimensions and thus the electric field within the depletion region of substrate-to-drain *pn* junction is so high in submicron MOSFETs that hot-carrier effects degrade the performance of devices [1]. Futhermore, the subthreshold slope cannot be steeper than the thermal voltage *kT/q* because subthreshold conduction is dominated by the diffusion mechanism and it is only a function of temperature [2]. As the effective channel length is scaled down, the threshold voltage is reduced and subthreshold slope even degrades because of drain-induced barrier lowering (DIBL) effect which is resulted in by reduction of control of the gate in scaled devices [3], [4]. Consequently, the leakage current at zero gate bias and off-state power dissipation are significant. The off current is given by

$$I_D(V_G=0,\ V_{DS}=V_{DD}) \approx \mu_{eff} C_{ox} \frac{W}{L} (m-1)\left(\frac{kT}{q}\right)^2 e^{-qV_T/mkT} \quad (1)$$

where m is the body-effect coefficient [2]. The reduction of the threshold voltage V_T causes substantial increase in the off current but the threshold voltage must be scaled down to achieve the high saturation current.

Many novel devices have been proposed to solve the problem of the trade-off between the device performance and off-state characteristics. However the subthreshold slope cannot be improved without modification the diffusion transport mechanism in the subthreshold region. The impact ionization MOS (I-MOS) was first proposed by Gopalakrishnan et al. using a *p-i-n* structure [5]. The I-MOS in which the subthreshold conduction is induced by impact ionization and thus avalanche effect has a subthreshold slope lower than *kT/q*. The I-MOS device proposed in Gopalakrishnan et al. is based on germanium which has high impact ionization coefficients but the reliability of Ge is poor and seldomly used in the modern VLSI technology.

This paper proposed the *n*-channel silicon I-MOS device with the 50 nm channel-length. The device was designed and the current-voltage characteristics including the subthreshold characteristics are analyzed using 2-D device simulator ISE-TCAD.

2. EXPERIMENTAL

2.1 Device Structure and Physical Operation

The outline of the device structure for the *n*-channel I-MOS using SOI technology is shown in Fig.1. It is based on a gated *p-i-n* structure. The *i*-region can be either an intrinsic or lightly doped semiconductor substrate. The n^+ region is the drain and p^+ region is the source for the *n*-channel I-MOS. The gate does not fully cover the *i*-region and the gate is attached to the edge of the drain.

The distance between the source and drain is the entire

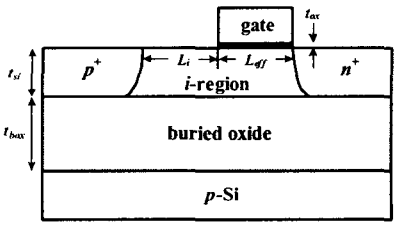

Fig. 1. Outline of device structure for the *n*-channel I-MOS

i-region when $V_G<V_T$. The inversion layer is formed as V_G is increased and the effective channel length is L_{eff}. Therefore the DIBL effect can be effectively reduced while the on-current is maintained as high as that of the general nMOSFET with the corresponding channel length. When the positive voltage is applied to the drain with the source as the reference, the depletion region at the source-substrate junction extends to the i-region outside the gate and impact ionization takes place at the depletion region. The generated carriers contribute to the channel conduction and this leads the subthreshold slope steeper than kT/q.

2.1 Device Simulation

Simulations of 50 nm n-channel Si I-MOS device were performed using ISE-TCAD. The dimensions and doping concentrations are given in Table 1. The i-region is a lightly doped p-type region in this work. The conventional n-channel SOI MOSFET with the same channel length was also simulated for comparison.

Table 1. Device parameters

Doping Concentration	Thickness	Length
N_d=10^{18} cm^{-3} for n^+	t_{ox}=2 nm	L_{eff}=50 nm
N_a=10^{18} cm^{-3} for p^+	t_{si}=30 nm	L_i=50 nm
N_a=10^{14} cm^{-3} for i	t_{box}=100 nm	

3. RESULTS AND DISCUSSION

Fig. 2 shows the simulation result of the electrostatic potential with the position in the surface under the gate bias V_G=1V and the drain bias V_D=1V for the I-MOS device. It is obvious that the channel is formed only under the gate (between x=0.10 ㎛ and 0.15 ㎛). Moreover most of drain-source voltage is applied at the i-region outside the gate in which the electric field is so high that impact ionization occurs.

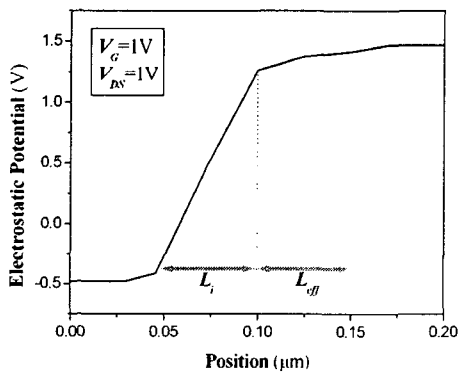

Fig. 2. Simulation of the electrostatic potential with the position in the surface at V_G=1V and V_D=1V.

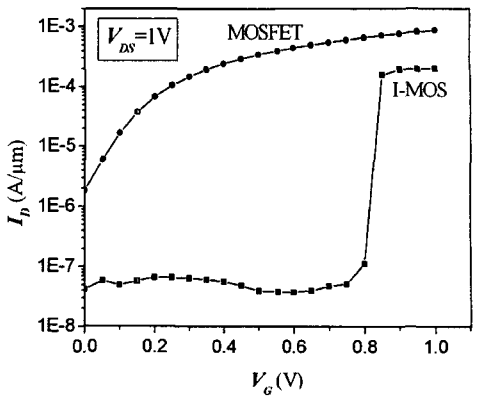

Fig. 3. I_D - V_G characteristics of the n-channel MOSFET and I-MOS device at V_{DS}=1V.

Fig. 3 shows the I_D versus V_G characterisitcs of both the MOSFET and I-MOS device for a drain bias V_{DS}=1V. The simulated subthreshold slopes the MOSFET and I-MOS device are approximately 104 mV/dec and 11.7 mV/dec respectively. The off-current of the I-MOS device is 4.1×10^{-8} A/㎛ smaller than that of the MOSFET. However, the threshold voltage of the I-MOS device is quite higher and the on-current is smaller than those of the MOSFET. This can be improved by channel doping profile modification.

4. CONCLUSION

We have presented the 50 nm n-channel I-MOS device and showed that it has the small subthreshold slope lower than kT/q. The I-MOS can be promising for high speed and low power dissipation.

REFERENCES

[1] D. J. Frank, R. H. Dennard, E. Nowak, P. M. Solomon, Y. Taur, and H. P. Wong, "Device scaling limits of Si MOSFETs and their application dependencies", Proc. IEEE, Vol. 89, No. 3, p. 259, 2001

[2] Y. Taur and T. Ning, Fundamentals of modern VLSI devices, Cambridge Univ. Press, 1998

[3] W. Fichtner and H. W. Potzl, "MOS modelling by analytical approximation, I. Subthreshold current and threshold voltage", Int. J. Electron., Vol. 46, p. 33, 1979

[4] R. R. Troutman, "VLSI limitations from drain-induced barrier lowering", IEEE Trans. Electron Devices, Vol. 26, No.4, p. 461, 1979

[5] K. Gopalakrishnan, P. B. Griffin, and J. D. Plummer, "I-MOS: A novel semiconductor device with a subthreshold slope lower than kT/q", IEDM Tech. Dig., p. 289, 2002