종이 기판을 이용한 유기박막 트랜지스터의 제작

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Polymer Thin-Film Transistors Fabricated on a Paper

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Abstract : In this report, we demonstrate a high performance polymer thin-film transistor fabricated on a paper substrate. As a water barrier layer, parylene was coated on the paper substrate by using vacuum deposition process. Using poly (3-hexylthiophene) as an active layer, a polymer thin-film transistor with field-effect of up to 0.086 $cm^2/V \cdot s$ and on/off ratio of 10^4 was achieved. The fabrication of polymer thin-film transistor built on a cheap paper substrate is expected to open a channel for future applications in flexible and disposable electronics with extremely low-cost.

Key Words : Polymer thin-film transistor, paper substrate, parylene, P3HT

1. Introduction

Organic thin-film transistors (OTFTs) are now widely investigated as switching devices for active-matrix displays and integrated circuits such as radio-frequency identification tags (RF-IDs) [1,2]. Various fabrication techniques are currently used to develop high performance OTFTs such as vacuum deposition, ink-jet printing, screen printing and rubber stamp printing. OTFTs with vacuum deposited organic semiconductors exhibit the highest performance but from the manufacturing cost point of view, printing based technology is more favorable.

The focus of this paper is to develop polymer thin-film transistor arrays on an extremely cheap paper substrate. In this approach, with a combination of roll-to-roll process extremely low-cost electronics can be realized. However, compared to a plastic or a thin metal substrate, the paper substrate suffers from wet and various chemical processes. In order to protect the paper from degradation, a barrier layer must be coated over the entire substrate. As a barrier layer, parylene was coated on the paper by vacuum deposition process. Since the parylene is a hydrophobic material with thermal mechanical stability up to 150°C, the parylene layer effectively protects the paper from water and chemical penetration.

2. Experimental Details

The gate electrode has been made of 100 nm-thick Ni, deposited at room temperature by using radio-frequency (RF) magnetron sputtering. Dual layer of polyimide (PI)/SiO_2 was used as a gate dielectric, which improves the electrical properties of the OTFT device. The thickness of PI and SiO_2 films were 40 and 210 nm, respectively. As source/drain electrode, electron beam deposited Cr (20 nm) with thermally evaporated Au (50 nm) layer was used. After defining the source and drain electrodes, O_2 plasma and hexamethyldisilazane (HMDS) treatments of oxide layer were followed sequentially.

Poly (3-hexylthiophene) (P3HT) was used after purification process with tetrahydrofuran (THF) and acetonitrile to increase the head-to-tail regioregularity. Later, P3HT was dissolved in chloroform with a concentration of 0.2 wt% and then spin coated or rubber stamp printed on the substrate. Electrical characteristics of the device were measured using Keithley 4200-SCS semiconductor characterization system.

3. Results and Discussion

Figure 1 shows the atomic force microscopy (AFM) images of bare paper substrate and parylene coated paper substrate. As expected from the observation through the optical microscope, the surface characteristic of the bare paper substrate is very poor and the root-mean-square (RMS) roughness of the bare surface is more than 31 nm as shown in Fig. 1 (a). This poor surface characteristic of the substrate leads to, inferior dielectric properties of gate dielectric layer and significant degradation in the performance of the resulting organic transistor by more disordered molecular structure of polymer layer on gate dielectric. Therefore, improvement of surface characteristics of the bare paper substrate should be considered to achieve high field effect mobility.

The AFM image of a 5 μm-thick parylene coated paper substrate is displayed in Fig. 1 (b). Compared to the bare surface, the surface of parylene layer is relatively smooth

with the RMS roughness less than 11 nm. To further improve the surface characteristics of the paper substrates, additional organic or inorganic coating can be applied. Particularly, with an additional surface coating with SiO_2 coating, the RMS roughness can be reduced down to 7 nm (Fig. 1 (c)). Thus, the RMS roughness has been considerably reduced from 31 nm to 7 nm after the treatment of paper surface by depositing different barrier layers. To further improve the surface properties of paper substrate, thicker parylene (10 ㎛) or polymer resin can be coated additionally (Fig. 1 (d) ~ (f)).

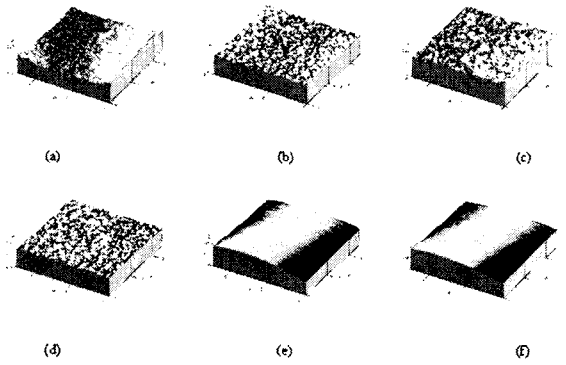

Fig. 1. AFM images of paper substrate surface with various coating layers; (a) bare, (b) parylene coated, (c) parylene / SiO_2 coated, (d) parylene / parylene coated, (e) parylene / polymer resin coated and (f) parylene / polymer resin / SiO_2 coated.

Using the parylene coated paper substrate, OTFT array was fabricated with P3HT as the active channel layer. The P3HT solution was spin coated over the fabricated device. Figure 2 (a) shows the transfer characteristics of the OTFT device with drain voltage (V_{DS}) of -40 V, and the inset shows the drain current (IS) versus drain voltage (V_{DS}) at various gate voltages (VS). The OTFT device had bottom contact TFT geometry and the gate length (L) and the width (W) were 25 ㎛ and 500 ㎛, respectively.

The field effect mobility calculated in the saturation regime was 0.086 $cm^2/V{\cdot}s$ where the threshold voltage (VT) was -11.9 V. The current modulation which is the ratio of the current in accumulation mode over the current in the depletion mode was more than 10^4. These results of OTFT on paper substrate are compatible to the results in conventional OTFT on glass/polymer substrates.

In addition to the spin coating method, the transistor was also fabricated by using a rubber stamp printing process with pre-patterned stamps [3]. Figure 2 (b) shows the output characteristic of an OTFT device fabricated by using the rubber stamp printing method. The device was fabricated on a parylene coated paper substrate with an additional polymer resin coating to improve the surface properties. Here, the calculated field-effect mobility was 0.081 $cm^2/V{\cdot}s$, showing similar result compared to the spin coated devices.

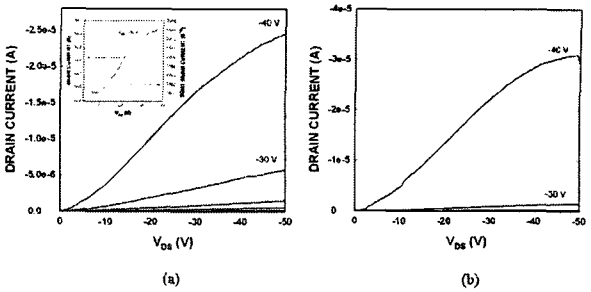

Fig. 2. I-V characteristics of polymer thin-film transistors on a paper (a) spin-coated, (b) rubber-stamp-printed.

4. Conclusions

We fabricated high performance organic transistors on a photo paper with the field effect mobility up to 0.086 $cm^2/V{\cdot}s$ and on/off ratio of 10^4. In order to carry out the wet chemical process, the paper was coated with parylene layers. The fabrication of organic devices on a extremely cheap paper substrates may be important for realizing future applications in flexible and disposable electronics.

Acknowledgement

This work was supported by grant No. RTI04-01-02 from the Regional Technology Innovation Program of the Ministry of Commerce, Industry and Energy (MOCIE).

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