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Solid Phase Crystallization of Amorphous Silicon at High Temperatures

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Polycrystalline silicon films have received a great deal of attention since they can be applied to various applications such as a gate electrode for MOSFET, the emitter in bipolar transistors and interconnects. Recently polycrystalline silicon thin film transistors (poly-Si TFT's) have attracted considerable interest for the fabrication of active matrix liquid crystal display (AMLCD) and active matrix organic light emitting diode (AMOLED). Directly deposited Poly-Si films exhibit a very fine grain size with a columnar microstructure. Enhancement of the grain size is generally achieved by solid phase crystallization (SPC) of amorphous silicon (a-Si) films. SPC is usually conducted at relatively low temperatures such as 600℃ due to a transparent glass substrate which is thermally susceptible. The kinetics and the microstructural characteristics of SPC low temperature polycrystalline silicon (LTPS) have been extensively investigated for the past 20 years. High temperature behavior, however, of SPC Poly-Si has not been studied to a great extent and thus is not well understood. In this study we performed SPC in the temperature range of 600℃ to 1000℃ using 500A-thick PECVD a-Si films on a silicon wafer. We will report the behavior of crystallization and defect anneal during SPC in these temperature ranges.