Discharge delay reduction by controlling the roughness of dielectric surface in AC PDP

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Abstract
We report a method for reducing the address discharge delay. The address discharge delay was reduced when the MgO protective layer was made on the dielectric area which was made rough intentionally. The delay reduction was more pronounced in the formative delay.

1. Introduction
An AC plasma display panel(PDP) has been the most important device in the large flat displays. Although AC PDP was commercialized successfully in recent years, it still has some display characteristics which need improvements such as the contrast ratio, luminous efficacy or high speed addressing.[1] For dealing with the requirement of increasing the resolution, the high speed addressing is an essential technique and needs short address discharge delay. There have been many works for reducing the discharge delay, such as via the improvement of voltage waveform[2,3], material characteristic[4,5], electrode structure[6], and so on.
In this paper, we changed the roughness of MgO protective layer and could obtain the address discharge delay reduction especially in the formative delay.

2. Results
2.1. Preparing the rough MgO

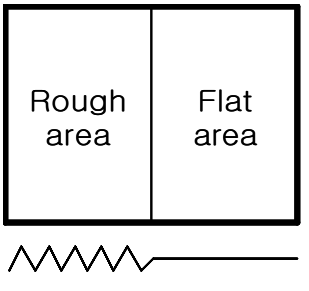


Figure 1. Dielectric surface of the front panel

Figure 1 shows the simplified concept of the idea used in this work. Half of the dielectric layer surface of test panel is chemically etched to make its surface rough. The distance between peaks and valleys in the rough area is about 1 ㎛. 4000 Å thick MgO layer is formed on the dielectric surface by e-beam evaporation, and test panels were made to investigate its effects on the discharges.

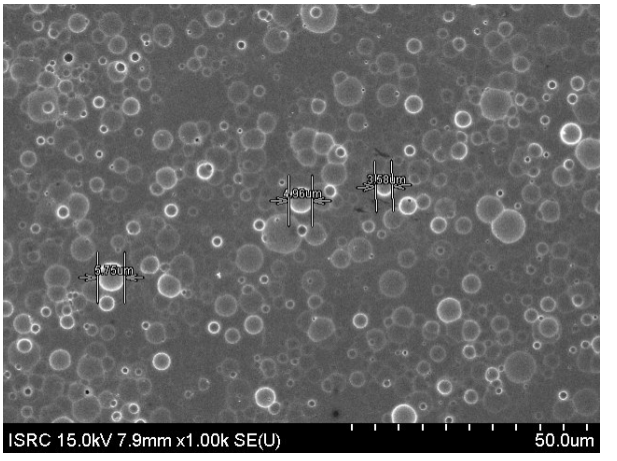
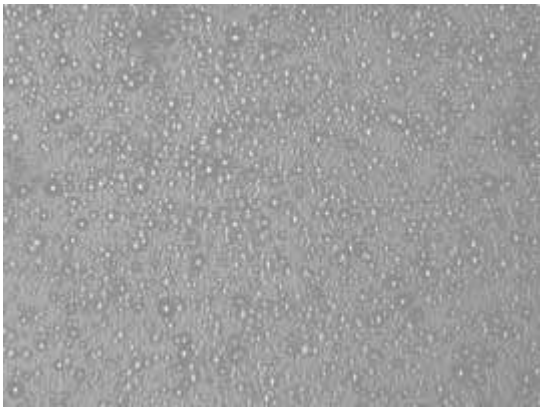
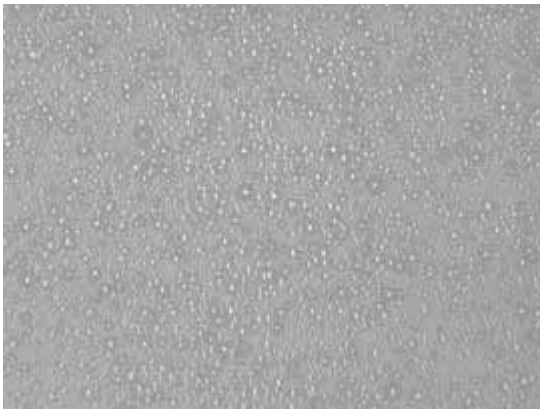


Figure 2. SEM image of dielectric surface

Figure 2 is an enlarged photograph of dielectric surface. The etchant does not dissolve dielectric layer uniformly, so we could obtain rough surface. The round particles on the dielectric layer have the height around 1 ㎛. Although 4000 Å thick MgO layer were formed on the dielectric surface, the average roughness did not changed much as shown in figure 3 which shows that the Ra value of 0.595 ㎛ changed to 0.529 ㎛ when MgO was deposited.



(a) Before forming MgO (Ra = 0.595㎛)



(b) After forming MgO (Ra = 0.529㎛)

Figure 3. Average roughness of the surface

2.2. Driving condition

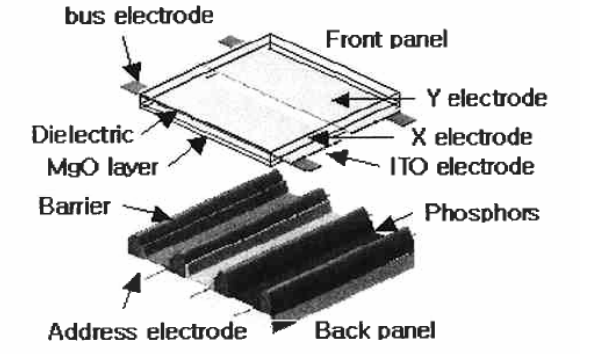


Figure 4. Schematic diagram of the single pixel structure of an AC PDP

The test panels used in this experiment have VGA resolution and their single cell structure is shown in figure 4. The widths of ITO and bus electrodes are 340 ㎛ and 80 ㎛ respectively. The gap between ITO electrodes is 80 ㎛ and barrier rib height is 150㎛. Used voltage waveform is shown in figure 5. Vy1, Vy2, Vscan, Vx, Vadd are 190V, 240V, 80V, 180V and 80V respectively.

The address discharge delay was measured for three gas condition, Ne+Xe 4, 8, 12% . Total pressure is 400 torr in all the cases.

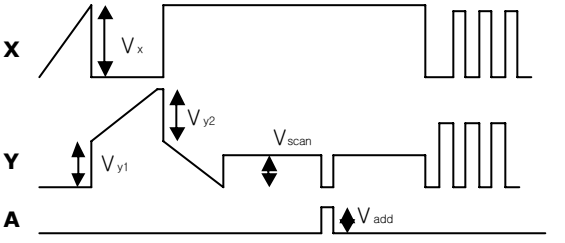


Figure 5. Schematic diagram of driving waveform

2.3. Measurement and discussion

In every test panel and gas condition, the formative discharge delays were reduced and the reduction ratio increased as the Xe partial pressure increased. The statistical delays were also reduced. But apparent tendency could not be found in the statistical delay. Figure 6 shows the results of three test panels and figure 7 is the delay measurement of three gas conditions in the same panel. There was variation of measured delay according to the panels, but it is obvious that the panels with rough MgO surface have shorter address discharge delay.

We think these shorter formative delays are caused by the difference in the amount of wall charges. Although the voltage difference between scan(Y) and address(A) electrodes is made to be the nearly breakdown voltage after ramp reset, there are supposed to be differences in the wall charge amount, which make the apparent difference in electric field. As the Xe partial pressure increases, the breakdown voltage increases too. And the wall charge amount on Y and A electrodes is larger after ramp reset when the Xe partial pressure is high. We think that the wall charge amount difference and thus the wall voltage difference between the rough and flat area is larger when the wall charge amount itself is larger.

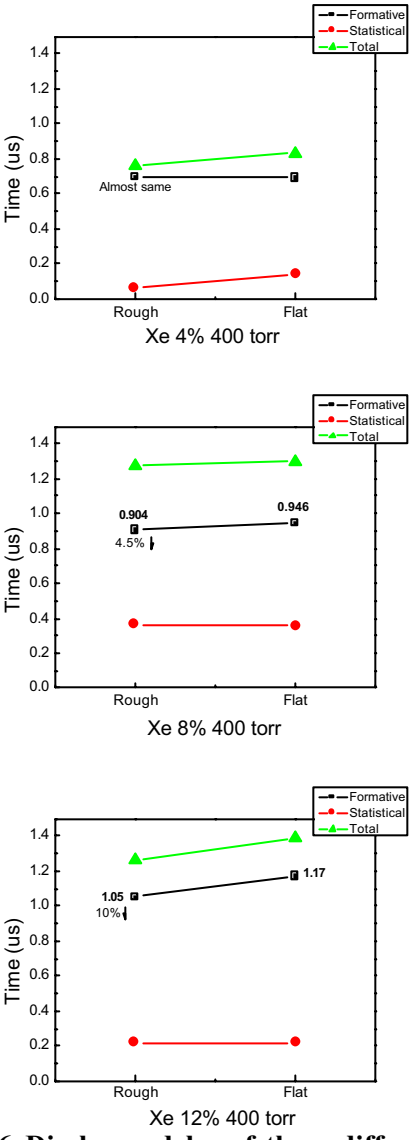


Figure 6. Discharge delay of three different test panels

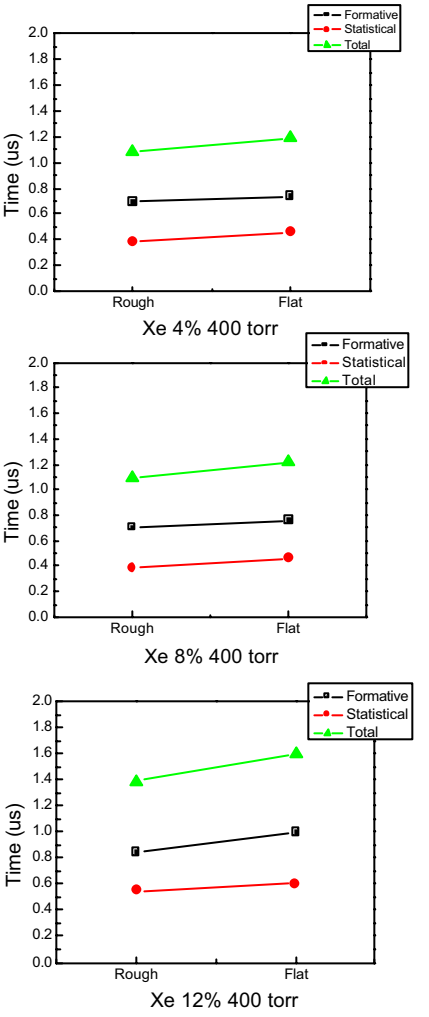


Figure 7. Discharge delay of three gas conditions in the same panel

Larger wall charge amount also seems to change statistical delay, but its reduction shows no apparent tendency. The difference between the rough and flat was little in firing and sustain minimum voltage as shown in figure 8. The test panel used in figure 7~9 is same. In X axis of figure 8, 'E' means 'Etched(rough)' and 'NE' does 'Not Etched(flat)'. The numbers(4~12) mean partial pressure of Xe gas. The luminance in the rough area was somewhat darker because the transparency was reduced by the roughness. But the efficiency was not different very much.

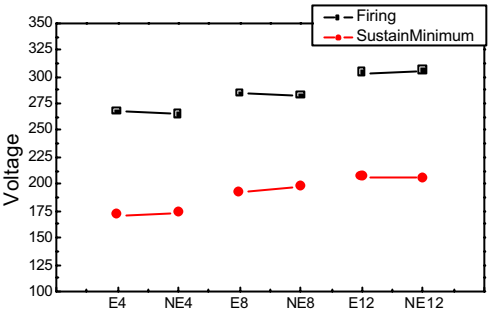


Figure 8. Firing and sustain minimum voltage

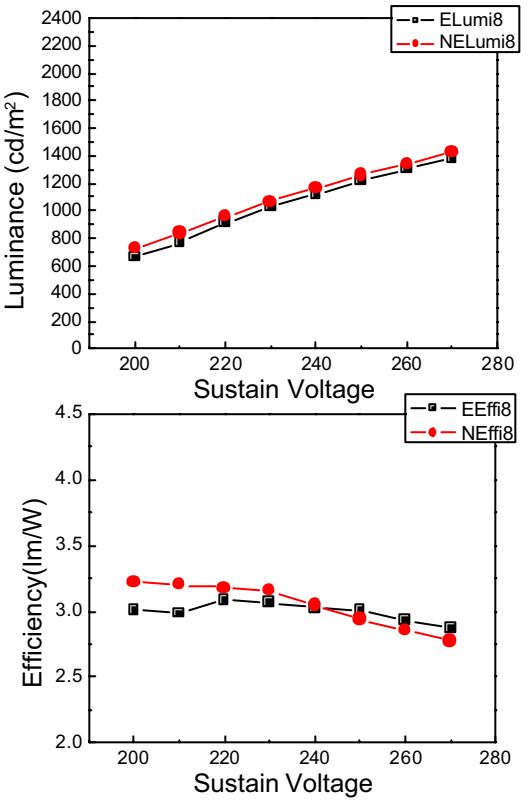


Figure 9. Luminance and efficiency of the panel(Ne+Xe 8%)

3. Conclusion

In our work, address discharge delay was reduced by making the MgO surface rough. Formative delay was reduced consistently in all of the gas conditions. Statistical delay was also reduced slightly. The reduction of discharge delay by roughening the dielectric surface became more pronounced as the Xe partial pressure increased.

4. References

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