LTPS (Low Temperature Poly Si) Technology Based on SLS (Sequential Lateral Solidification) Crystallization for Advanced Mobile Display

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Abstract
LTPS technology based on SLS Crystallization was intensively reviewed. LTPS structure produced by SLS crystallization is composed of much larger grains compared with conventional ELA crystallization structure, which can give higher TFT performances. However, TFT performance uniformity and anisotropy problem should be solved for it to be used in mass production. TFT performance uniformity was from main grain boundary position and could be solved by equal defect area structure (EDAS™). TFT performance anisotropy could be also solved by multi-channel (MC) structure that can make parallel component in perpendicular channel direction. The higher TFT performances from SLS technology can make superior optical and/or electrical properties and has been adopted in mass production successfully.

1. Introduction

Polycrystalline-silicon (p-Si) thin-film transistors (TFTs) are used in a variety of applications, including large-area electronics [1, 2] and vertically stackable components for three-dimensional integration [3]. P-Si is typically fabricated from amorphous Si (a-Si) thin-film deposited on an inexpensive glass, such as Corning 1737, which has a quoted working range below 600°C. Various recrystallization technologies of a-Si film have been developed to meet this temperature limitation of glass. Among various recrystallization technologies, the ELA (Excimer Laser Annealing) method has been commonly adopted in commercial fields. [4] In ELA, a XeCl excimer pulsed laser is irradiated on a-Si precursor film. It is absorbed by a film surface and induces instant melting and solidification. The short pulse duration of the laser beam prevents sustained heating of the underlying substrate, and makes the process compatible with glass substrate [5]. The crystallinity is superior to that of other crystallization techniques such as SPC (Solid Phase Crystallization) because the transformation from a-Si to p-Si is occurred via melting and re-solidification process.

In the mean time, the property of p-Si TFTs is mainly dependent on grain boundaries within channel area and interface between gate insulator and silicon [6]. Trap state in grain boundary increases Vth and decreases Ion and also uniformity, which makes it difficult to use LTPS technology in advanced AMOLED application.[7] To minimize the number of grain boundaries within the channel area, SLS [8] technology, which can make large lateral grains, have been developed.

SLS technology can make it possible to produce a few micrometers order of grains that are almost 10 times larger than those produced by ELA technology. From the large grain size and controlled grain boundary locations, much higher TFT performance can be obtained. SEC has developed 21.3" world's largest LTPS LCD [9] using SLS technology.

However, larger grain size can induce poor TFT performance uniformity. Also the microstructure produced by SLS crystallization is quite anisotropic. These two problems can make it difficult for SLS to be adopted in mass production. In this paper, the reasons for these problems will be discussed. The solutions could be obtained from the main mechanism.

2. Results and Discussions

2-1. General Features of SLS technology

Fig. 1 shows the microstructures of poly Si (p-Si) materials produced by SLS (1(a)) and ELA (1(b)) crystallization.

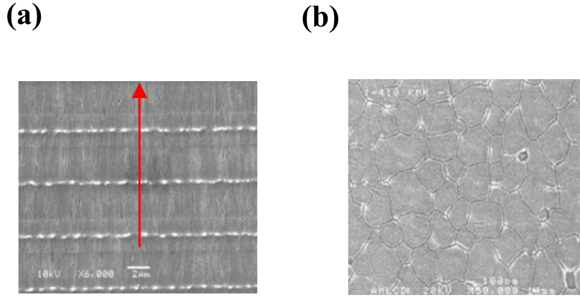


Fig.1. Schematics and SEM microstructure of p-Si produced by (a) SLS and (b) ELA crystallization.

As can be seen in Fig 1(a), SLS p-Si is composed of large uniform grains of which sizes are over 3μm following the direction indicated by arrow. The perpendicular to this direction shows much smaller grain size. For ELA crystallization, the grain size is about 0.3um and shows no anisotropy. The orderly located lines in SEM microstructure of Fig. 1(a) are main grain boundaries formed in the center of melted region when lateral grains collide. Due to density difference between liquid and crystalline Si, protrusions are formed along the main grain boundaries so that the lines look brighter in SEM picture.

Fig. 2 shows the champion data of n-channel TFTs made by both SLS (parallel channel direction to crystallization) and ELA technologies. The overall properties are summarized in Table 1.

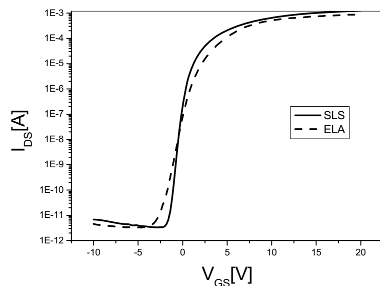


Fig.2. TFT transfer characteristic comparison between SLS and ELA TFTs.

Table1. Comparison of TFT performance between SLS and ELA TFT

	SLS	ELA
Mobility(cm2/Vs)	192	93
Vth(V)	1.39	1.62
Ion(μA)	1430	792

As can be seen Fig.2 and table1, the mobility of SLS TFT is over twice than that of ELA TFT. SLS TFT shows much higher Ion characteristic and similar Ioff level. Vth is also lower. These superior TFT performances can be attributed to the larger grain size from lateral growth in SLS technology.

2-2. TFT performance uniformity

Because the grain size of SLS is much larger than that of ELA, it is difficult to get similar TFT performance uniformity in SLS to that in ELA. Fig. 3 shows the TFT performance variation, Mobility and Vth, for ELA and SLS TFTs. The data was measured for 48 sequential TFTs spaced 240μm between each TFT.

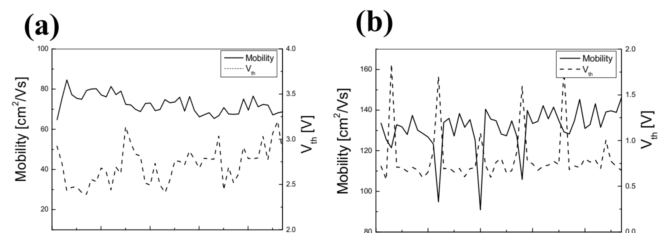


Fig.3. TFT performance variation for the uniformly distributed 48 TFTs; (a) ELA and (b) SLS TFTs

For ELA TFTs, overall Vth variation is not so good, as is shown in Fig. 3(a). The overall variation is almost 1V. Mobility is also varying over the whole area. However, the variation between adjacent TFTs isn't so much. On the other hand, SLS TFT shows quite different manner. The overall variation of Vth looks not so much except some poor TFTs. These poor TFTs have almost 1V higher Vth value and

lower mobility than normal ones. The Vth variation except these TFTs is less than 0.2V but variation increases up to 1V if these TFTs are included.

From an extensive study on TFT uniformity, it was found that a protrusion is close to a junction of the gate edge in the source region for all the degraded TFTs. The exact distance between source junction and protrusion could be measured in FIB observation. The results are summarized in table 2. If the protrusion is nearer than 3000A or farther than 7000A to the source junction, there was no property degradation of SLS TFTs. However, if the protrusion is located between the range of 3000A and 7000A, all the TFTs showed high Vth and low mobility.

Table2. Relationship between Vth and distance between gate edge and protrusions

Distance	Vth property
< 3000 Å	Good
3000 ~ 7000 Å	Bad
> 7000 Å	Good

To overcome Vth non-uniformity with high reliability, the best way is to make every TFT have the same situation. Fig. 4 shows the schematic of this idea.

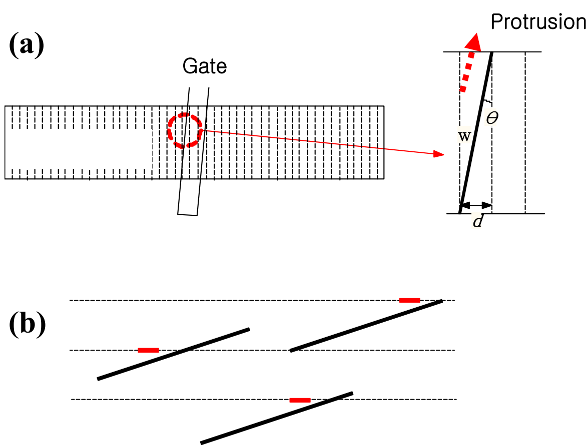


Fig.4. (a) Schematic illustration of Equal Defect Area Structure (EDAS^{TM}) and (b) various gate edge locations having the same defect area.

For making every TFT have the same defect area, the protrusion and gate edge were made to have special tilt angle. The optimum tilt angle can be determined for gate edge to be the diagonal of two adjacent protrusions. This angle can be calculated following Eq. (1).

$$\theta = \text{arcsine}\ (d/w) \qquad (1)$$

W is TFT width and d is the distance between protrusions. Fig. 4(b) shows this relationship between protrusion and EDAS^{TM} TFTs. Wherever the TFT locates, the area of defect region are all the same.

New EDAS^{TM} TFTs for 3.5μm protrusion distance and 20μm TFT width was fabricated for verification. The optimum angle for this structure could be calculated following Eq.(1) and determined to be 10.4^0. The measured uniformity of TFTs is shown in Fig. 5.

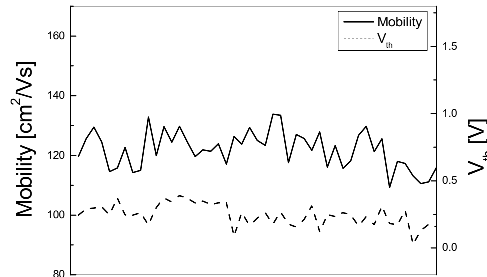


Fig.5. TFT performance variation for the uniformly distant 24 EDAS TFTs

As can be seen Fig. 5, the maximum Vth variation is decreased to less than 0.2V. The poor TFTs that could be found in normal SLS TFTs cannot be found in this data. These strikingly improved results can be attributed to the new EDAS^{TM} architecture. All the TFTs have the same defect area and the variation could be minimized. With fine tuning of this structure, SLS technology will be used successfully in high performance required fields such as OLED and SOG.

2-3. TFT performance anisotropy

Fig. 6 shows dependence of TFT performance on the SLS crystallization direction. The mobility of TFT along parallel direction is $192cm^2/Vs$ and on current is over 1430μA. But the mobility and on current decrease to less than $50cm^2/Vs$ and 600μA for the TFT along perpendicular direction even the p-Si material is the same. The TFT along perpendicular direction is even lower than that of conventional ELA TFTs.

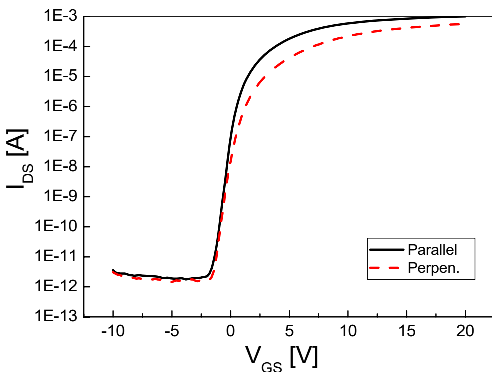
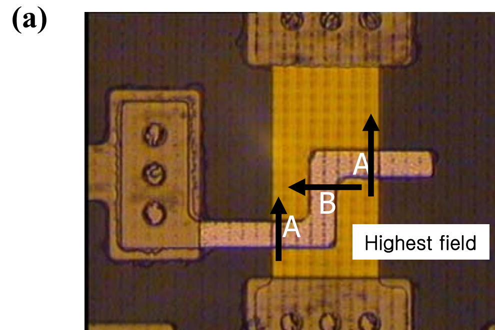


Fig.6. Dependence of SLS TFT performance on the channel direction

The best way to solve this property anisotropy is to locate every TFT channel along the same direction. But as the integration level increases, it is difficult to make every TFT have the same direction. It will make circuit area and device size larger.

To improve TFT performance of perpendicular TFT to the level of parallel direction, multi channel (MC) structure having parallel chanel component within perpendicular TFT was devised as Fig 7(a). MC structure has three channel areas. (Two perpendiculars (A) and one parallel (B)) If there is no B component, it will be a perpendicular TFT and show low property. But MC TFT has parallel current path (B) so that the property can be increased to the level of parallel TFT.

(a)



(b)

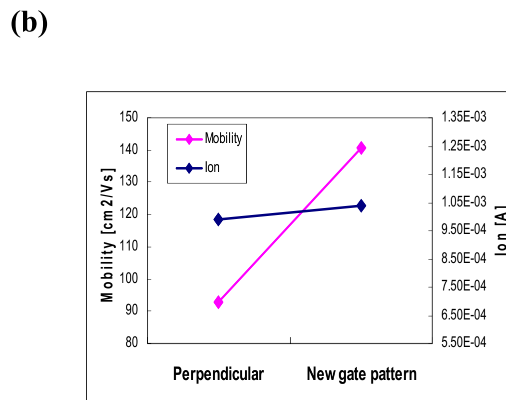


Fig.7. (a) MC TFT structure and (b) comparison between perpendicular and MC TFT performances

Fig 7(b) compares the perpendicular TFTs and MC TFT having the same channel width and length. As can be seen in Fig. 7(b), the insertion of parallel component improved TFT performance dramatically. The on current increased little by 5%, but mobility increased by 52%. From the fact that the mobility increased much higher, it can be thought that the material characteristics was improved. MC can match highest field and parallel direction for carriers to follow lateral growth direction. So the TFT performance is similar to that of parallel TFTs. The MC TFT area can be increased more but the increased area is much smaller than that of TC structure or perpendicular TFT having a large width to achieve the same level of performance. MC is the most efficient way to improve perpendicular TFT performance.

MC structure can provide a solution for not only perpendicular SLS TFT but also other semi-conductor materials that have property anisotropy. The

additional benefit of this structure is to tailor TFT performance by adjusting ratio between perpendicular and parallel width from the panel design stage, which can expand the flexibility of panel design for high end SOG applications.

Fig.8 shows the world 1st commercial product adopting QVGA TFT-LCD produced by SLS technology. The higher TFT performance and productivity could make it possible for SLS to be applied to mass production in a very short time.

Fig.8. World 1st commercial HHP product adopting SLS technology incorporated TFT-LCD.

3. Conclusion

State of the art SLS technology has been developed for high end mobile application. SLS crystallization can produce higher grain size so that TFT performance can be improved with less number of laser shots.
However, larger grain size causes uniformity problem and property anisotropy. Bad uniformity was caused by main grain boundary position and could be solved by EDAS proposed in this paper. Performance anisotropy could also be improved by MC TFT structure.
Using many improvements in problems of SLS crystallization, SEC could apply SLS to mass production successfully.

4. References

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