System Interface for SoG in LTPS TFT Process

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Abstract

For system-on-glass (SoG) with low-temperature poly-silicon (LTPS) thin film transistor (TFT), a new system interface architecture and timing controller are developed. With the newly developed system interface architecture, line memory can be eliminated which would take large area of SoG display panel. The system interface and timing controller are targeted for the application for 6-bit gray scale, 60-frames/s qVGA format.

1. Introduction

With low-temperature poly-silicon (LTPS) thin-film transistor (TFT) technology, display driving circuitry can be integrated on the same glass substrate as display panel and the ultimate goal is system-on-glass (SoG) where all the display electronics are on the same glass substrate as shown in Figure 1. Recently, various research results have been reported for the realization of SoG. For example, scan and data drivers are integrated on pixel size panel [1-2] and highly efficient DC-DC converter for scan driver is implemented on glass substrate [3]. Dynamic random access memory (DRAM) was also implemented in a LTPS TFT technology to verify the feasibility of integration of frame and line memory on glass [4].

For SoG, the system interface including timing controller has to be integrated on glass substrate as well which connects external graphics controller and the internal display electronics as shown in Figure 2. However, it is very challenging to implement the system interface on the glass substrate with LTPS TFT because of the poor performance of LTPS TFT. The circuitry for system interface includes various kinds of analog circuits which is heavily dependent on the characteristic and its variation of transistors. Unfortunately, the characteristics of LTPS TFT are much poorer and their variations are much larger than those of single-crystalline transistors [5]. Another problem associated with the integration of system interface is the required glass substrate area. The minimum channel length of advanced LTPS TFT process is still much larger than that of single-crystalline process. Therefore, in order to achieve the acceptable performance with LTPS TFT, the area will be very large.

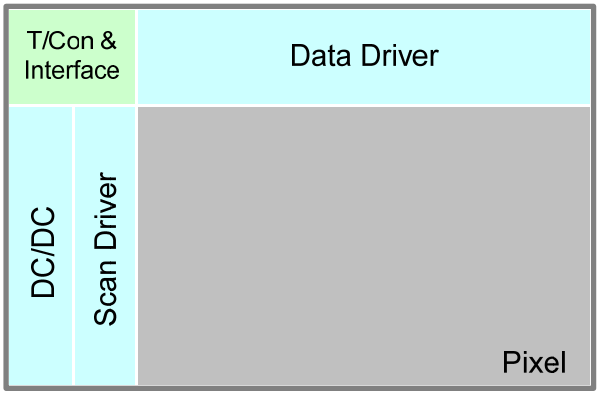

Figure 1: Conceptual diagram of system on glass.

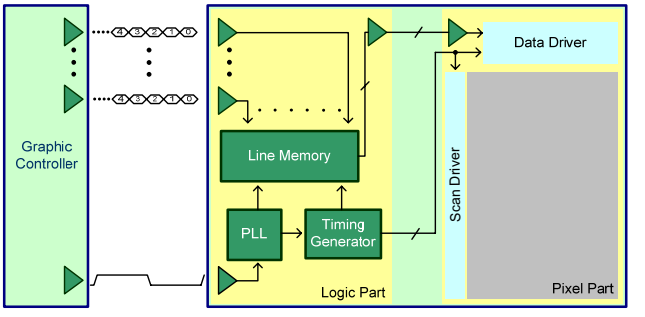

Figure 2: Schematic of system interface and timing controller.

In this paper, new system interface architecture is proposed with which line memory can be removed for small-area realization of SoG. The large variations of the characteristics of LTPS TFTs are compensated by a full-digital scheme. The proposed techniques are applied to a 60-frames/s, 6-bit gray scale, qVGA format panel.

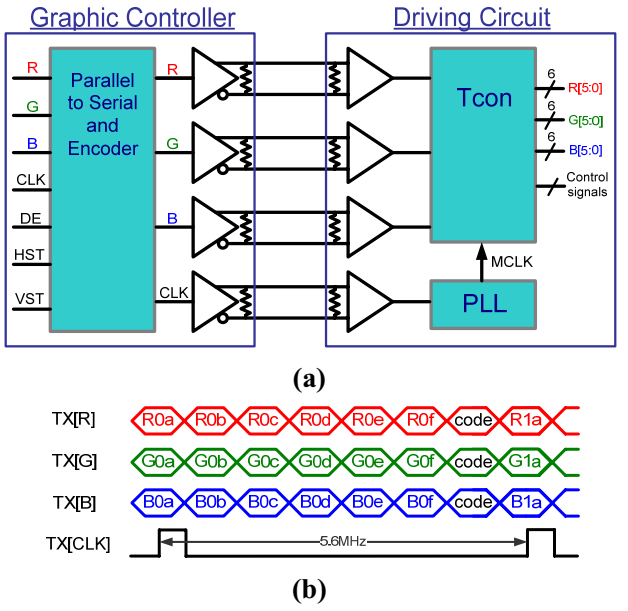

Figure 3: (a) Conventional system interface and (b) simplified timing diagram of graphic data transfer.

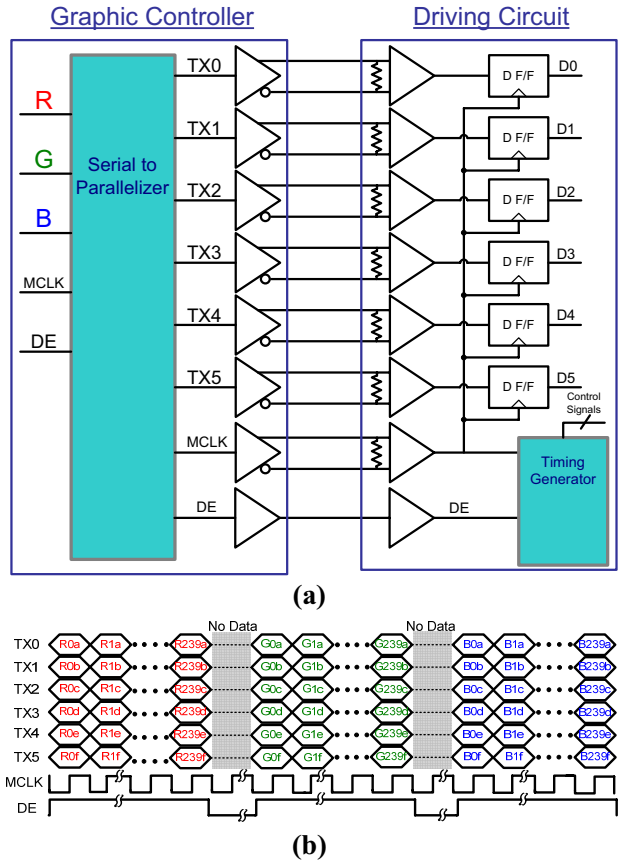

Figure 4: (a) System interface for SoG (b) Data transferring method for SoG

2. Conventional system interface

Conventional interface of a display system is configured as shown in Figure 3-(a) and its simplified timing is in Figure 3-(b). For signaling between the graphics controller and driving circuitry, low-voltage differential signaling (LVDS) scheme is most widely used for its low electro-magnetic interference (EMI), high immunity to common-mode noise, and low power consumption [6].

Graphics controller encodes RGB data which are transferred to display driving circuit along with clock and relevant control signals. The graphics RGB data are encoded with DC balance code. The horizontal and vertical start information is encoded and sent along the RGB data lines. The phase locked loop (PLL) in the driving circuit generates main clock signal which has the same clock period as dot clock of panel. The data rate of RGB data is much higher than the dot clock frequency and in order to receive them, PLL provides multi-phase clock for de-serializing data reception as well.

Because the data rate of RGB data is higher than the dot clock speed, line memory is required to buffer the rapidly incoming data and arrange them properly to meet the display format. Usually, the line memory is located in timing controller. Although the size of line memory is dependent on the architecture of display system, it would occupy substantial area if it is to be integrated on a glass substrate with LTPS TFT.

3. System interface for SoG

3.1 Interface architecture

Because of relatively poor characteristics of LTPS TFT, especially low mobility, the data rate of RGB data cannot be increased much. With the LTPS TFT technology used for this work, the maximum clock speed is limited to 15MHz and thus the number of LVDS data lines becomes larger than for conventional display system with driving circuits implemented with single-crystalline transistors.

As shown in Figure 4-(a), RGB data are transferred along six LVDS data lines. Unlike the conventional architecture, there is no PLL because with LTPS TFTs, it is very difficult to implement good PLL due to the huge variation in the characteristics of LTPS TFTs. Without PLL, however, received RGB data cannot be synchronized to the system clock and the

horizontal and vertical start information cannot be sent along the RGB data lines. Therefore, a control signal (DE = Data Enable) is sent along with the RGB data. For the synchronization of the received data, the output of LVDS receiver is applied to D flip-flop which is toggled by the clock from the graphics controller. This scheme is very similar to the source-synchronous clocking used in high-speed memory interface such as double data rate (DDR) DRAM interface [7].

3.2 Elimination of line memory

In conventional system, red, green, and blue data are sent in parallel and rearranged in the line memory in accordance with the display format and driving method. A pixel is composed of three sub-pixels each of which corresponds to red, green, and blue. If we see the sequence of pixel driving, all the sub-pixels of red color are driven and then other color sub-pixels are driven. That is, sub-pixels of the same color are driven simultaneously. Therefore, if the RGB data are sent in the same sequence as the sub-pixel driving as shown in Figure 4-(b), there is no need for line memory. Of course, the re-arrangement of the graphic RGB data must be performed by the graphic controller.

Normally, line memory is implemented in timing controller to buffer the graphics data. But, for SoG, it would be very costly to integrate line memory on glass because the required area will be very large. In order to avoid the use of line memory in timing controller, the RGB data transmission method is different from the conventional architecture as shown Figure 4-(b).

With 1:3 deMuxing method, RGB sub-pixels share a driving circuit for small area. If the dot clock speed is 5MHz, conventional value for qVGA display, there must be buffers because of the difference between the dot clock speed and incoming data rate. Therefore, we increased the dot clock speed to 15MHz to avoid the use of line memory. Although we can remove the line memory from the timing controller, the number of channels in the shift register is tripled as shown in Figure 5-(a).

3.3 Generation of control signals

Figure 5-(b) shows the timing signals designed to support the line-memory-less operation. HST (Horizontal Start) and VST (Vertical Start) signals are

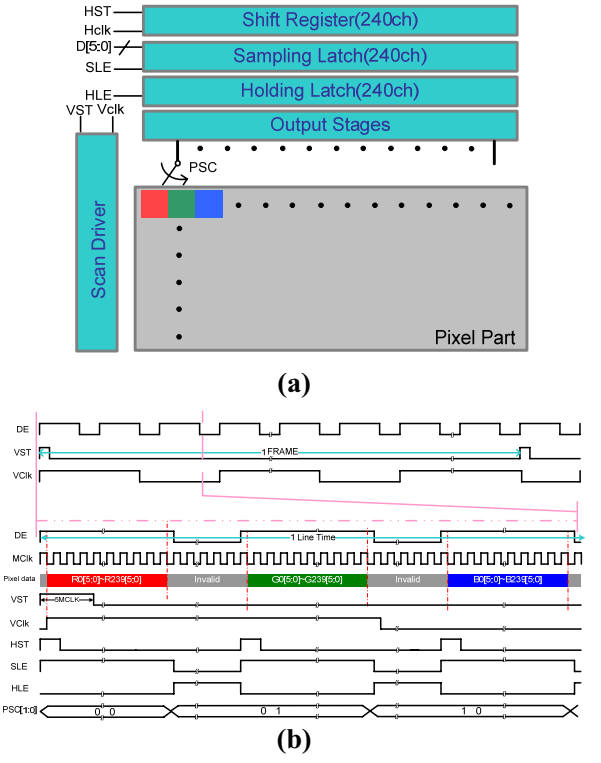

Figure 5: (a) Panel architecture and (b) timing diagram of the proposed SoG system interface.

activated when DE signal arrives. MCLK (Main Clock) represents the dot clock for panel. The sampling and holding latches are operated by latch enable signals, SLE and HLE, respectively. They are set high when one color data are all transferred. PSC (Pixel Switch Clock) is changed when DE is high.

3.4 Offset-compensated LVDS receiver

Large variation of LTPS TFT results in input offset of LVDS receiver which can be much larger than the voltage swing of LVDS input. For error-free reception of LVDS signal, the offset of the receiver must be controlled to be less than 100mV. In conventional schemes, the offset is stored and then subtracted by switched capacitor circuits, which requires extra timing period for offset cancellation and these results in reduced data rate [8]. Therefore, we have developed a full-digital offset compensation scheme where the input offset is compensated during the power-up sequence and the result is used for the normal operation. Thus, there is no need for extra timing period for offset compensation during the normal operation and the data rate can be maximized.

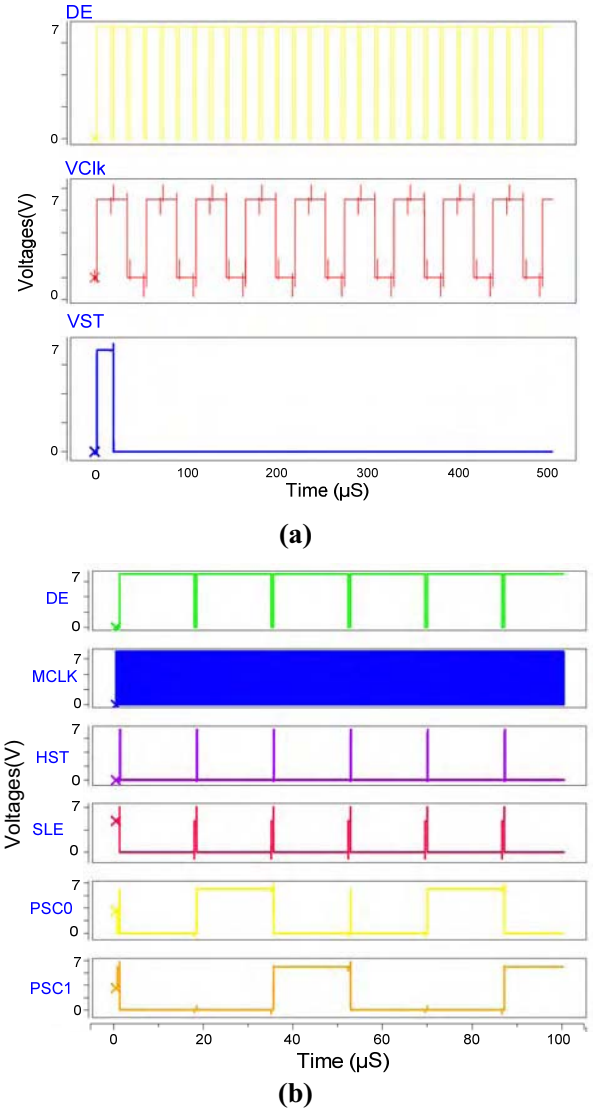

Figure 6: Simulation results of (a) scan driver driving signals (b) data driver driving signals

4. Experimental results

The above described display interface system for SoG has been designed for the implementation with LTPS TFT technology with 4μm minimum channel length. Extensive simulation has been performed with the corresponding TFT parameters considering the variations of TFT characteristics. In Figure 6, the generated timing control signals are shown. We can see the timing control signals are generated appropriately. The interface system dissipates 2.11mW from a 7V supply and the maximum clock frequency is 15MHz. The input offset of LVDS receiver is compensated to be less then 15 mV.

5. Conclusion

For system-on-glass (SoG) with low-temperature poly-silicon (LTPS) thin film transistor (TFT), a new system interface architecture and timing controller are developed. With the newly developed system interface architecture, line memory can be eliminated which would take large area of SoG display panel. The system interface and timing controller are targeted for the application for 6-bit gray scale, 60-frames/s qVGA format.

Acknowledgements

This work was supported by a grant(F0004110) from the Information Display R&D Center, one of the 21st Century Frontier R&D Program funded by the Ministry of Commerce, Industry and Energy of the Korean Government, BK21, and IDEC.

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