GNSS Software Receivers: Sampling and jitter considerations for multiple signals

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Abstract

This paper examines the sampling and jitter specifications and considerations for Global Navigation Satellite Systems (GNSS) software receivers. Software radio (SWR) technologies are being used in the implementation of communication receivers in general and GNSS receivers in particular. With the advent of new GPS signals, and a range of new Galileo and GLONASS signals soon becoming available, GNSS is an application where SWR and software-defined radio (SDR) are likely to have an impact. The sampling process is critical for SWR receivers, where it occurs as close to the antenna as possible. One way to achieve this is by BandPass Sampling (BPS), which is an undersampling technique that exploits aliasing to perform downconversion. BPS enables removal of the IF stage in the radio receiver. The sampling frequency is a very important factor since it influences both receiver performance and implementation efficiency. However, the design of BPS can result in degradation of Signal-to-Noise Ratio (SNR) due to the out-of-band noise being aliased. Important to the specification of both the ADC and its clocking Phase- Locked Loop (PLL) is jitter. Contributing to the system jitter are the aperture jitter of the sample-and-hold switch at the input of ADC and the sampling-clock jitter. Aperture jitter effects have usually been modeled as additive noise, based on a sinusoidal input signal, and limits the achievable Signal-to-Noise Ratio (SNR). Jitter in the sampled signal has several sources: phase noise in the Voltage-Controlled Oscillator (VCO) within the sampling PLL, jitter introduced by variations in the period of the frequency divider used in the sampling PLL and cross-talk from the clock line running parallel to signal lines. Jitter in the sampling process directly acts to degrade the noise floor and selectivity of receiver. Choosing an appropriate VCO for a SWR system is not as simple as finding one with right oscillator frequency. Similarly, it is important to specify the right jitter performance for the ADC. In this paper, the allowable sampling frequencies are calculated and analyzed for the multiple frequency BPS software radio GNSS receivers. The SNR degradation due to jitter in a BPSK system is calculated and required jitter standard deviation allowable for each GNSS band of interest is evaluated. Furthermore, in this paper we have investigated the sources of jitter and a basic jitter budget is calculated that could assist in the design of multiple frequency SWR GNSS receivers. We examine different ADCs and PLLs available in the market and compare known performance with the calculated budget. The results obtained are therefore directly applicable to SWR GNSS receiver design.

Keywords: Global navigation Satellite Systems (GNSS), BandPass Sampling (BPS), Analog to Digital Converter (ADC), Jitter, Phase noise, Phase Locked Loop (PLL).

1. Introduction

The development of the superheterodyne type receivers revolutionized receiver design, relegating previous receiver architectures to occasional, special-purpose use. The advantages of a digital receiver solution are significant, and include reduced system cost, increased temperature stability, finer tuning resolution, faster tuning speed, excellent quadrature channel phase balance, increased filter selectivity, robustness in terms of both hardware and software signal processing algorithms, reconfigurability, advanced signal processing techniques and the ability to store signals for subsequent off-line processing. These benefits have resulted in the digitization process moving closer to the RF front-end, with the ultimate goal of directly digitizing the antenna output. The “Software Defined Radio” (SDR) has been realized [3], allowing reconfiguration of signal processing functions through software, and resulting in reconfigurable radios capable of operating over multiple air interfaces. Research and development continues to extend the capabilities and to increase the robustness of Global Navigation Satellite Systems (GNSS) receivers. Software receivers are quite valuable in evaluating potential improvements because of their flexibility as compared to conventional hardware GNSS receivers, and are more suitable for research and development.

The advent of SDR and other high speed applications imposes exceedingly challenging demands on the state-of-art Analog-to-Digital Converters (ADCs). The ADC is a key component in any radio that uses direct digitization of the RF input signal. The important question is that at what rate the signals should be sampled in order to preserve information. Sampling the received signal using low-pass sampling (LPS), the more usual interpretation of Nyquist’s sampling theorem, requires a sampling rate of twice the maximum frequency of interest. For GNSS, this is of order of 3.2 Gs/s. Analog-to-digital converters (ADCs) that operate at such high frequencies are not readily available - they are expensive and consume a great deal of power [1]. So in order to avoid these constraints, a cheaper, more efficient method of conversion in a SWR is Band-Pass Sampling (BPS). In BPS we can sample the signal at twice the information bandwidth and remain consistent with the Nyquist’s sampling theorem i.e. the signal can be reconstructed from the samples. Another advantage

of using BPS is that it is easily extendable to multiple distinct frequency bands. Akos [4] proposed a novel multi-band digitization method that utilizes BPS to significantly reduce the required ADC sampling frequency. In the case of multi-band sampling, to comply with Nyquist's theorem, the minimum sampling frequency is twice the sum of all the individual bandwidths of interest (however there are other constraints as we will see below). The filters as shown in figure 1 are narrow bandpass filters centered about multiple RF carriers of interest. The appropriate sampling frequency of the ADC is then determined such that all the required bandpass signals are aliased into the baseband without causing aliasing. However, for multiple signals it is critical to find a sampling frequency in which the resulting aliased bands will also not cross the information bandwidth boundaries at 0 and fs/2, and also not overlap each other [5].

Jitter and phase noise describe the same physical effect. While timing jitter describes the fluctuations of zero-crossings of an oscillator output signal, phase noise is the frequency-domain equivalent. The level of phase noise or jitter that can be tolerated is a critical factor in designing the sampling circuit. In the case of BPS the jitter is combined in each of the Nyquist bands within the bandwidth of sampling device and hence causing performance degradation.

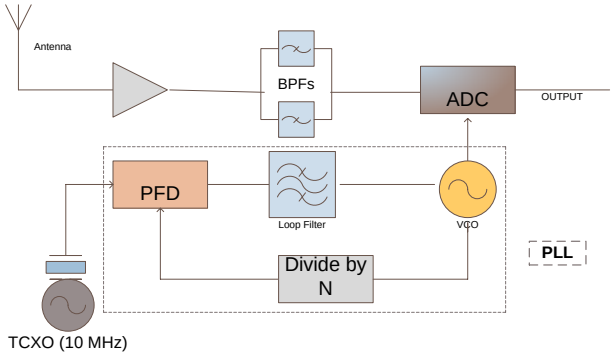

Figure 1. GNSS software radio receiver front-end

The evolution of high resolution ADCs capable of direct IF-sampling requires system designers to make performance/cost trade-off decisions on low jitter and phase noise circuits. The contributions to the system jitter are the aperture jitter of the sample-and-hold switch at the input of ADC and the sampling-clock jitter. Aperture jitter, otherwise referred to as aperture uncertainty, is one of the limiting factors in any sampling system. Today system designers may not adequately specify the jitter requirements for the data converter clock and, as a result, system performance is degraded. In many cases the sampling clock jitter is several times larger than the ADC aperture jitter and is therefore the dominant contributor to SNR degradation [6]. It is difficult, though not impossible; to change the ADC aperture jitter but a number of things can be done to reduce the sampling-clock jitter. Walden [7] and Le [8] produced perhaps the best overviews of the ADC performance trends. However, our survey is based mainly on the aperture jitter, input sampling frequency and sampling rate of the ADC as we are dealing with very high frequency signals i.e. the GLONASS G1 signal is 1.6 GHz.

Sampling-clock jitter has several sources: phase noise in the VCO within the sampling PLL, jitter introduced by variations in the period of frequency divider used in sampling PLL and cross-talk from the clock line running parallel to signal line. Sampling clock jitter based on PLL design parameters has been subject of numerous studies which provide many models to predict the overall jitter at the output of PLL (Mansuri [9], Lee [10], Kundert [11]).

Dempster [1] evaluated the jitter requirement such that the noise due to jitter at the carrier frequencies of GNSS signals was 10dB less than the thermal noise. These jitter requirements do not vary very much with the loosest (6.35ps) being only 3.1 times the tightest (2.05ps) for different classes of single frequency GNSS receiver. The tightest of these jitter requirements is for the GPS L1 band. Keeping in mind these sources of jitter in a multiple frequency GNSS receiver, a budget is designed and various approaches to satisfy the jitter requirements based on ADC and PLL design parameters is discussed.

This paper is organized as follows: In section 2, BPS considerations for multiple bandpass signals are discussed and the minimum non-overlapping sampling frequency is calculated and graphically represented using a MATLAB routine for various receiver types. In section 3, we have evaluated the required jitter standard deviation allowable for each GNSS band of interest. In section 4, first we have discussed the performance limitations of ADCs, characterized the different ADCs available in the market and compared the known performance with that of calculated budget. Second, the different noise sources in a PLL are discussed and then the jitter budget based solely on VCO phase noise is calculated, since the VCO noise has much stronger impact on PLL jitter than any of the other noise sources. Finally, the total jitter budget is calculated.

2. BandPass Sampling (BPS) considerations

Software radio has been described as a revolutionary advance in receiver design but the fundamental design philosophy is simple. The ADC should be placed as near as possible to the antenna in the chain of front-end components and the resulting samples should be processed using a programmable microprocessor. In software radio, the goal is to minimize the number of analog components, and ideally sample the signal at RF. There are two ways to consider the required sampling rate of the ADC involved. One is based on centre frequency and the other is based on information bandwidth. Sampling the received signal using Low-Pass Sampling (LPS), the more usual interpretation of Nyquist's sampling theorem, requires a sampling rate of twice the maximum frequency of interest. For GNSS, this is of order of 3.2 Gs/s [12]. Sampling at such a high frequency will consume a great deal of power. A cheaper, more efficient method of conversion in a SWR receiver is Band-Pass Sampling (BPS). Using BPS we can sample the signal at twice the information bandwidth rather than the highest frequency in the signal. At this point we can clearly restate the Nyquist Criterion: *A signal must be sampled at a rate equal or greater than twice its* ***bandwidth*** *in order to preserve all the signal information.* As depicted in figure 1, the signal enters through the antenna and is amplified by a Low Noise Amplifier (LNA) along with all frequencies within the bandwidth of LNA. The signal then attenuated, when it is passed through a narrow BandPass Filter (BPF) centered about the carrier frequency. When several bands are required for downconversion, the minimum sampling rate is twice the sum of bandwidths. So, a sampling frequency f_s is chosen, which defines the resulting sampled bandwidth. This can be ensured if certain constraints are met as described by Akos [4]. The Intermediate Frequency (IF), can be found as

$$fix\left(\frac{f_c}{f_s/2}\right) is \begin{Bmatrix} even,\ f_{if} = rem(f_c, f_s) \\ odd,\ f_{if} = f_s - rem(f_c, f_s) \end{Bmatrix} \quad (1)$$

If the following constraints are not met a portion of the information bandwidth of the signal can fold on top of itself creating interference.

$$\left| f_{if_b} - f_{if_a} \right| \geq \frac{BW_a + BW_b}{2} \; for, a = 2, ..., N \qquad (2)$$

$$b = 1, ..., a$$

We have developed a routine in MATLAB to calculate the minimum sampling frequency meeting the above mentioned constraints. The results are shown in the table 1 for different multiple-band receivers.

Table 1. Sampling and jitter considerations for example GNSS receivers. * denotes wideband (14 MHz) Galileo L1

Receiver/ Bandwidth (MHz)	GPS			Galileo				GLONASS		f_{smin}	$\sigma_{\tau_{Allowable}}$ (ps)
	L1	L2C	L5	L1	E5a	E5b	E6	G1	G2		
	2	2	24	4	24	28	40	19	15		
A										10.8 MHz	2.0
B										18.5 MHz	2.0
C										55.7 MHz	1.1
D										76.8 MHz	2.0
E*										37.7 MHz	1.2
F										77.0 MHz	2.0
G										78.9 MHz	1.1
H										60.4 MHz	1.1
I										445.3 MHz	1.1

The combination of signals was selected that are likely to be common within a GNSS receiver. Type 'I' is the most expensive receiver processing all the available GNSS signals, with a very high non over-lapping sampling frequency of 445.3 MHz. Receiver types 'B' and 'E*'are similar type of receivers, the only difference is that type 'E*' receiver exploits the MBOC modulation technique i.e. 14 MHz bandwidth. The increase in bandwidth results in the increase of sampling frequency from 18.5 MHz to 37.7 MHz i.e. almost double. Receiver type 'A' is the cheapest arrangement, simply using GPS L1 and L2C signals only.

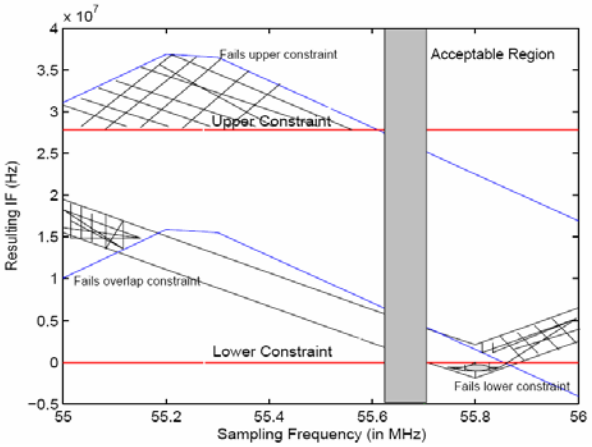

Figure 2. Resulting IF's for a range of sampling frequencies for receiver type 'C'

The plot in figures 2 and 3 depicts the resulting frequency of information bands for receiver type 'C' and 'H' respectively. The horizontal axis indicates the sampling frequency after frequency down-conversion. The shaded area in figure 2 shows the acceptable region of sampling frequencies. If the frequency after down-conversion exceeds the upper constraint ($f_s/2$) or is below the lower constraint (0), the noise aliasing arises. The sampling process is critical for software radio based GNSS receivers with bandpass sampling techniques as it requires selection of an appropriate ADC based on certain design parameters. Another requirement is narrow bandpass filter centered about the carrier frequency to attenuate all the noise outside the information bandwidth. In case of high frequency narrow band signals, the BPF may require a very high Q.

3. Jitter limits

In BPS the sampling rate is lower than twice the maximum frequency of the signal; therefore the SNR will be worse than that from an equivalent analog system, in which the SNR is preserved. The BPFs in figure 1 are used as Anti-Aliasing (AA) filters prior to BPS. These filters can only reduce the out-of-band noise. In that case, out-of-band rejection must be very good because the out-of-band noise is aliased into the baseband. Aperture jitter effects in sampled systems have usually been modeled as additive noise. However, in GNSS receivers exploiting BPSK, large errors can occur if the jittered sample crosses a data bit boundary.

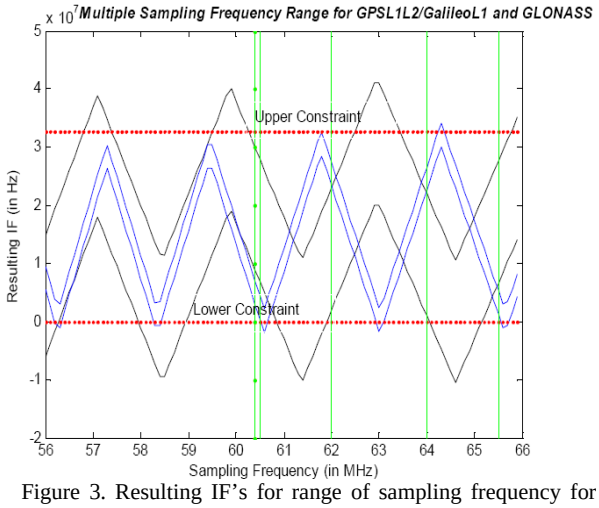

Figure 3. Resulting IF's for range of sampling frequency for receiver type 'H'

Dempster [2] evaluated the jitter requirements for BPSK system and found to give a higher value than previous expressions for typical satellite navigation signals. The power of jitter noise signal is:

$$N_\tau \approx A^2 \left(\frac{\sqrt{2}\sigma_\tau}{\sqrt{\pi} T_d} + \frac{w_c^2 \sigma_\tau^2}{2} \right) \qquad (3)$$

It is assumed that jitter is relatively small with respect to the carrier frequency, so the SNR due to jitter is

$$SNR_j = \frac{S}{N_\tau} = \frac{A^2/2}{A^2\left(\frac{\sqrt{2}\sigma_\tau}{\sqrt{\pi}T_d} + \frac{w_c^{\,2}\sigma_\tau^{\,2}}{2}\right)} \quad (4)$$

In order to keep jitter contribution to an insignificant size, the jitter noise power is restricted to 10dB down from the thermal noise power [1],

$$SNR_j = \frac{1}{\left(\frac{2\sqrt{2}\sigma_\tau}{\sqrt{\pi}T_d} + w_c^{\,2}\sigma_\tau^{\,2}\right)} \geq 10\frac{S}{N_{th}} \quad (5)$$

where S is the signal power and $N_{th}=kTB$ is the thermal noise power, with the data bandwidths of interest B for each of the individual bands. By rearranging equation 5 becomes

$$w_c^{\,2}\sigma_\tau^{\,2} + \frac{2\sqrt{2}\sigma_\tau}{\sqrt{\pi}T_d} - \frac{N_{th}}{10S} \leq 0 \quad (6)$$

By solving equation 6 using quadratic equation method, it is possible to evaluate the required jitter standard deviation allowable for each GNSS band of interest. Evaluating the above expression for various GNSS bands gives the jitter requirements in table 2.

Table 2. Allowable jitter limits for GNSS bands

GNSS Signals	Allowable Jitter (ps)
GPS	
L1	2.0
L2C	2.5
L5	6.7
Galileo	
L1	2.5
L1*	1.2
E5	2.4
E6	6.2
GLONASS	
G1	1.1
G2	1.4

Dempster [1] evaluated the jitter requirements for a sinusoidal signal such that the noise due to jitter at the carrier frequencies of GNSS signals was 10dB less than the thermal noise. These jitter requirements do not vary very much with the loosest (6.35ps) being only 3.1 times the tightest (2.05ps). We have performed the same analysis, but the jitter noise is evaluated using BPSK signal. The new expression doesn't give significantly different results to [1]. It gives the tightest requirement for GLONASS G1 i.e. 1.1ps and loosest for GPS L5 i.e. 6.7ps. Interestingly, receiver type 'E*', exploiting MBOC modulation has the second tightest requirement in terms of jitter which is around 2 times more than receiver type 'B'. This is because of the fact that strength of signals exploiting MBOC modulation is 2.2 times more than BOC modulated signals [13].

4. Jitter budget for GNSS software receiver design

In this section, a basic jitter budget is calculated that could assist in the design of SWR GNSS receivers. There are a number of parameters that are involved in designing a jitter budget of ADCs for GNSS software receivers, but we have designed our budget based on three types of performance parameters for ADCs: sampling rate, jitter and input signal bandwidth. Since the GLONASS G1 signal is 1.602 GHz, we require ADCs which can operate on such high frequencies. Psiaki [15] has used Dallas Semiconductor MAX104 ADC, with an input bandwidth of 2.2 GHz, a maximum sampling rate of 1GHz and an aperture jitter of less than 0.5*ps*.

The carrier frequency for GNSS receivers is high enough so that the timing inconsistencies, such as clock jitter (phase noise) and ADC aperture jitter, can increase noise when the signal is sampled by the ADC. The noise sources include the quantization noise of the converter (or the ac differential-nonlinearity error), the internal converter thermal noise, and the system jitter. The ADC quantization noise and thermal noise have a direct effect on the converter's Signal-to-Noise Ratio (SNR). The contributors to the system jitter are the aperture jitter and sampling-clock jitter. Since both of these terms are uncorrelated they can be combined in a root-sum-square basis to give the total system jitter [6]:

$$\sigma_T = \sqrt{\sigma_a^{\,2} + \sigma_c^{\,2}} \quad (7)$$

where σ_T is the total system jitter. σ_a and σ_a is aperture jitter and sampling-clock jitter respectively.

4.1 Aperture Jitter

Aperture jitter, also known as aperture uncertainty, is the uncertainty in the aperture time. Aperture jitter stands for the random sampling time variations in ADCs which are caused by the thermal noise in sample and hold circuit. Walden [7] identified the aperture jitter as the dominating error effect that limits the achievable Signal-to-Noise Ratio (SNR). The product data sheet indicates the aperture jitter specification for most of ADCs. Aperture jitter is often specified as an rms value, which represents the standard deviation in the aperture time.

Le [8] determined the maximal allowable aperture jitter with respect to the input signal's frequency and the ADC's resolution by

$$\sigma_a = \frac{1}{2^N . \pi . f_{\max}} \quad (8)$$

where f_{max} is the maximum frequency of the input signal, and N is the stated number of bits. Based on the above equation the analysis for various ADCs available in the market, is shown in table 3. σ_a' is the aperture jitter as specified by the vendor. GLONASS G1 signal has the highest frequency of all the other signals i.e. 1.6 GHz. So the tightest of the aperture jitter requirements is for the GLONASS G1 signal (which also has the tightest jitter limit). While using the maxim MAX104 ADC the calculated aperture jitter using equation 8 for the GLONASS G1 signal is 0.77*ps*.

4.2 Sampling-clock Jitter

Clock jitter is a property of the clock generator that feeds the ADC with the clock signal. It is caused by the phase noise of the oscillator and generates additional sampling time errors in the ADC [14]. Most of the high speed communication systems which include radio transmitters and receivers use phase-locked loops for frequency synthesis such as in figure 1. Such systems suffer from sampling-clock jitter, defined in the time domain as the random variations in the sampling phase of the signal, or in the frequency domain as phase noise.

In GNSS software radio receivers as depicted in figure 1, clock jitter can originate in the oscillator/synthesizer system that provides the ADC sample clock. Sampling frequencies have been generated using frequency synthesizers that employ frequency dividers and PLLs to develop clock signals based on reference

oscillator signals.

Jitter and phase noise characterize the same phenomenon. However, oscillators are most often specified in terms of phase noise. Therefore, the approximation of rms jitter based upon phase noise is required. In order to convert the phase noise into jitter following expression is derived in the previous work [12],

$$\sigma_c = \frac{1}{2\pi f_c}\sqrt{\phi(t)} = \frac{1}{2\pi f_c}\sqrt{2\int_{f_1}^{f_2} 10^{\pounds(f)/10}\,df} \qquad (9)$$

where,

$$\pounds[\text{dBc/Hz}] = 10\log_{10}\frac{P_{sideband}}{P_{carrier}} = 10\log_{10}(S_{SSB}[1/Hz]) \qquad (9a)$$

Table 3. Jitter specifications for commercially available ADCs

ADC	Input (Hz)	Sampling Frequency	σ_a '(ps)	N (bits)	σ_a (ps) From (8)
MAX104	2.2G	1Gsps	<0.5	8	0.77
MAX108	2.2G	1Gsps	<0.5	8	0.77
MAX106	2.2G	600Msps	<0.5	8	0.77
ATMELTS83	3.3G	2Gsps	<0.2	10	0.10
ATMELAT84	3.0G	1.5Gsps	<0.1	10	0.20
ATMELS003	3.3G	2.2Gsps	<0.2	10	0.10
LTC2208	700M	130Msps	<0.07	16	0.01

Kester [6] mentioned a similar expression for conversion of phase noise into jitter, by approximating the phase noise curve into a number of individual line segments, and the end point of each line segment are defined by data point. The rms jitter in seconds is given by

$$\sigma_c = \frac{1}{2\pi f_c}\sqrt{2\times 10^{A/10}} \qquad (10)$$

The area of the curve *A* is obtained by integrating the phase noise power over the frequency range of interest. The upper frequency of integration should be twice the sampling frequency and the lower frequency of integration should be as low as possible.

Computer programs are available online to calculate the rms jitter. The calculations in this paper are based on the program by Raltron Electronic Corporation which converts phase noise into jitter, using the same technique as mentioned above.

Table 4. Jitter specifications for commercially available PLLs

PLL	Frequency Range (Hz)	*SSSB* @ 1KHz (dBc/Hz)	SSSB @ 10KHz (dBc/Hz)	SSSB @ 100KHz (dBc/Hz)	σ_c *(ps)*
Vectron	1 ~ 800 M	-120	-140	-145	0.8
ADF	10 ~ 250 M	-80	-100	-111	1.8
Wenzel	10M	-130	-155	-165	1.0
WA	10M	-166	-167	-167	0.2
RF PL	1M ~ 2.4 G	-125	-140	-150	1.3

4.3 Phase Noise in PLL

In a PLL, each block contributes to a certain extent to the total phase noise but VCO noise is typically the dominant source [7]. Other sources of noise in a PLL system consist of phase detector, reference signal and frequency divider. Therefore other noise sources are neglected for simplicity as VCO noise has much stronger impact on the PLL jitter. When VCOs are embedded inside a PLL, the loop dynamics will modify the noise characteristics. Phase noise spectral components below the corner frequency, the negative feed back means that the PLL output will closely follow the PLL input, and the phase noise of the oscillator is attenuated. Above the corner frequency the feed back falls. This means that the phase noise of the PLL output will be increasingly determined by the phase noise of the oscillator and less by input phase noise of reference signal. It is desirable to have corner frequency (loop bandwidth) as large as possible to attenuate noise, but for stability reasons, the loop bandwidth should not exceed one tenth of the VCO frequency [16].

Lee [10] gave an expression for the calculation of jitter in a VCO, based on phase noise measurement

$$\sigma_c = \sqrt{\frac{\pounds(f)\,f^2}{f_c^3}} \qquad (11)$$

where *10log(f)* falls at the rate of 20 *dBc/Hz* per decade. PLL jitter due to VCO noise can be calculated from the measured or simulated phase noise of the VCO, which is typically known before the PLL design. Herzel [17] gave an expression to calculate absolute rms jitter of a PLL from phase noise of the VCO in 20 *dB/decade* region.

$$\sigma_c = \frac{f_{offset}}{f_c}\sqrt{\frac{S_{SSB}}{4\pi B_L}} \qquad (12)$$

S_{SSB} is the single sideband phase noise of the VCO, taken at an offset frequency in the region of spectrum with a -20dB/decade slope. S_{SSB} can be measured from $\pounds$ (*dBc/Hz*) using equation 8a. B_L is the loop bandwidth of first order PLL. Loop bandwidth is the most critical system design parameter for a PLL, and as stated earlier that the phase noise inside the loop bandwidth is dominated by VCO. Loop bandwidth has only a small impact on phase noise inside the loop bandwidth but narrower loop bandwidths can reduce phase noise outside the loop bandwidth.

PLL as a first order system does not give a finite jitter [17], so flicker noise in the VCO within a second-order PLL model is included. So, the equation 12 takes the form

$$\sigma_c = \frac{f_{offset}}{f_c}\sqrt{\frac{S_{SSB}}{4\pi B_L^{eff}}} \qquad (13)$$

where the effective loop bandwidth is defined by

$$B_L^{eff} = \frac{\varsigma w_n^2}{\pi w_n + 4\pi f_c \varsigma f(\varsigma)} \qquad (14)$$

In the absence of flicker noise we have

$$B_L^{eff} = \frac{2\varsigma w_n}{2\pi} \qquad (15)$$

Herzel [17] suggests that the flicker noise can be suppressed by increasing f_n to ten times the corner frequency f_{cor}, that is

$$\sigma_c = \frac{f_{offset}}{f_c}\sqrt{\frac{S_{SSB}}{8\pi\varsigma f_n}} \qquad f_n \geq 10\,f_{cor} \qquad (16)$$

Based on above equation the clock jitter exhibited by various PLLs is shown in the table 4. Sampling clock frequency used in calculations is 10MHz. Since the jitter is dependent only on the phase noise of VCO, therefore all the other quantities are constant

except VCO phase noise.

4.4 Total System Jitter

The total system jitter is calculated by considering the aperture jitter and sampling-clock jitter. The total jitter at the output of ADC is given by equation 7. In order to meet the minimum jitter requirements, ADC and PLL with the minimum jitter specification are considered. As shown in table 3, the least expensive ADC, Maxim MAX104 has a specification which can meet our requirements with ADC aperture jitter only 0.77*ps* and cost is much less than the other ADC's. Similarly, Wenzel WA 5100 has the best jitter specifications for a 10MHz sampling clock input i.e. 0.2*ps* as shown in table 4. Note the ADF and RF PLL themselves cannot meet the G1 jitter specifications in table 1. The PLLs have similar costs. Therefore, the total jitter at the output of ADC for single band receiver i.e. GPS L1 receiver is

$$\sigma_T = \sqrt{0.77^2 + 0.2^2} = 0.79\,ps$$

which is meeting our design requirements of less than 1.1*ps* of jitter for all the receiver types incorporating GLONASS G1 signal. By substituting 0.79*ps* in equation 6, satisfies the equation, therefore validating the result.

5. Conclusions

This paper discusses the BandPass Sampling (BPS) and jitter considerations for multiple band GNSS software radio receivers. Selection of a suitable sampling frequency is very crucial in BPS technique. In this paper we have calculated the minimum sampling frequency, that alias the frequency bands of interest onto non-overlapping portions of the Nyquist bandwidth, for multiple frequency software GNSS receivers incorporating GPS, Galileo and GLONASS signals. The analysis evaluates the jitter requirements for BPSK signals such that noise due to sampling jitter at carrier frequencies of GNSS was 10*dB* less than thermal noise. For all GNSS bands, this requirement was of the order of picoseconds. Receiver types incorporating GLONASS G1 signal has the tightest requirement for jitter i.e. a standard deviation of less than 1.1*ps*.

Furthermore, we have investigated the sources of jitter and a basic jitter budget is calculated that could assist in the design of multiple band SWR GNSS receivers. Aperture jitter and sampling clock jitter is defined and the individual contribution of each of them to the total system jitter is calculated. The relationship between phase noise and jitter is mathematically expressed as oscillators are most often specified in terms of phase noise. Different ADCs and PLLs available in the market, which match our specifications, are examined and known performance with the calculated budget is compared. The results obtained are therefore directly applicable to a multiple band SWR GNSS receiver design. Although it is impossible to address all the possible variations, there are some general recommendations for designing a multiple band GNSS receiver front end:

- BPS technique provides a good alternative to LPS for multiple band GNSS receivers, at the cost of increase in the total system jitter. High input frequency by BPS causes a large jitter effect and hence large SNR degradation.
- Bandpass Filter (BPF) design is an important factor, because a multi-frequency BPF upstream of ADC prevents unwanted out of band signals and noise getting aliased on the top of signals of interest.
- Analysis of jitter in ADCs revealed that the application circuit cannot be changed to improve the ADC's aperture jitter. However, several techniques can improve the clock jitter.
- When designing the receiver front end, sampling clock jitter and phase noise should be taken into account. The clock source need not be expensive but it must have low noise.
- Input bandwidth that manufactures mention in datasheets is not an indication that a device will hold the performance up to those input frequencies, but it is usually the flatness of ADC response vs. input frequency.
- In order to get a more accurate measure of phase noise in a phase locked loop, all the other sources of phase noise should be considered as each noise affects the total output.

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